Update on Peripheral Electronics

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Multilayer Bus Status

- Two contacts with CERN during August:
  - reported is the email received by Bertrand Mehl on August 8th

Dear Mauro.
All was good after the last mail.
The production is not easy with the fine tracks and the fine pads in aluminum but it is in process.
However it is long because for us it's height "single layer" board before the press.
We have produce the raw material to follow your stack up that you have discuss with Rui.
We have had the substrate that is missing under the last layer on your first stackup.
I will inform you of the progress of the job.
Best regards. Bertrand

- Two weeks ago a similar mail received: they told us that they are still working on the BUS … not other real info
- I am trying to schedule a meeting with them to go into the details
  - It will be useful to understand where the production difficulties are
  - We would like to get advices on what can be changed in the «next» revision of the design
- We want to use the meeting to initiate layer 0 fan-out production
  - (see next slide)

Layer 0 Fan-out Status

- → After Elba meeting: careful check on the layout has been performed
  - → To include features requested by
  - → Luciano: strip identification
  - → Fillippo: alignment reference for positioning fan-out on sensor
  - → Stefano: additional pads for testing
    - → *Last point not really achieved so far !! … thinking more towards a "bed of nail" approach with rounded tip to avoid damage to the pads*.

- → In the meantime follow up with CERN: email received sometime in July

Dear Mauro,
We looked at the feasibility of the pcb STRIPLETS_BUS with Mr DE OLIVERA.
The manufacture is complicated so we can do with the following stack:
BOTTOM => 50um Kapton / Copper 5um / Glue 10um / 50um kapton / copper 5um / gold => TOP
The price is 5500 CHF for 4 pieces. Best regards, Bertrand MEHL.

- → Phone discussion are on-going to:
  - → Decrease material thickness to real minumum
  - → Agree on two productions: single layers + full 2-layer fanout
  - → Convince Rui to initiate an Aluminum version in parallel ….

Other Components Status

- We have completed the firmware to perform test on the Pixel Bus
  - The system was developed in collaboration with Sanitas s.r.l.
  - We are basically waiting for the Bus
- We have ordered some other components, connectors + micro data and power cable to start Tail "understanding" and design
- We have acquired "nails" for Fanout testing, we are designing a gadget to test the idea
- Discussion on going with people from the CERN Versatile team to
  - Get some optical package
  - Understand other possible small size solution for electrical-to-optical translation (custom packages proposed by K.K. Gan for example)
  - Understand the "potential" of the GBT system for our application
- Transition card: Component placement initiated … assuming FPGA on board for data formatting/serialization
  - Goal is to have a test bed of the full chain by next spring

TDR Status

- → Section 6.9.1 Fanout for Layer 0 and 6.10.5 Hybrid Design will be ready by Friday afternoon
  - → Some repetition with other sections of the document still present
  - → They will need another “pass” to polish/correct them

- → Section 6.10.6 Data transmission
  - → First reasonable draft by Monday evening
  - → I have the feeling that it is more a “proposal” than a really paragraph in a TDR