PID Summary

Pisa SuperB Meeting
September 21rst 2012

Nicolas Arnaud,
for the SuperB PID group

FDIRC

- Prototype at SLAC CRT almost ready to take data
  - Commissioning in progress
    → Hawaii IRS-2 electronics
  - Software developments (simulation, reconstruction)
  → If not major delay, should have first results for the December meeting
- Promising first tests of the FEE TDC chip (SCATS)
  - LAL + Bari (+ Caen) involved
- On track for a submission of the front-end chip at the end of the year
- Detailled background studies in progress
  - Rates down w.r.t. Elba (bug in the simulation)
- Proposal from Guy to submit a project to the ERC advanced grant call (2012/11) for an ‘European-based quartz PID center’
  → Discussions among the group; interest for this project and to submit other projects to a more junior grant call called ‘consolidator’ (early 2013)
- Ongoing studies: motherboard (Padova) & MaPMT (Bari)
- Padova and Bari will likely get funding to buy a second FBLOCK (camera)

FTOF

- Background studies ongoing
  - TDR oriented

- Design to be updated asap

  $\rightarrow$ Based on the new drawing of the forward side shown this morning
  - Simulation (BRN) will then be updated accordingly

TDR

- Both barrel and forward chapters almost complete

- Editing/tuning work still ahead of us
  - Major task for a ~60 pages draft
  - Final reader: Doug Roberts

- Dedicated parallel session yesterday
  → Jerry already started implementing comments

- Electronics summary included in the ETD chapter today

- Inputs to the MDI chapter being written