SVT-Status

5th SuperB Collaboration Meeting

Pisa, Sept - 2012

- Studies completed for TDR since Elba
- Summary from SVT parallel sessions
- TDR status

Giuliana Rizzo
Universita' & INFN Pisa

Hit time resolution & back. occupancy

Some significant progress during the summer useful to complete TDR:

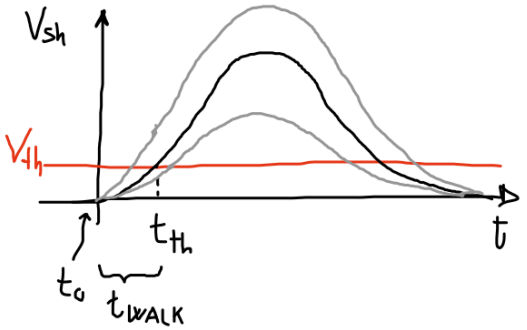
1. New/more reliable simulation of the hit time resolution to define time window cut for reconstruction/offline occupancy

L.Ratti PV

   - Now include noise effects and sim. results are able to reproduce time resolutions achieved in BaBar data.

2. With present background simulation and new time window cut SuperB average offline cluster occupancy ~ 2% (x5 safety included) only 2-3 times higher than average BaBar occu.
   - Studies on BaBar data in high background conditions (L1 cluster occup. up to 5%) used to evaluate hit-to-track efficiency in SuperB : 95% with 3% cluster occu!

N. Neri (MI)
I. Ripp-Baudot (IPHC Strasbourg)



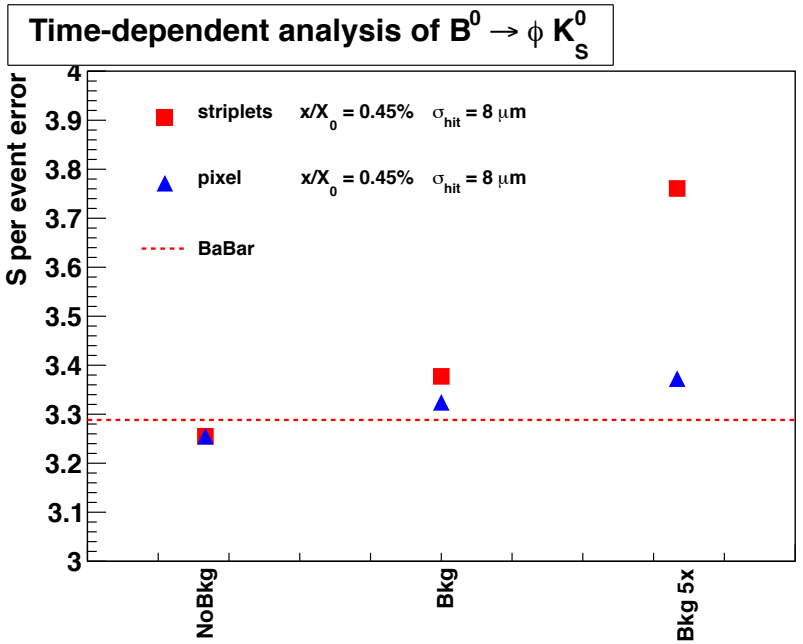
Layer	View	Shaping time	Offline time window (+/- 5x NEW time resolution) ns	offline cluster occupancy (x5 included)
0	1	25	100	0.018
0	2	25	100	0.018
1	phi	75	110	0.016
1	z	75	110	0.016
2	phi	100	120	0.015
2	z	100	120	0.017
3	phi	150	150	0.030
3	z	150	150	0.015
4	phi	500	500	0.027
4	z	500	500	0.022
5	phi	750	550	0.023
5	z	750	550	0.017

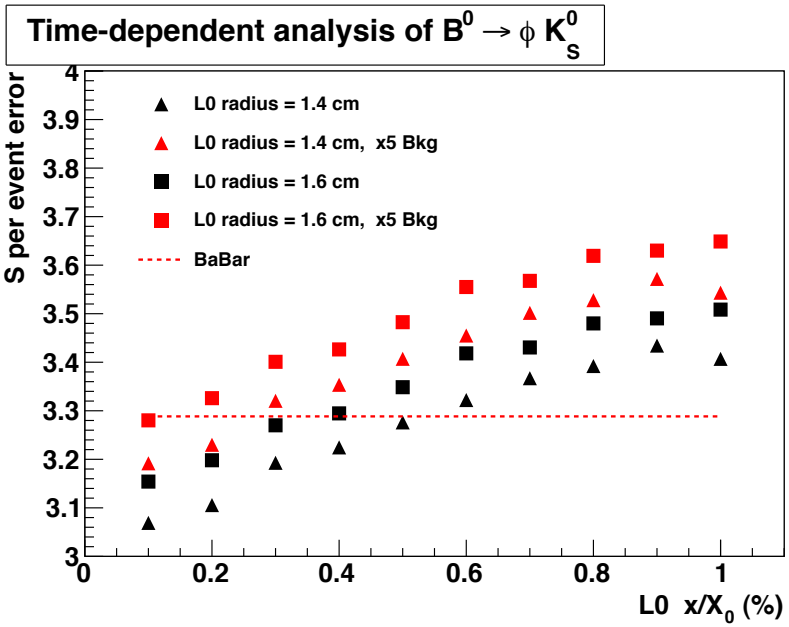
Fastsim Studies completed

N.Neri MI

3. Fastim performance comparison for striplets and pixel in Layer0 completed

- As expected pixel performance more robust in high background (pixel occup. 200 times smaller than striplets)→ main motivation for pixel upgrade for full luminosity.
  - With x5 background, sensitivity to S reduced by 15% with striplets, while only 3% degradation seen with pixel with same material budget assumed.
- Thinner pixel options can further improve S sensitivity even with nominal background





G. Rizzo

FE chip S/N update

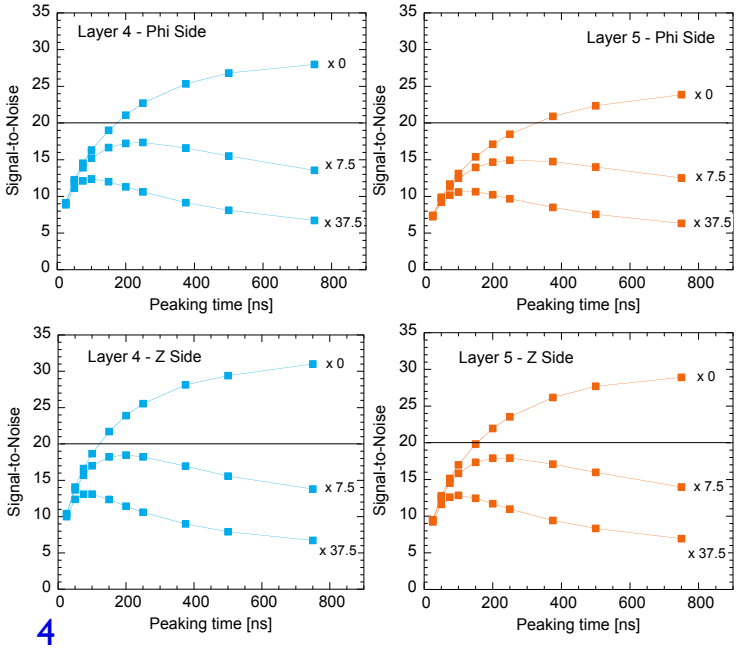
PV/BG-MI-TS

4. Higher neutron fluence found in SVT (bug fix in July) and effect on leakage current and FE noise reevaluated
   - S/N marginal (<10) in L4-5 with 7.5 yrs x5 safety
   - A few knobs to improve the situation.
   1. Reduce ambient temperature (T=12^0 C, in this table)
   2. Reduce shaping time.

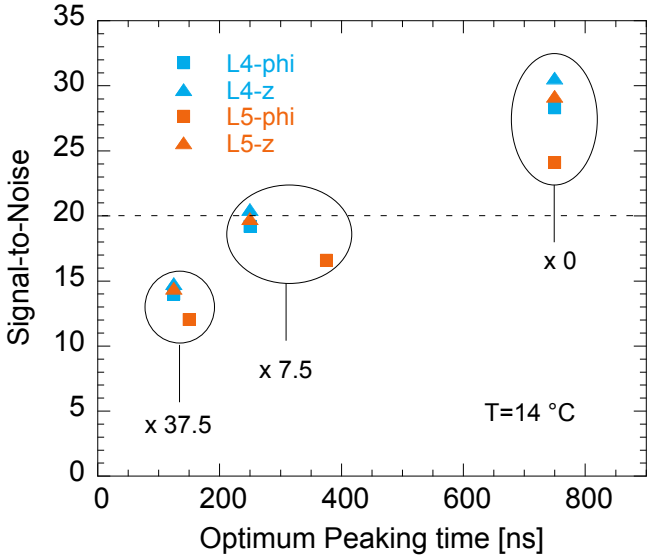
Need to investigate effect of some neutron shield in the hall

Layer	View	Shaping time	S/N at the start of data taking	S/N in 75 ab-1	S/N in 75 ab-1 x5 bkg
0	1	25	17	17	16
0	2	25	17	17	16
1	phi	75	21	20	16
1	z	75	32	27	18
2	phi	100	22	20	16
2	z	100	34	27	18
3	phi	150	27	21	14
3	z	150	34	27	16
4	phi	500	22	17	10
4	z	500	29	19	11
5	phi	750	22	14	8
5	z	750	30	18	10

S/N ratio vs t_P at 1 MIP



Simulation performed at T=14 °C



G. Rizzo

SVT Parallel sessions

16:30->*18:30* **Parallel 1 - SVT** (Convener: Giuliana Rizzo (*PI*)) (Aula 131) EVO meeting information; EVO meeting url

16:30	Introduction (10') (Slides)	Giuliana Rizzo (*PI*)
16:40	Update on background simulation (20') (Slides)	Riccardo Cenci (*University of maryland*)
17:00	First look at INMAPS irradiated chips in Pisa (20') (Slides)	Stefano Bettarini (*PI*)
17:20	First look at INMAPS irradiated chips in Pavia/BG (20') (Slides)	Lodovico Ratti (*PV*)
17:40	Update on Strasbourg activities on 180 nm technology (20') (Slides)	Isabelle Ripp-Baudot (*IPHC, CNRS/IN2P3, Strasbourg*)

08:30->*10:30* **Parallel 2 - SVT** (Convener: Giuliana Rizzo (*PI*)) (Aula 131) EVO meeting information; EVO meeting url

08:30	Update on activities in UK (20') (Slides)	Adrian Bevan (*Queen Mary*)
08:50	Update on peripheral electronics (TBC) (20') (Slides)	Mauro Citterio (*MI*)
09:10	SVT ambient temperature reduction: discussion (10') (Slides)	Filippo Bosi (*PI*)
09:20	November testbeam: discussion (20') (Slides)	Stefano Bettarini (*PI*)
09:40	Discussion on TDR budget and schedule (20') (Slides)	
10:00	TDR reading (30')	

11:00->*13:00* **Parallel 3 - SVT** (Convener: Giuliana Rizzo (*PI*)) (Aula 131) EVO meeting information; EVO meeting url

11:00	TDR reading (2h00')	

SVT Background Update

R. Cenci - Maryland

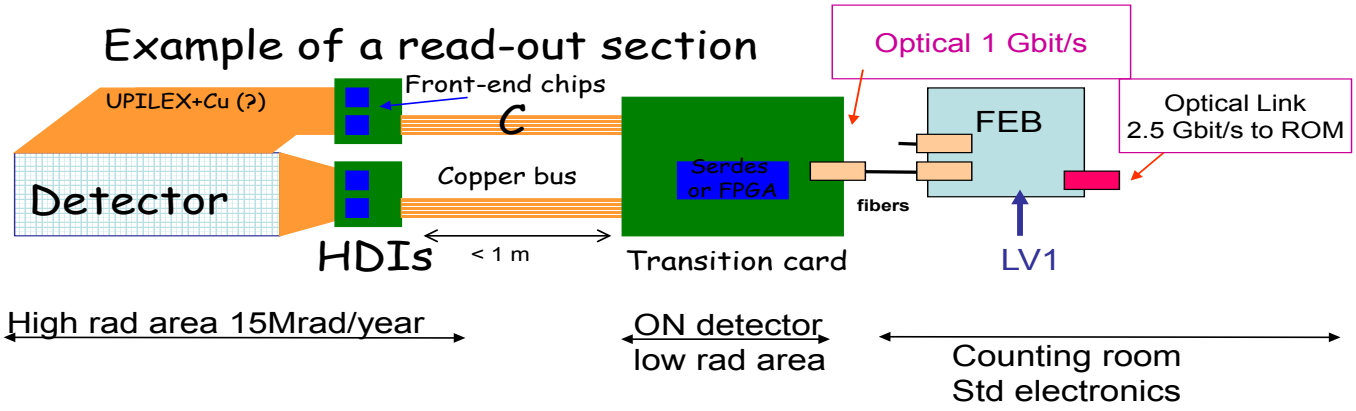
- Small contribution from new RadBhabha
- L0 lower rate due to different radius (Jun12, Sep12)

LAYERS	2photons				Bbbrem		Touschek HER		Touschek LER		BeamgasHER		Beamgas LER		Bbbrem LowΔE
MHz/cm^2	Jan12	May12	Jun12	Sep12	May12	Sep12	May12	Sep12	May12	Sep12	May12	Sep12	May12	Sep12	May12
L0 phi	29.4	30.1	18.7	18.8	0.83	0.54	0.62	0.40	1.70	1.39	0.47	0.37	1.48	1.12	0.013
L0 z	37.2	38.1	20.2	20.3	1.58	0.80	1.94	1.23	4.73	3.7	1.37	1.04	4.27	3.03	0.021
L1 phi	1.56	1.60	1.71	1.66	0.13	0.13	0.19	0.21	0.67	0.93	0.16	0.2	0.58	0.77	0.027
L1 z	0.74	0.76	0.80	0.79	0.08	0.086	0.20	0.23	0.69	0.98	0.18	0.22	0.61	0.80	0.020
L2 phi	0.78	0.81	0.94	0.82	0.079	0.086	0.135	0.13	0.51	0.66	0.12	0.14	0.43	0.56	0.021
L2 z	0.40	0.41	0.49	0.41	0.056	0.056	0.15	0.14	0.55	0.69	0.13	0.14	0.47	0.58	0.018
L3 phi	0.14	0.15	0.26	0.14	0.049	0.023	0.035	0.03	0.165	0.16	0.029	0.028	0.14	0.14	0.009
L3 z	0.13	0.14	0.24	0.11	0.055	0.023	0.057	0.05	0.255	0.25	0.048	0.046	0.21	0.22	0.009
L4 phi	0.022	0.027	0.031	0.023	0.013	0.006	0.0042	0.004	0.014	0.018	0.0035	0.003	0.012	0.016	0.002
L4 z	0.014	0.019	0.019	0.016	0.0081	0.005	0.0031	0.003	0.010	0.014	0.0026	0.003	0.0087	0.012	0.0017
L5 phi	0.012	0.016	0.015	0.014	0.0062	0.005	0.0020	0.002	0.0070	0.011	0.0015	0.002	0.0056	0.009	0.0017
L5 z	0.0082	0.011	0.010	0.010	0.0039	0.003	0.0015	0.002	0.0054	0.008	0.0012	0.002	0.0044	0.007	0.0012

- New rad Bhabha source doesn't affect rates in SVT but increases neutron fluence (+30%), already critical in external layers.
- All results for TDR studie still valid (stick with the old numbers in TDR) with the known weakness of S/N in L4-5 with x5 safety applied.

Layer0 Fanout and Peripheral electronics

M. Citterio(MI)



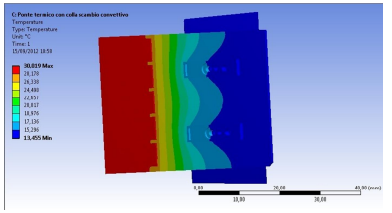
- Update on the production status for Layer0 pixel bus and Striplets fanout @ CERN
  - Very slow turn around time with CERN workshop.
  - Important to investigate again other possible supply!
- Update on the status of components order for peripheral electronics prototypes
- Mauro is very happy if SuperB goes to 40 MHz for the reference clock (possible use of GBT for our links become more realistic).
- First version of corresponding TDR sections promised in the next few days!

SVT Mechanics Update

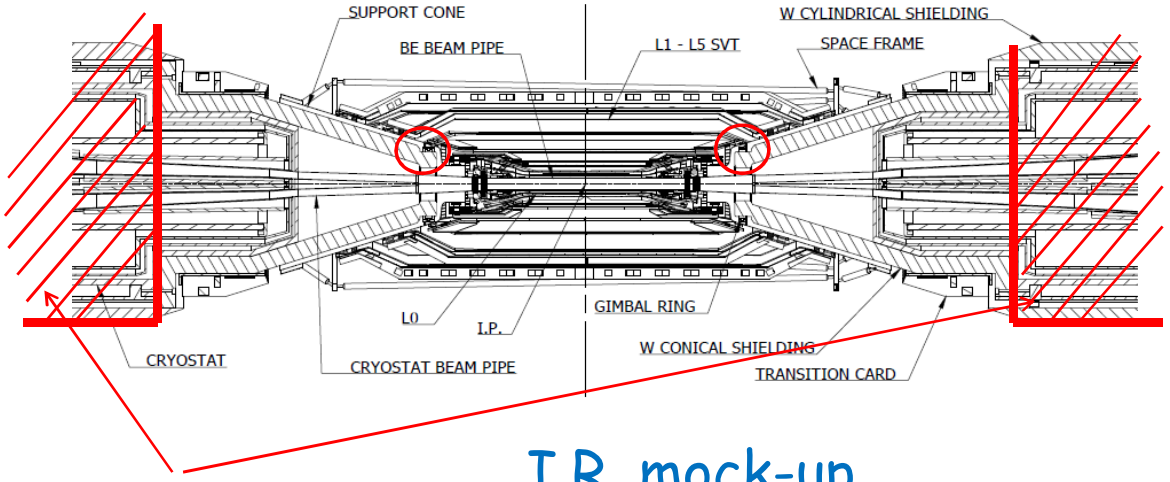
F. Bosi PI

1. TDR writing & prepare for module & beam pipe prototype construction.
2. Started to work actively on the problem of reducing the ambient temperature on sensor, to reduce the effect of leakage current increase (increased neutron fluence seen in background simulation in July)
   - thermal simulation of various components started
   - dry air pipes on the SVT support cones under evaluation

HDI Thermal Simulation

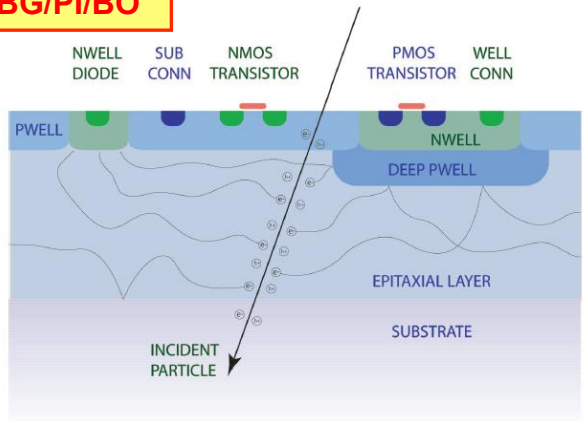


3. Plan to build a mock up of the SVT/IR to reproduce and measure the mech. stress and deformation induced on the SVT modules by the movement of the W conical shield due to movements/misalignment during installation (demounting) operation
   1. Pisa-QMUL-Milano for the different components of the SVT mechanics



R&D on pixel: APSEL MAPS

PV/BG/PI/BO



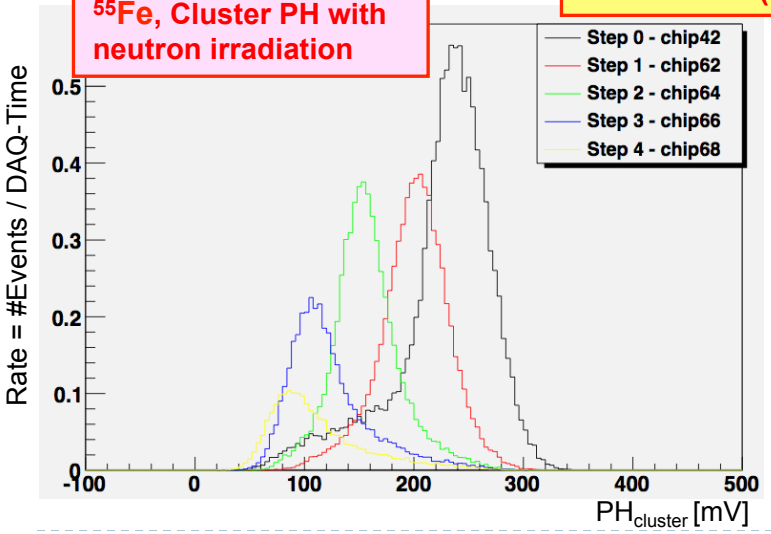
- INMAPS MAPS with high resistivity epi layer under test:
  - Better charge collection evident with high resistivity

- Irradiation with neutrons: 4 steps up to 1x10^14 n/cm2
- Chips tested in Pisa/PV (^{55}Fe, ^{90}Sr, Laser) → significant charge collection deterioration even at low fluence
- Other group observed better rad resistance (Strasbourg)
- Need to optimize the sensor design with the new process:
  - Collection diode dimension, diode bias voltage …

INMAPS CMOS process with 4 wells & high resistivity to improve charge collection efficiency and radiation resistance

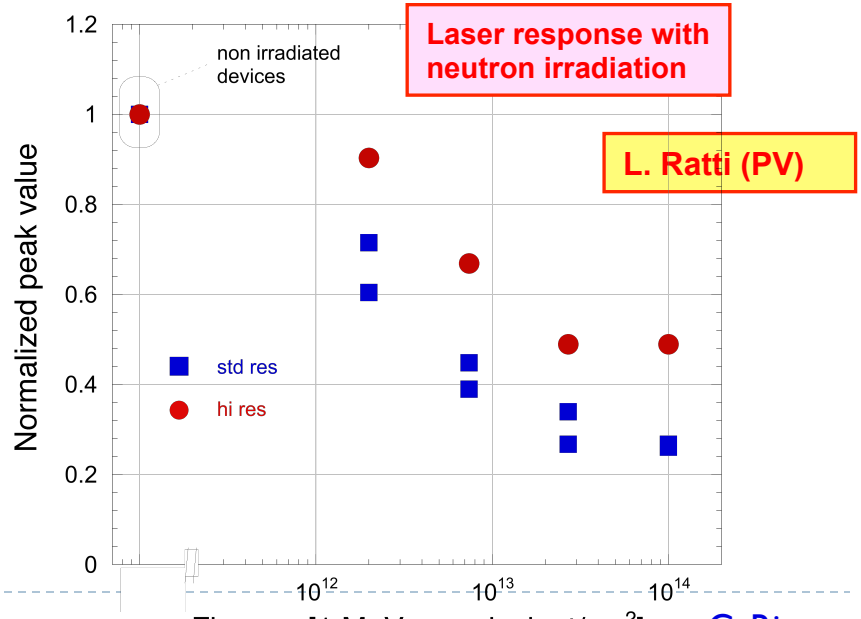
S. Bettarini (PI)

^{55}Fe, Cluster PH with neutron irradiation



Laser response with neutron irradiation

L. Ratti (PV)

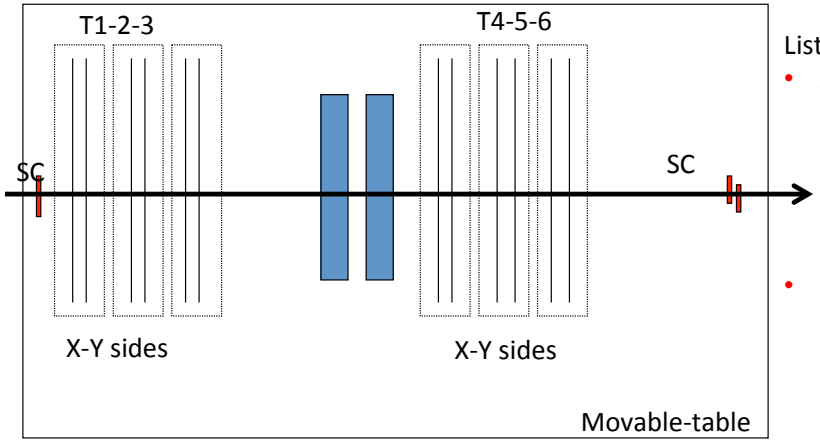


G. Rizzo

Testbeam Preparation

S. Bettarini (PI)

Test beam 2012: which DUTs?



List of possible DUTs

- Analog MAPS:
  - INMAPS(High-Ω and Low-Ω irr. and not irr.)
  - V.I. 3D MAPS?
- Digital MAPS:
  - INMAPS 32x32 (High-Ω and Low-Ω not irr.)
  - SuperPix0 Lower THR (peace-keeper
  - 3D-TC
  - DIASuperPix

- Getting ready for the Nov. 2012 Testbeam with many pixel devices
- Discussion on priority list since we have only 5 days of beam

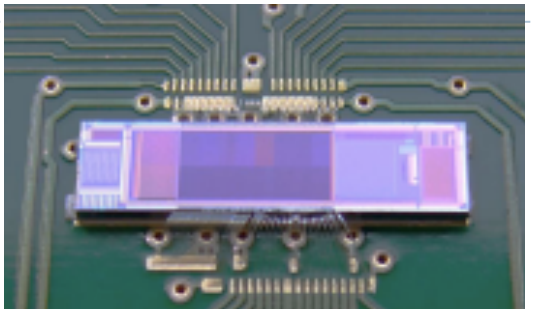
To be set a priority list!
(available only 5 days of beam)

Work in Lab. to be done

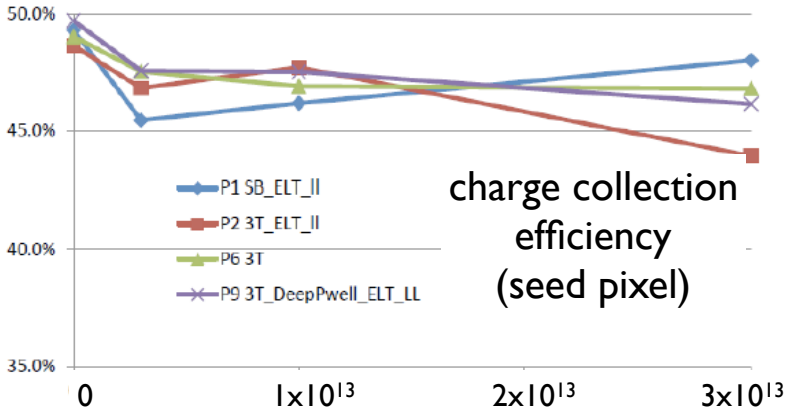
- Characterization: PISA
  - With TLA:
    - 3 chips INMAPS 32x32 high-Ω (Pi)
    - 3 chips 3D-TC (Pi)
    - 2 chips DIASuperpix0 (Pv/Lecce)
  - Superpix0:
    THR correction tests with chips TB2011 (Pi)
- DAQ(Bologna): Bologna
  - Writing the firmware for INMAPS 32x32 (debug possible:apsel4D board + inmaps chip)
  - IDEM for chip 3D-TC
  - Understand if the peace-keeper can work with lower THRs w.r.t. TB 2011

R&D on pixel in Strasbourg

I. Ripp-Baudot (IPHC Strasbourg)



- Encouraging results on irradiation test with neutrons with MIMOSA 32 MAPS:
  - 180 nm quadruple well CMOS process, high res, rolling shutter (time frame ~ 30 µs)



- The "Italian" MAPS pixels have already the right architecture for Layer0 (in pixel sparsification & small timestamp 100 ns), but need to optimize the sensor design to benefit of the improved radiation resistance of the new process….
- MIMOSA pixels have a better charge collection but still need to work on the evolution of their architecture to get the right specs for SuperB/ALICE:
  - Detailed plan

next steps

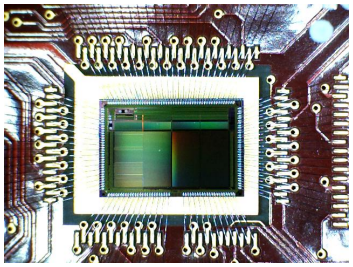
"towards a rad-hard sensor with a read-out time ~ 1.5 µs"

- MIMOSA-32: validation of the 0.18 µm technology.
  - Complete the data analysis of past beam tests (June, July and August): spatial resolution, ...
  - Next beam test foreseen in November at CERN: other radiation doses, ...
  - New submission of MIMOSA-32 in 0.18 µm in July: test of amplification.
- MIMOSA-22THR: validation of the optimised rolling shutter architecture.
  - Submission December 2012.
  - 2 different chips:
    - translation of MIMOSA-22AHR (0.35 µm techno.) with end-of-column discrimination.
    - simultaneous 2-row encoding with 2 discriminators/column ➛ twice faster.
- SUZE-02: validation of the sparsification.
  - Submission Autumn 2012.
  - Sparsification for 2 and 4 // rows ➛ data flow and power reduction.
- AROM-1 (Accelerated Read-Out Mimosa): validation of the in-pixel discrimination.
  - Submission 2013.
  - Simultaneous 4-row encoding with in-pixel discrimination ➛ 8 times faster.

- Very useful exchange of information on the technology among groups

Update of Activities in UK

A. Bevan (QMUL)



Queen Mary University of London

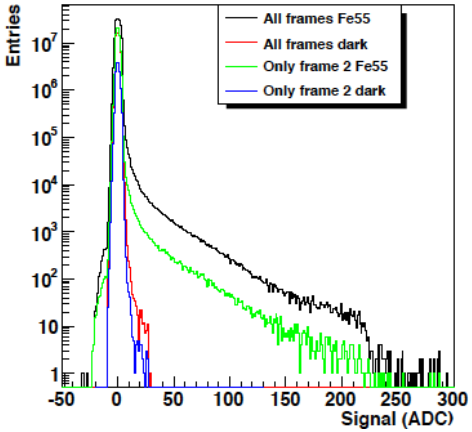
Particle Physics Rutherford Appleton Laboratory

Progress of the Arachnid Collaboration

- MAPS R&D with INMAPS process (pioneered by RAL) the with target application ALICE/ SuperB
- characterization of their INMAPS chip Cherwell (ENC~ 12e-) & preparation for testbeam in November

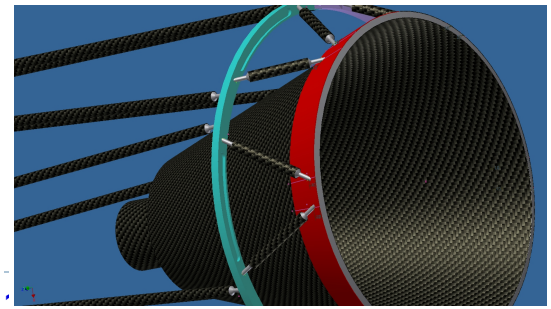
Reference pixel results

- There is a clear noise peak
- Fe55 spectrum shows a sharp cut-off at ~275(ADC counts)
- Consistent with noise and gain from PTC



Mechanics:

- Getting ready to build prototypes of support cones & space frame to be integrated with the mockup of the SVT & IR we plan to build in Italy in the next 12-18 months to test the stability of the SVT assembly and quick demounting procedure



SVT – TDR STATUS

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Almost Completed

Completed

V0 in few days

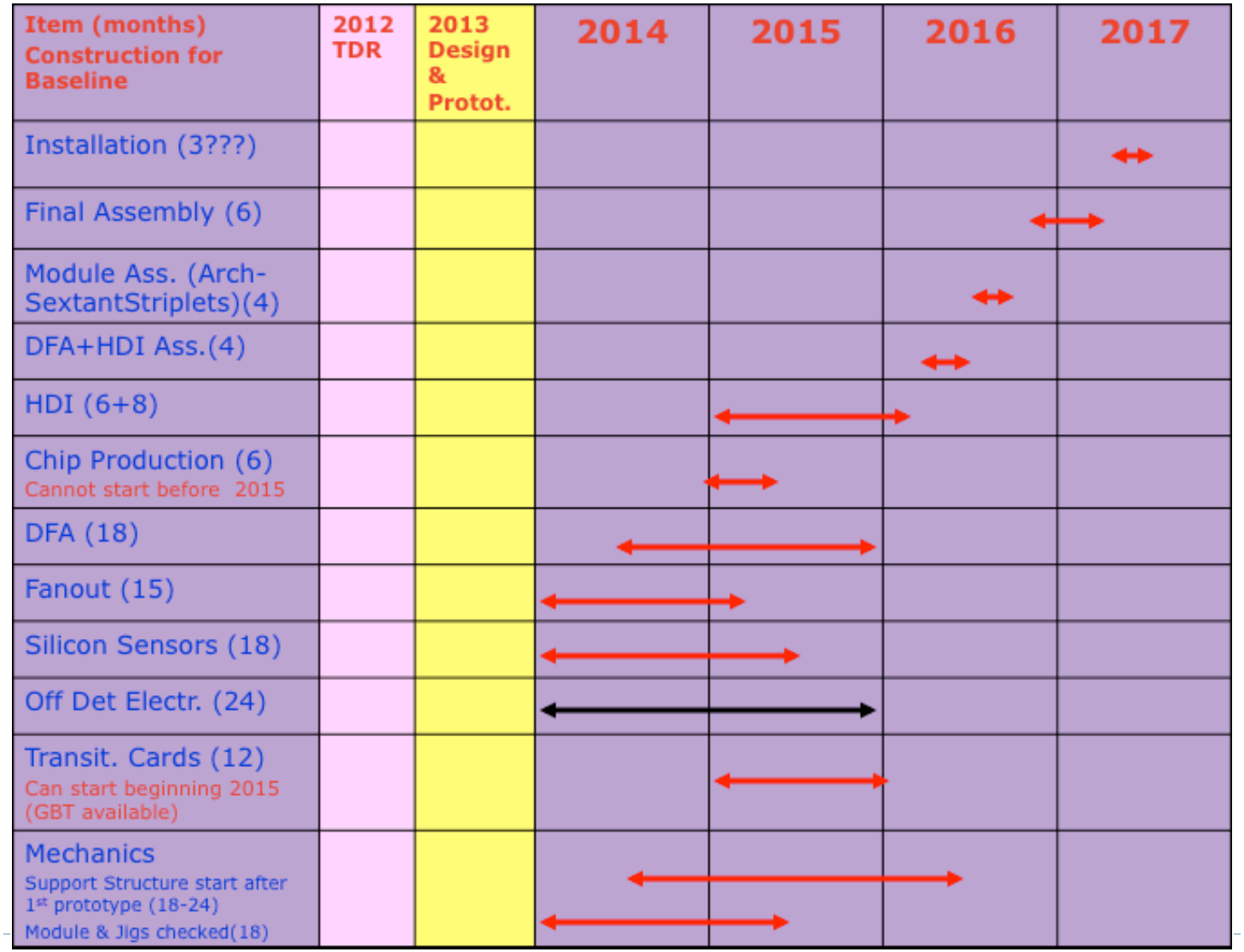
SVT – TDR final phase

- Internal revision of the text started on completed sections (~ 75%)
  - Mechanics/Silicon sensor chapters almost complete
  - Peripheral electronics & fanout layer0 first version promised in a few days
  - Background chapter still to be written (only 2-3 pages + table)
- Final "chapter reader" for SVT (A. Bevan) can hopefully start to work in 1-2 weeks.
- Need to include budget and schedule for SVT construction.
- Budget used for white paper should be revised
  - Need to include costing for quick demounting
  - Refine manpower/cost for technicians and eng. for construction (seems underestimated for some phases)
- Preliminary schedule built looking at BaBar experience (assuming right manpower available) + some guess on Layer0 needs and relaxing the final phase of construction w.r.t BaBar.
  - First draft of the schedule revised during the parallel sessions

Assumption for schedule

- Assumed enough manpower available and 2 main labs (as in BaBar):
  - Pisa+UCSB for modules
  - LBL+(Pisa) SVT Mechanics
  - Pisa+Trieste Silicon sensors
  - Pisa+Torino+Ferrara Jigs
  - LBL+PV+MI On detector electronics
  - UCSC Off Det. Electronics

Preliminary SVT – Construction schedule



Backup

Using BaBar SVT Construction Experience + Layer0 needs + more relaxed final phase

	BABAR Experience		comments	SuperB	end date	comments
	months	date		months		
Si sensor design	12	95		12		
Si sensor production test	18	mid 96- end 97		18		
DFA	12-18 months	beg full speed july 97 end 98		18		also L0
chips available		mid 98			mid 2015	prototyping ends in 2 yrs from now. + 6 months production
HDI loading	4	aug 98-nov 98	too hard in 4 months	12 m with 6m chips loading starting when chips avaliable	end 2015	include L0
DFA+HDI L1-2-3	3	sept - nov 98	in UCSB	module assembly in 2 places 3 month for DFA+HDI + 3 months for Module assembly 6 months total	Mar-16	
DFA+HDI L4-5	3	oct-dic 98	in PISA at the same time DFA_HDI bonding/testing and Arch construction (2 teams too hard!!)	module assembly in 2 places 3 month for DFA+HDI + 3 months for Module assembly 6 months total	Mar-16	
Module 1-2-3	2	oc-nov 98	in UCSB	module assembly in 2 places 3 month for DFA+HDI + 3 months for Module assembly 6 months total	mid 2016	
Arch 4-5	3	nov98 jan99	in PISA at the same time DFA_HDI bonding/testing and Arch construction (2 teams too hard!!)	module assembly in 2 places 3 month for DFA+HDI + 3 months for Module assembly 6 months total	mid 2016	
installation on support cones	3	jan-march 99		6 months considering L0 too	end 2016	
installation of SVT	3	march-june 99		3	Mar-17	

UPDATED looking more carefully at BaBar schedule and including Layer0 (OLD)

Item (months) Construction for Baseline (striplets +SVT)	2012 TDR	2013 Design & Protot.	2014	2015	2016	2017 Commissioning in SuperB
Installation (3)						
Final Assembly (6)						
Module Ass. (Arch-SextantStriplets)(3)						
DFA+HDI Ass.(3)						
HDI (12)						
Chip Production (6) Cannot start before 2015						
DFA (18)						
Fanout (15)						
Silicon Sensors (18)						
Off Det Electr. (24)						
Transit. Cards (15)						
Mechanics Support Structure (18-24) Module & Jigs (18)						