MAROC, PARISROC, SPIROC: Latest generation of ASICs for photodetectors readout

12th Pisa Meeting on Advanced Detectors

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Orsay MicroElectronics Group Associated

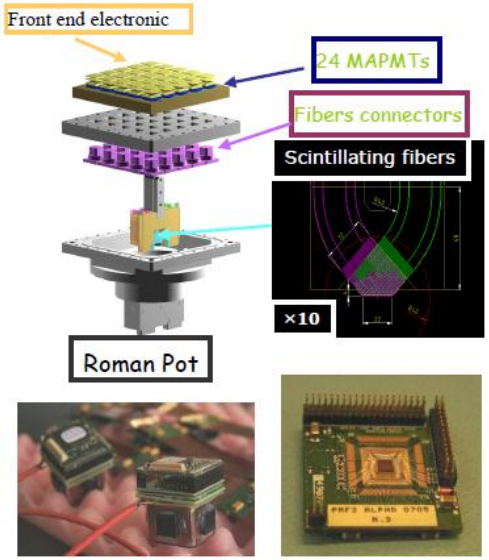
Outline

The OMEGA group (10 designers) has designed a new generation of ASICs, the "ROC" family in AMS (AustriamMicroSystem) SiGe 0.35 µm technology to read out signals from various families of photo-detectors

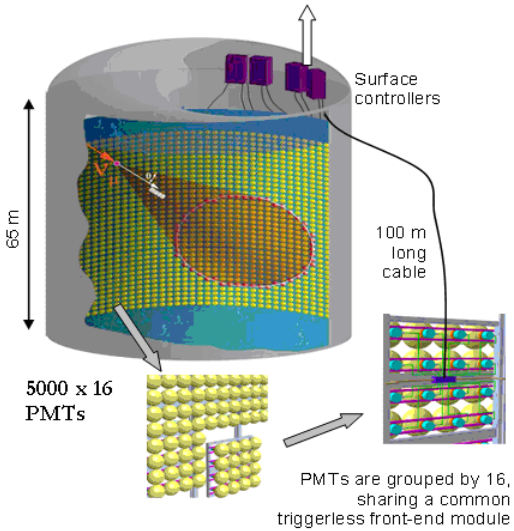
1. **MAROC3** (Multi Anode ReadOut Chip ***/SPACIROC/HARDROC/MICROROC***) a 64 channels chip to read out Multi Anode Photomultipliers (MAPMT)

2. **PARISROC2** (Photomultiplier ARray In SiGe ReadOut Chip) a 16 channel chip to read out array of Photomultipliers (PMT)

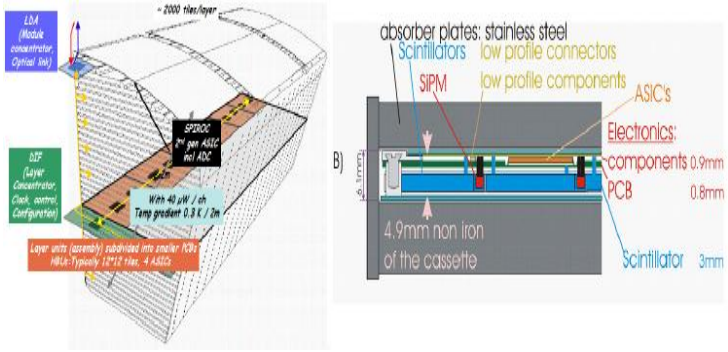
3. **SPIROC2** (SiPM Integrated ReadOut Chip) ***/EASIROC*** a 36 channel chip for Silicon PhotoMultiplier (SiPM) readout.



MAROC:
ATLAS luminometer Roman Pot



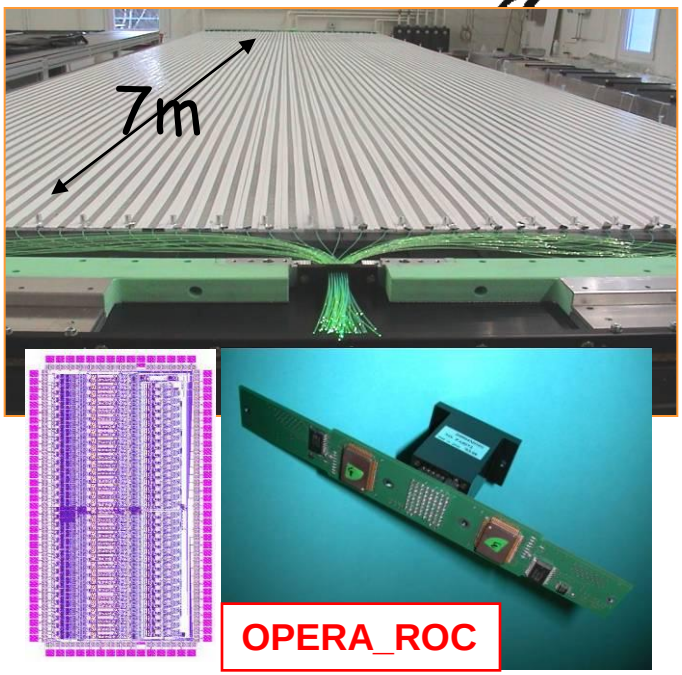
PARISROC:
PMm2 project

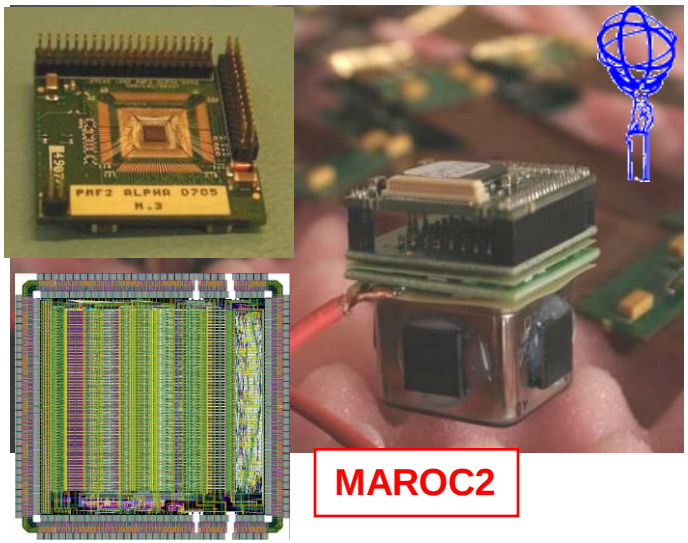


SPIROC:
ILC, Analog Hadronic Calorimeter prototype

MAROC for MAPMT

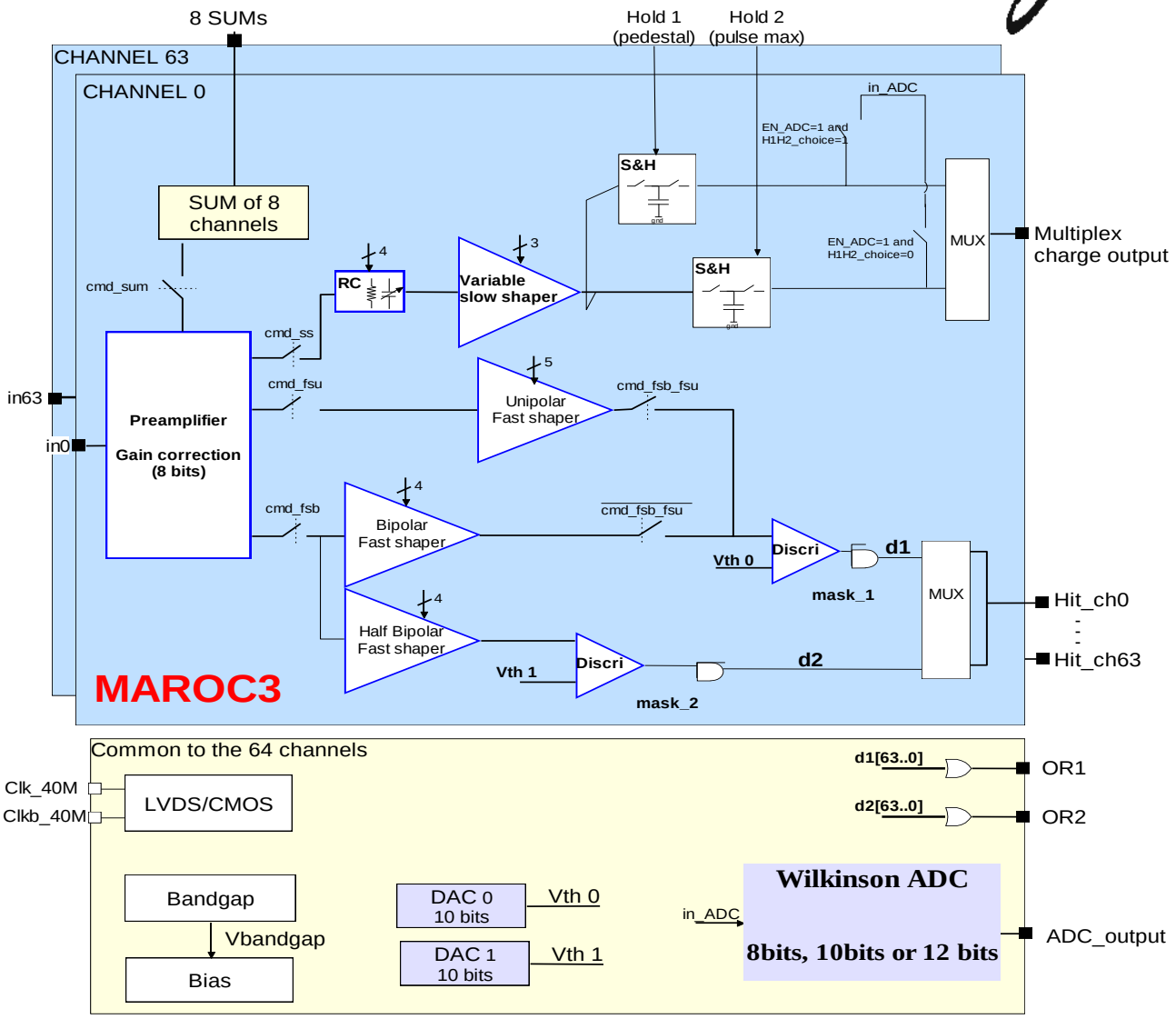
- Started with OPERA_ROC (2001)
  - 32 Channels in BiCMOS 0.8 µm
  - 3000 chips produced in 2002
  - Readout OPERA Target tracker in Gran Sasso
- MAROC1 (2004)
  - First prototype with 64 channels
  - AMS SiGe 0.35 µm (12 mm^2, Pw=5 mW/ch)
- MAROC2 (2006)
  - **1000 chips produced and bonded on a compact PCB for ATLAS luminometer (ALFA)**
- MAROC3 (2009)
  - Lower power dissipation
  - Wilkinson ADC added
  - 1000 chips produced in 2010
- Many applications: Double-Chooz, Menphyno, medical imaging(Valencia, ISS Roma)…





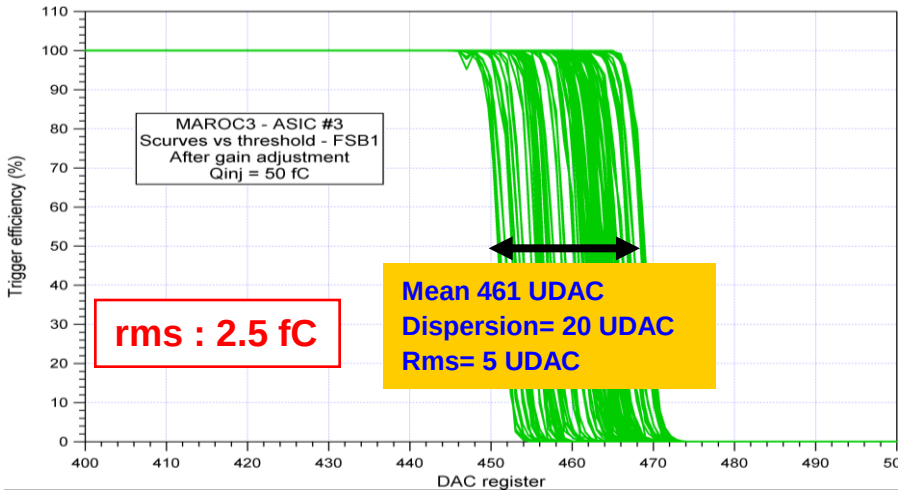
MAROC3 general architecture

- 64 channel inputs
- Low input impedance (50-100 Ω)
- Variable gain preamps (8 bits/ch.)
- Variable slow shaper (20-100 ns)
- 2 T&H (baseline and max.)
- 1 mux. analog charge output
- 1 digitized charge output (8, 10 or 12 bits ADC)
- 64 trigger outputs
- 2 OR outputs
- 10 bits DAC as threshold
- Internal bandgap for voltage references
- Pw = 3 mW/ch
- 828 slow control parameters

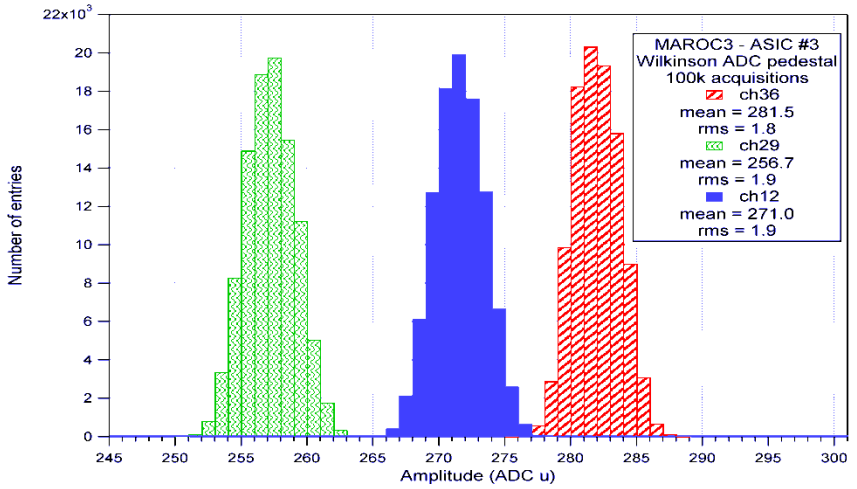


MAROC3: Scurves with FSB

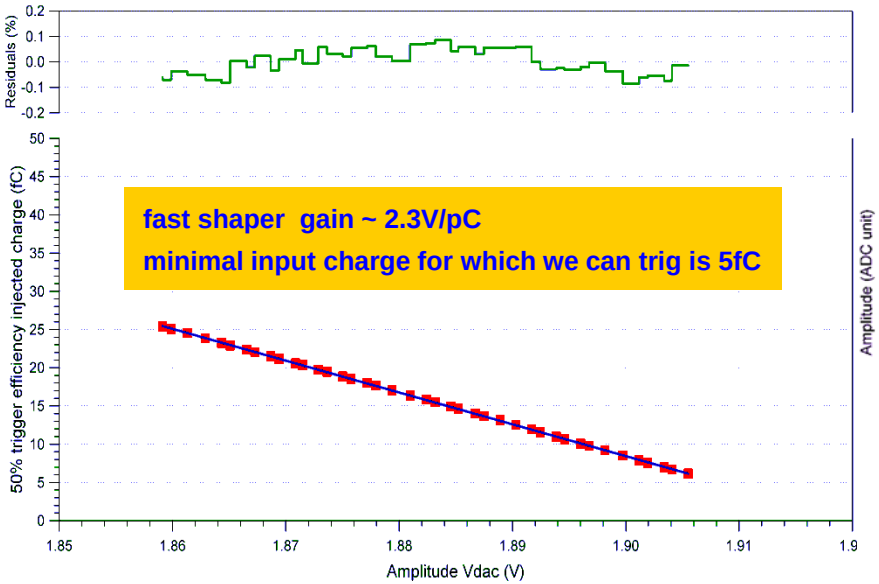
Trigger efficiency of the 64 channels as a function of the DAC value for 50fC injected charge and adjustment preamplifier gain



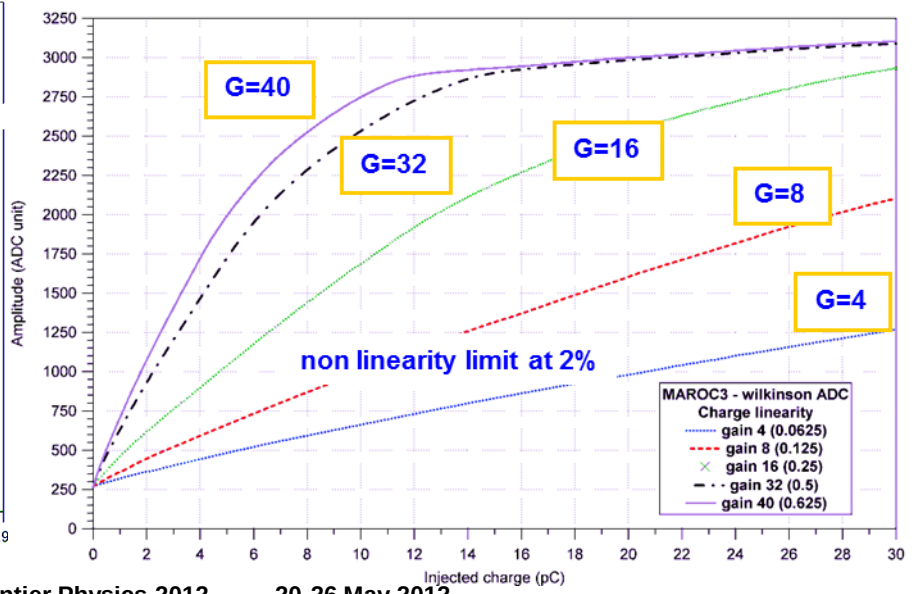
Histogram of pedestals for 3 channels



50% trigger efficiency as function of the threshold



Charge linearity for different preamplifier gain via 12-bit ADC



Variant: SPACIROC

JEM EUSO experiment

Analog Front End similar to MAROC

64 channels

Photoelectron counting (<50MHz)

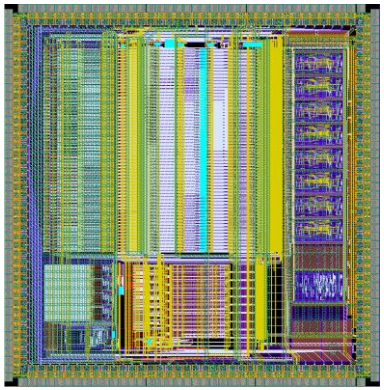
Time Over Threshold
(collab.JAXA/Riken/Konan University)

Digital part :Digitization,memorization

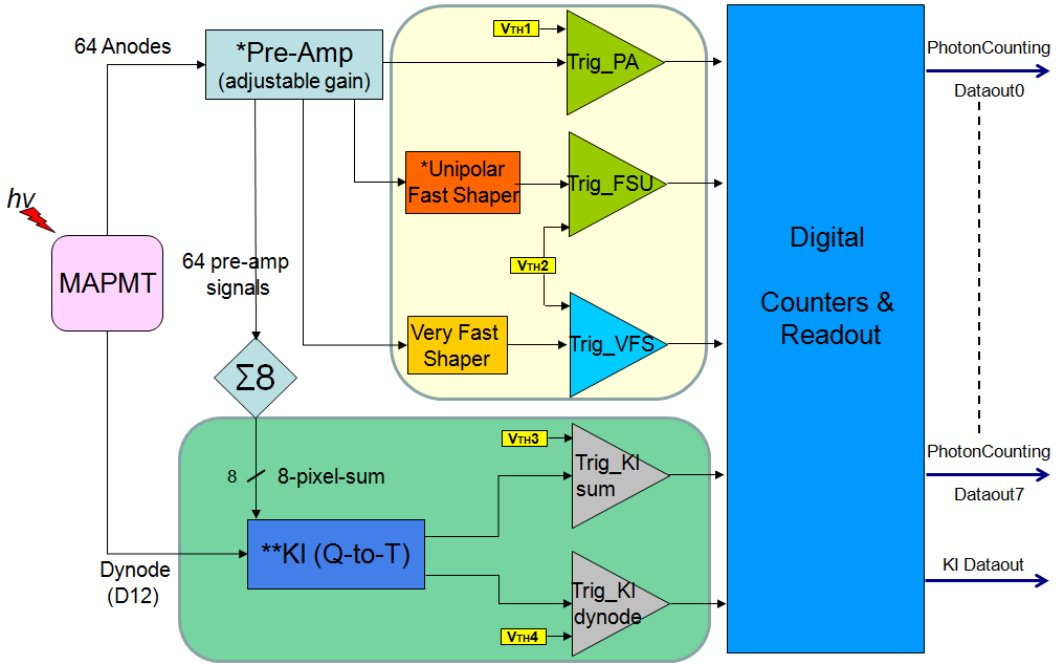
Power consumption < 1 mW/ch

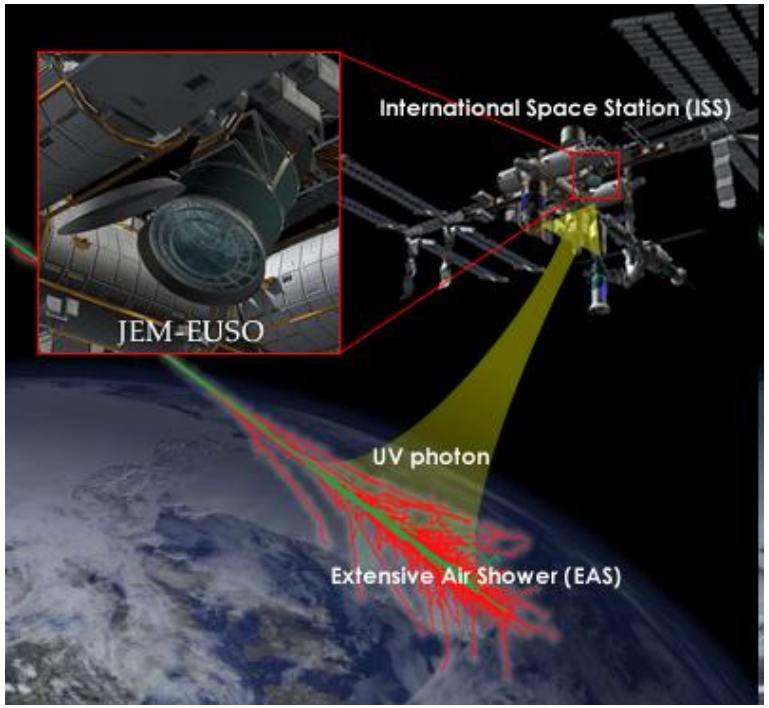
data flow ~ 384 bits / 2.5 µs

Radiation tolerance : triple voting



SPACIROC : 16mm^2





Variant: HARDROC

RPC detector (SDHCAL-ILC)

Analog Front End similar to MAROC

64 channels

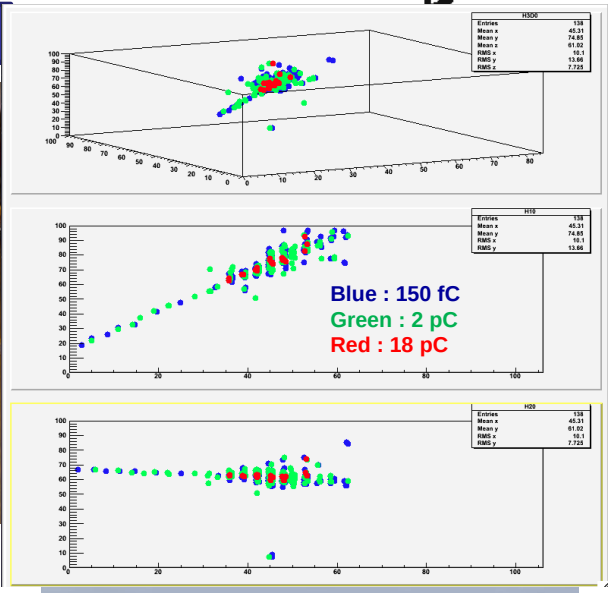
Auto trigger on 10fC up to 20 pC

5 0.5 Kbytes memories to store 127 events

Full power pulsing => 7.5 µW/ch

SDHCAL technological proto with 40 layers (**5760 HR2 chips**) built in 2010-2011. and under tesbeam at CERN May 2012

@IPN Lyon



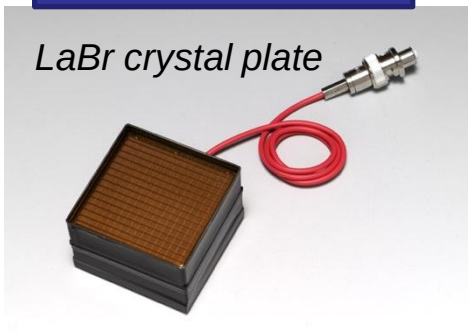
Medical applications (IMNC):

TRECAM (Tumor Resection CAMera): miniaturized gamma-camera for breast cancer surgery

Industrial transfer

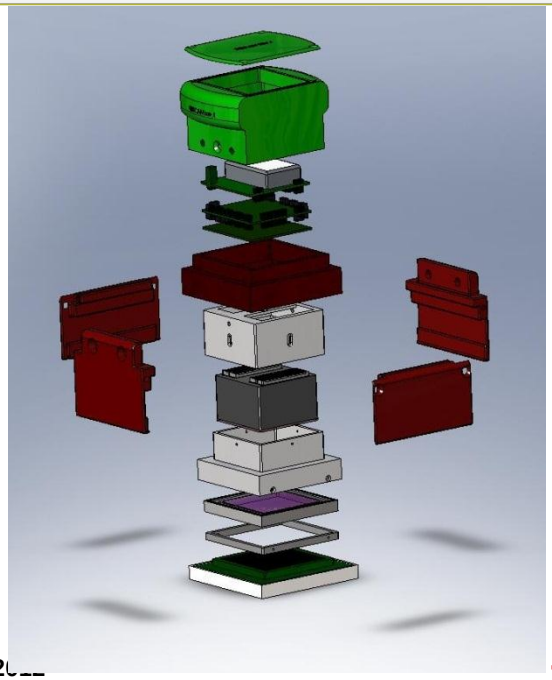
256 channels flat Panel MC-PMT 4x64 channels HARDROC2

@IMNC ORSAY



Field of view : 50 x 50 mm²

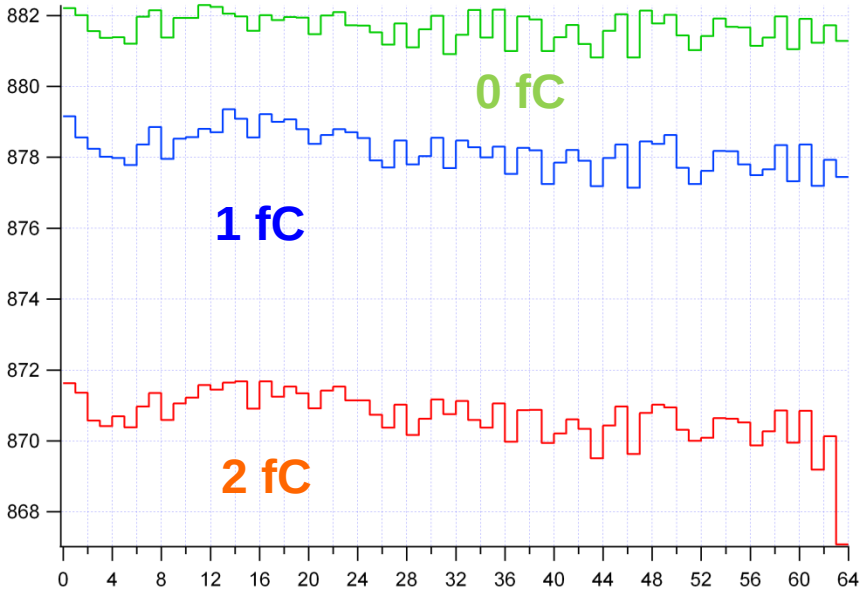
Weight : around 1 kg



Variant: MICROROC

MICROROC: 64 channels for µMegas (DHCAL ILC)

- ❑ Very similar to HARDROC except for the input preamp (collaboration with LAPP Annecy) and shapers (100-150 ns)
- ❑ Noise: **0.2fC Cd=80 pF => Auto trigger on 1fC** up to 500fC
- ❑ Pulsed power: **10 µW/ch** (0.5 % duty cycle)
- ❑ **HV sparks protection**
- ❑ 1 m2 in TB in August and October 2011. Very good performance of the electronics and detector (Threshold set to 1fC).
- ❑ 2012: 4 m2 in TB

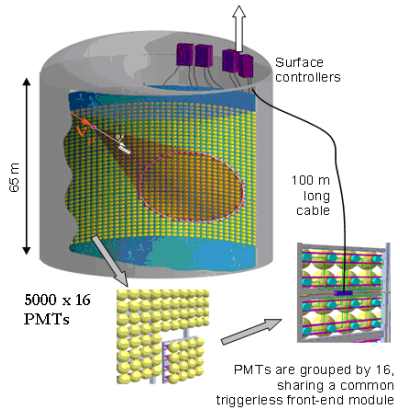


@LAPP Annecy

1m2 equipped with 144 MICROROC

PARISROC for large PMTs

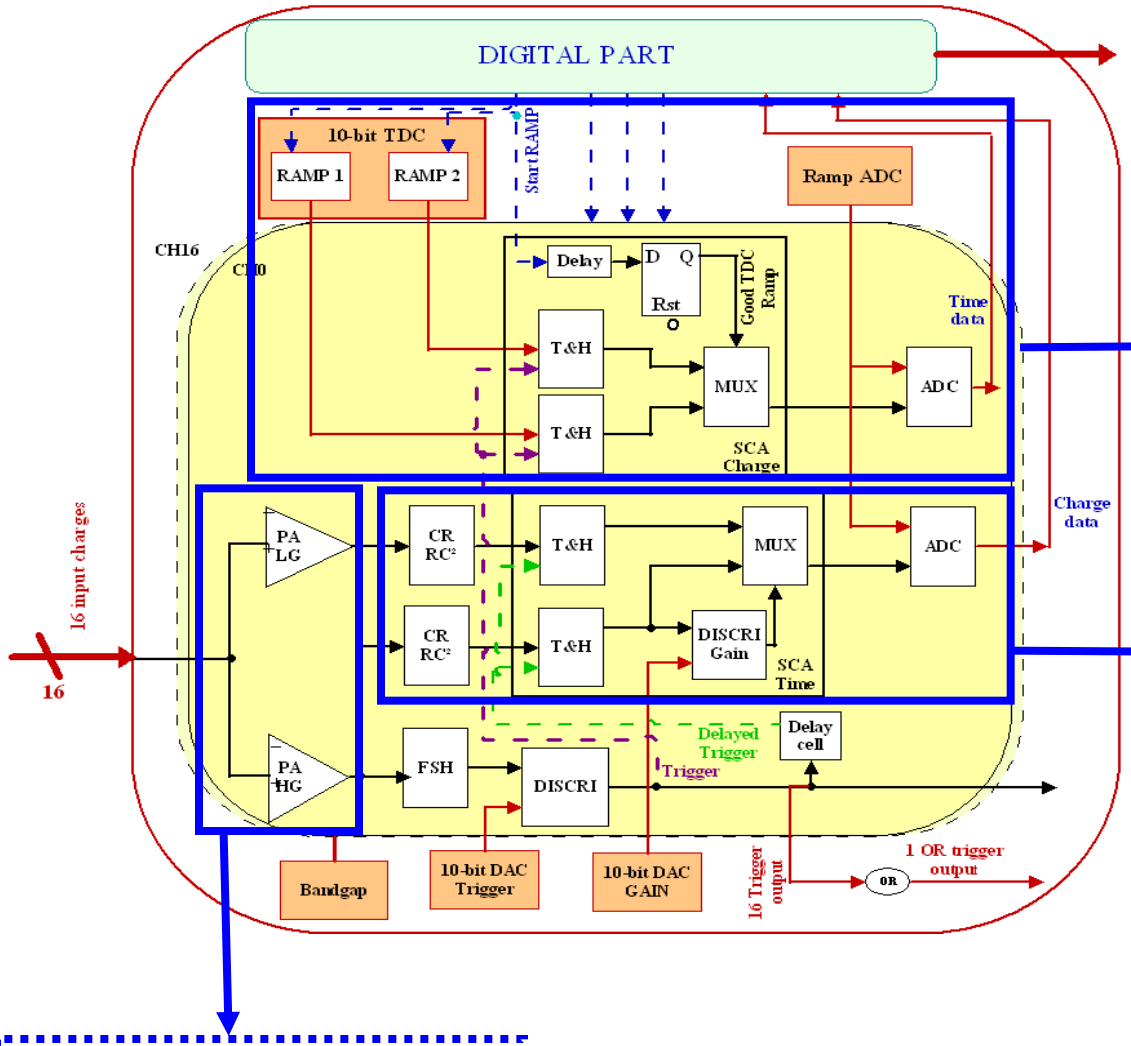
- Photomultiplier Array Integrated in SiGe Read-Out Chip
  - Replace large PMTs (20'') by arrays of 16 smaller ones (12'') , PMm2 project
  - **Smart photodetector**
  - 16 **independent** channels
  - Auto-trigger at 1/3 p.e.
  - Charge (300 pe) and time (1ns) measurement (10-12 bits)
  - Water tight, common high voltage for PMTs
  - Data driven : « One wire out » for DATA and power supplies



- First prototype in 2008
- Second prototype in 2010 (to improve the performances)
- Main applications in large Water Cerenkov
  - **Chip studied by LAGUNA (MENPHYS), LHAASO…**

Demonstrator realized by the IPNO with 16 x 8-inch Hamamatsu tubes

PARISROC: System On Chip



Time measurements

2 systems:

1. Coarse time by 24-bit gray counter (Digital part)
   - working at 10 MHz
   - with 1.67 s of dynamic
   - 100 ns steps
2. Fine time by analog TDC
   - ✓ 100 ns dynamic range
   - ✓ Time resolution: 220 ps
   - ✓ Non linearity: +/- 1ns

Charge measurements

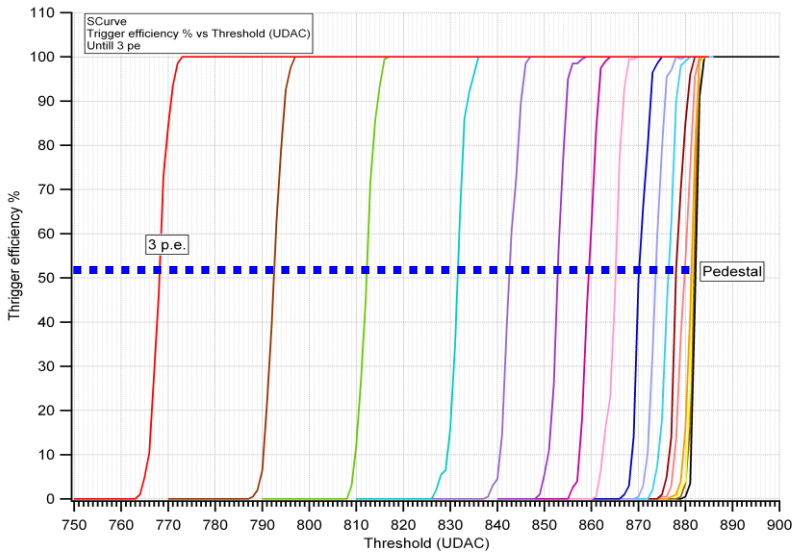
- ✓ Two gain channels to cover the large input dynamic range
- ✓ 2 input preamplifier with adjustable gains (on 8 bits)
- ✓ Shaper with variable shaping time (form 25 ns to 100 ns) and gain
- ✓ Charge resolution: max 0.2 p.e. (32 fC) for 10-bit ADC
- ✓ Dynamic range from 1/3 pe to 600 pe (~ from 50 fC to 100 pC)

Input stage

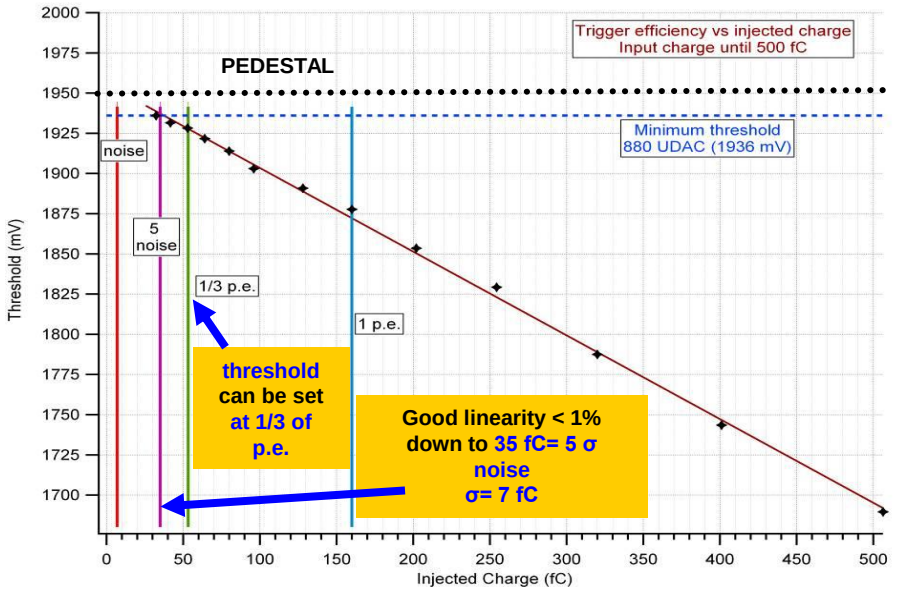
2 input preamplifiers with adjustable gains (on 8 bits)

PARISROC: Trigger efficiency and Auto gain with ADC

Trigger efficiency of one channel as a function of the injected charge at different threshold value

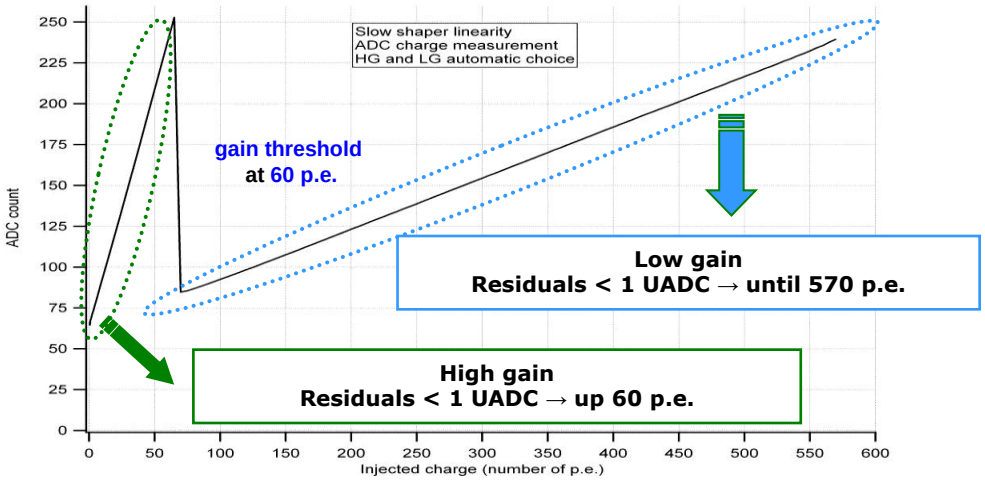


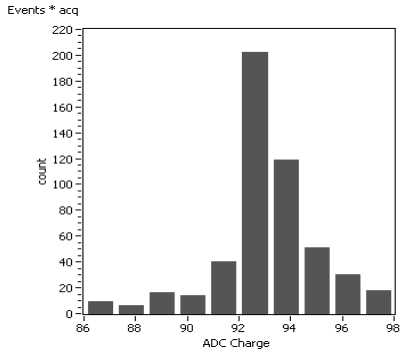
50% Trigger efficiency as a function of the injected charge



The whole chain is tested injecting a charge in the input of the channel: the signal is amplified, auto-triggered, held in the SCA cell and converted by 10-bit ADC

Auto-gain test (Charge measurements)

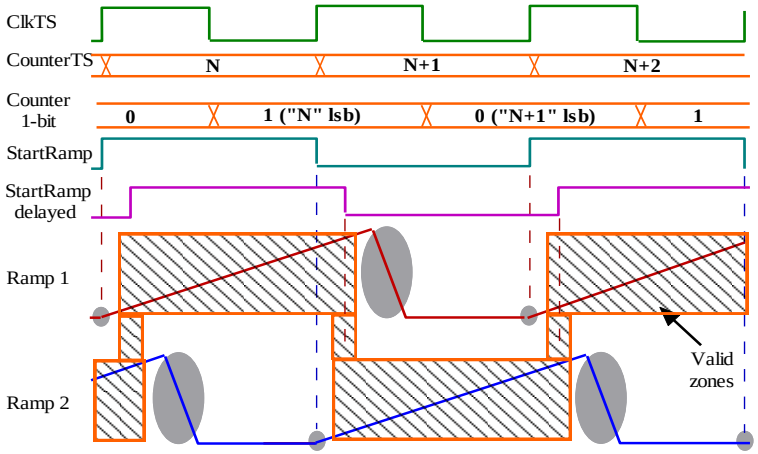


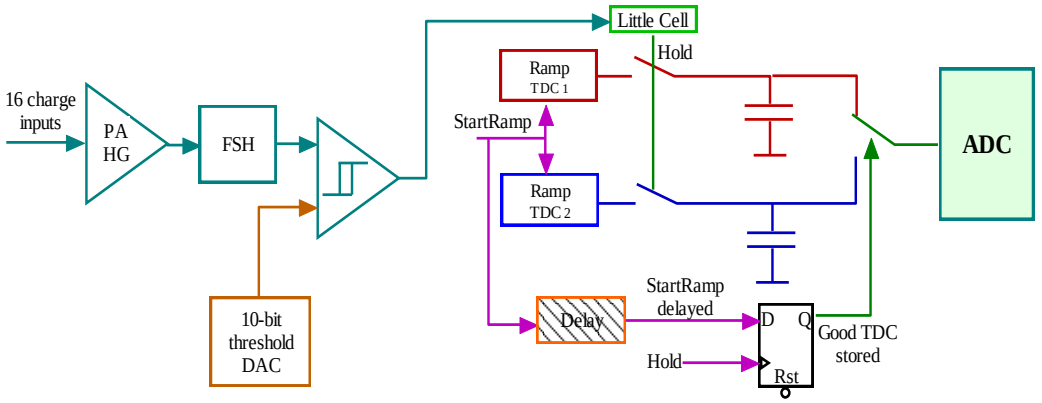


1 pe charge measurement by 10-bit ADC.
Average= 93.02 UADC,
sigma= 2.02 UADC,
range= 12UADC.

PARISROC: TDC ramps

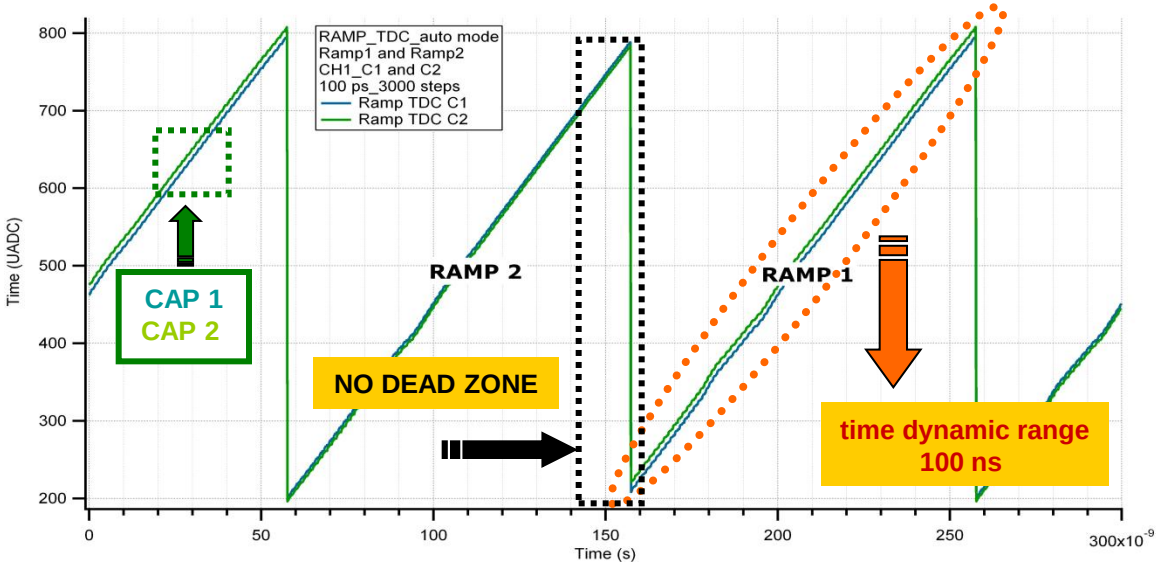
The TDC ramp has been reconstructed from the time values saved in the analog memory and converted by the ADC (10-bit).
The validation of the good ramp is made automatically





Time dynamic range	100 ns
"Blind zone"	0
linear zone	100 ns
Ramp 1 linear	± 1 ns
Ramp 2 linear	± 1 ns

Time overall measurements

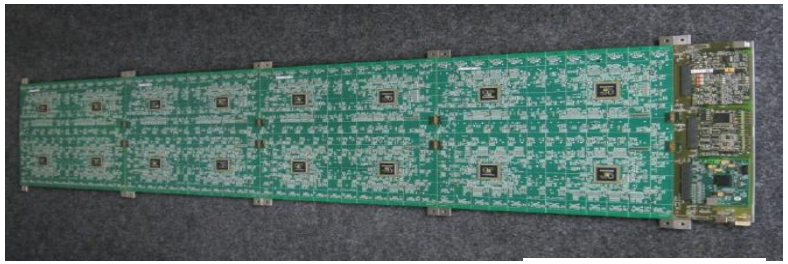


SPIROC for SiPM

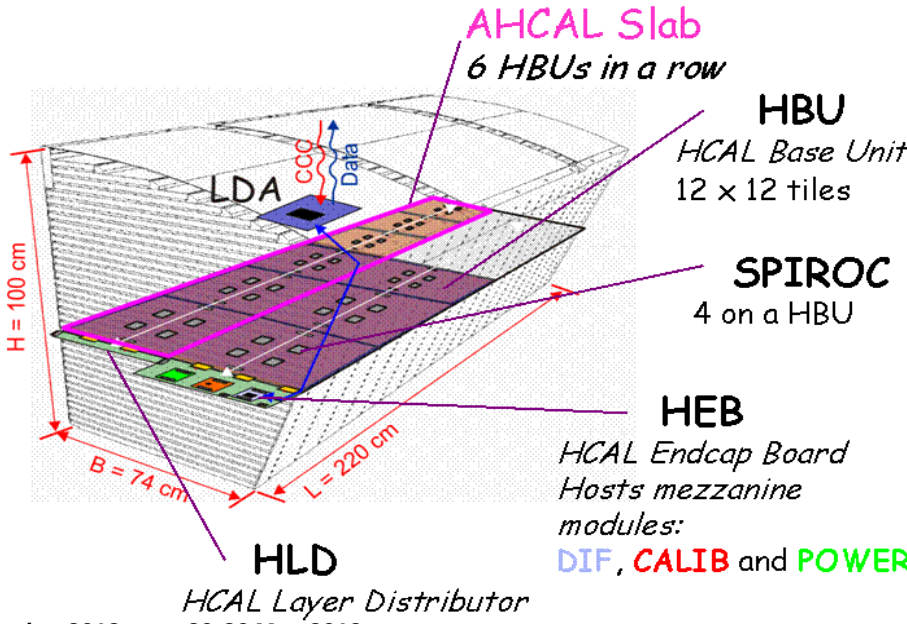
- SPIROC : Silicon Photomultiplier Integrated Readout Chip to read out the analog hadronic calorimeter for CALICE (ILC)
- Large detector with 8 millions channels= >Chip embedded in detector :
- **36-Channel ASIC**
- **Internal input 8-bit DAC** (0-5V) for individual SiPM gain adjustment
- **Energy measurement : 14 bits, 1 pe to 2000 pe**
  - pe/noise ratio : ~11
- **Auto-trigger on MIP or on single photo-electron**
  - Auto-Trigger on 1/3 pe (50fC)
- **Time measurement :**
  - 12-bit Bunch Crossing ID (coarse time)
  - 12-bit step~1 ns TDC->TAC (fine time)
  - Analog memory for time and charge measurement : depth = 16
  - Low consumption : ~25 µW per channel (in power pulsing mode)
  - 4kbytes internal memory and daisy chain readout

4 **new HBUs** in DESY lab

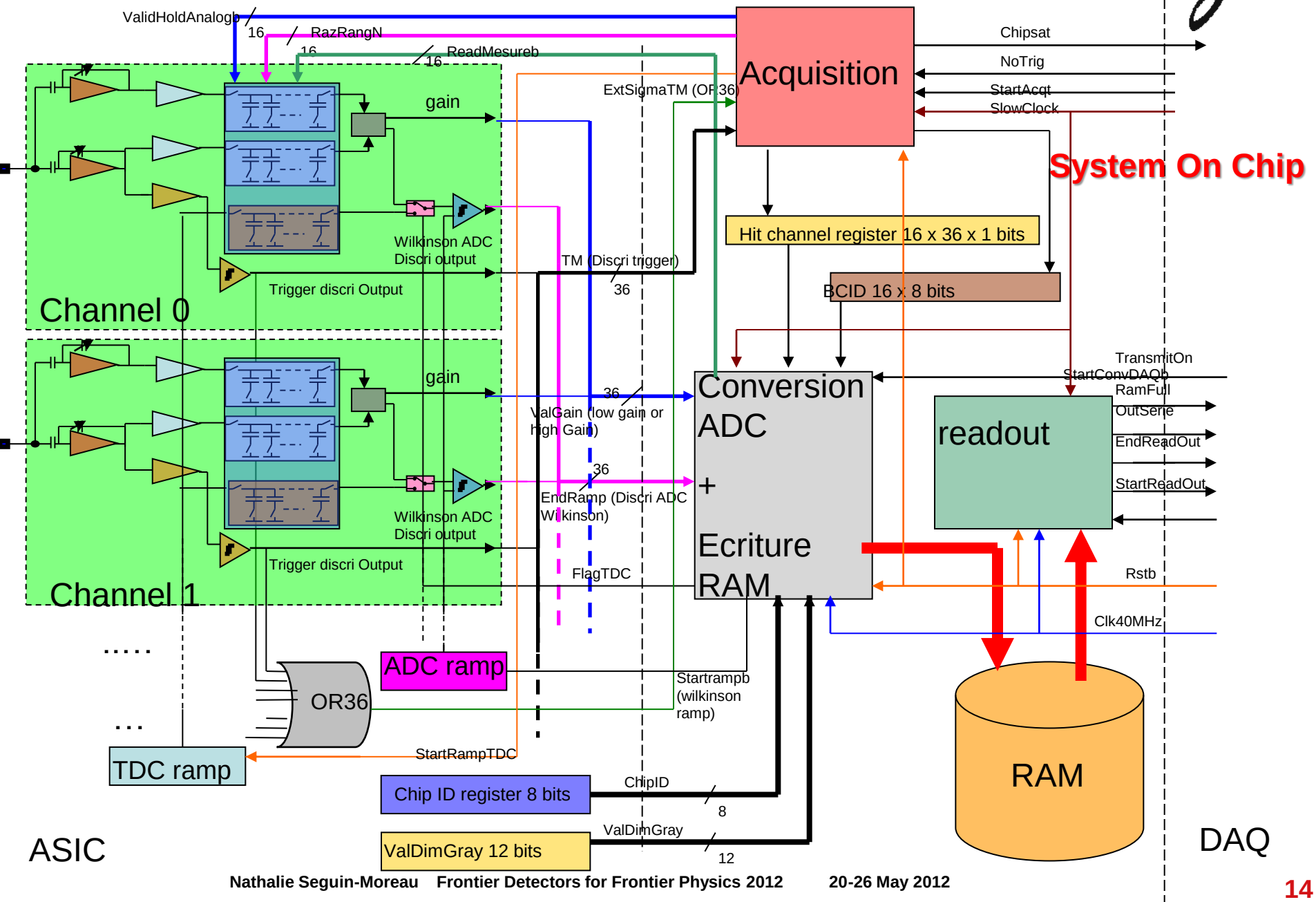
→ 70 channels equipped with scintillator tiles, LEDs, SiPM readout, 4 ASICs



(0.36m)² Tiles + SiPM + SPIROC (144ch)

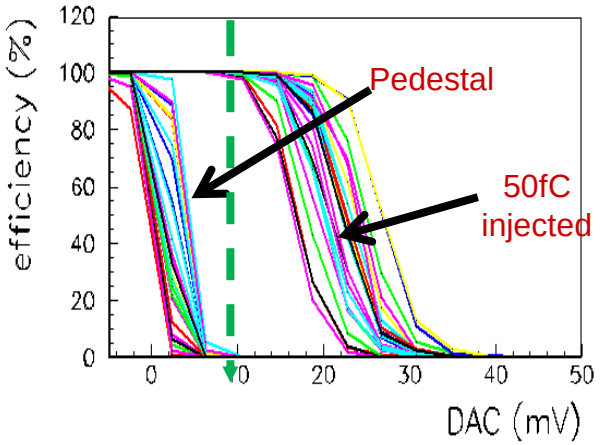


SPIROC : System On Chip

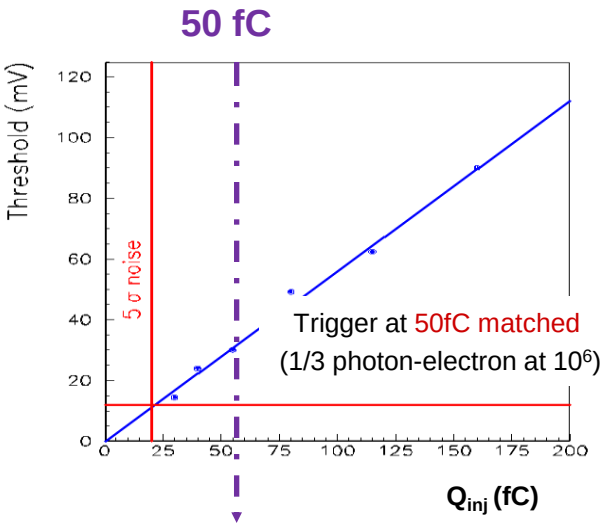


SPIROC: trigger efficiency measurements

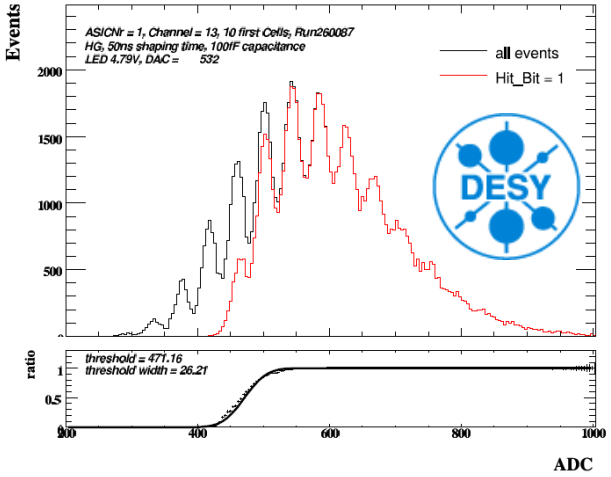
36-channel S-curves: trigger efficiency versus threshold (1 LSB = 2 mV)



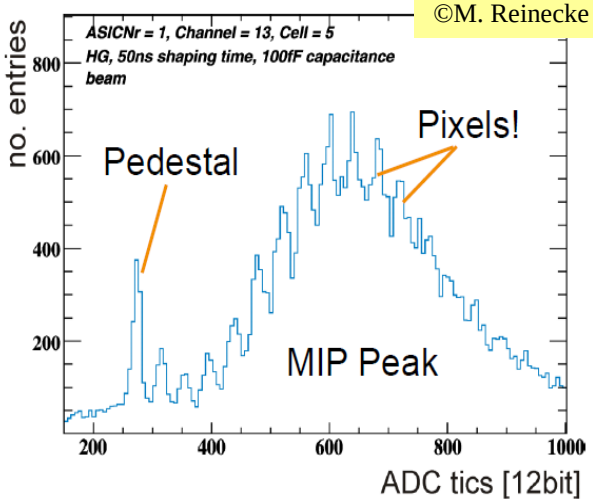
50 % Trigger efficiency point vs Q_{inj}



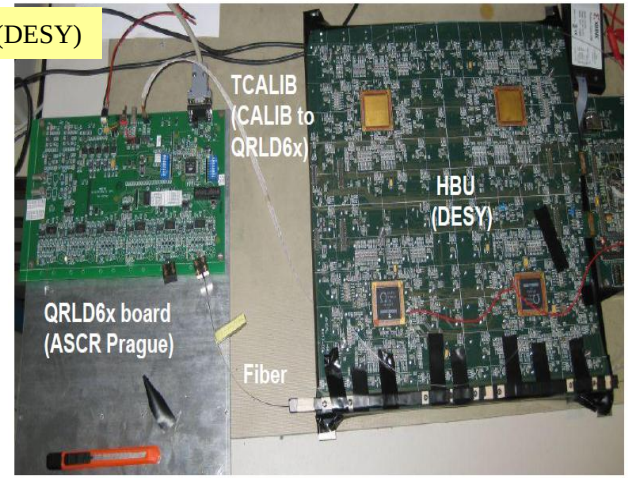
SiPM SPECTRUM with Autotrigger



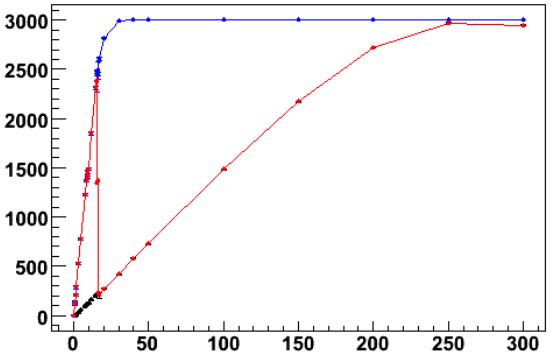
MIP response in DESY 6 GeV electron testbeam



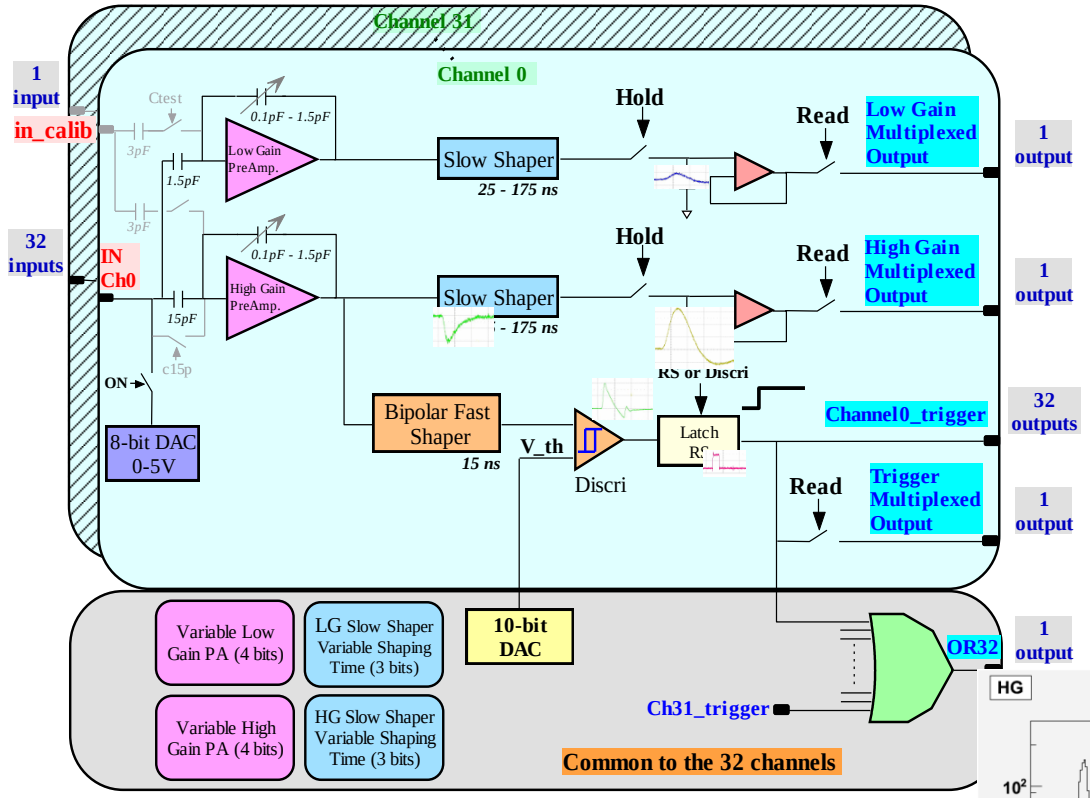
©M. Reinecke (DESY)



linearity using the auto gain mode and internal ADC

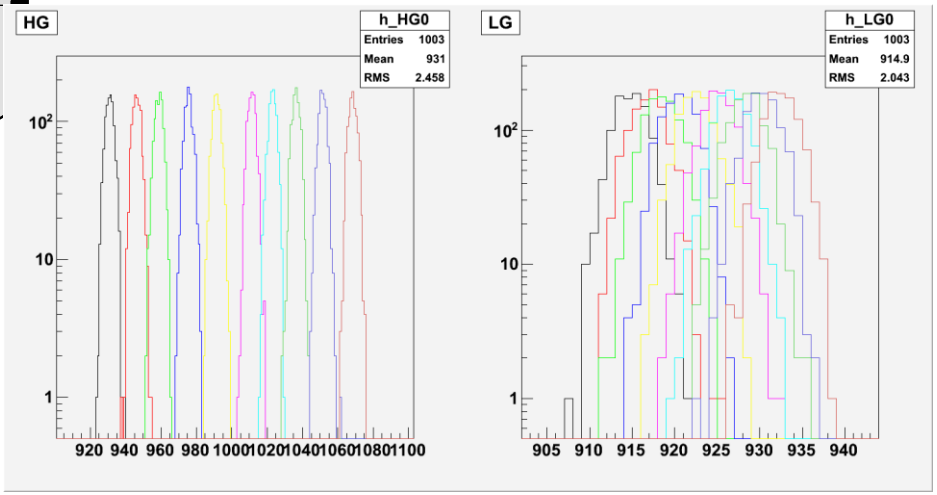


EASIROC: SIMPLER VERSION OF SPIROC CHIP



- 32-channel front-end readout (analogue part of SPIROC)
  - 2 multiplexed analog outputs (high gain, low gain) [tri state outputs]
- Trigger output
  - 32 Trigger outputs
  - OR32 output
  - Trigger multiplexed output (latch included) [Tri state output]
- Low power : 4.84mW/channel, 155mW/chip

Courtesy : Ryotaro HONDA



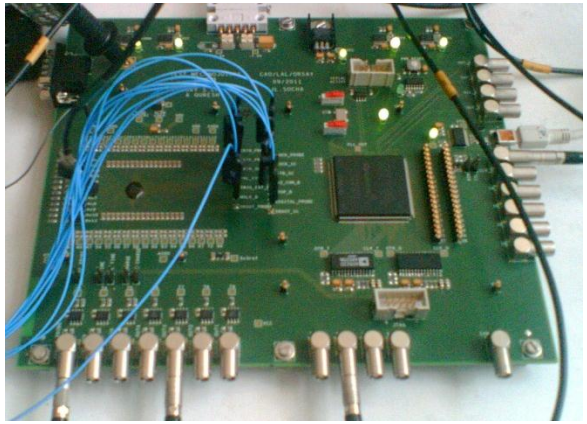
Histogram for 1 to 10 pe- on both gains

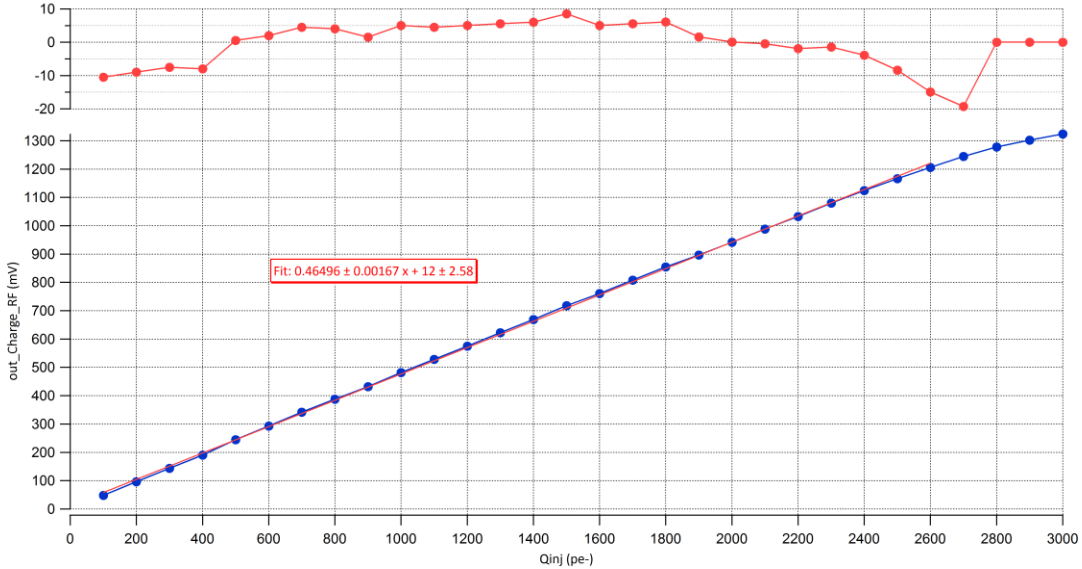
Many applications:

- astrophysics PEBS (Aachen),
- nuclear physics (KEK, Tohoku),
- PET (Roma, Pisa, Valencia),
- Vulcanology (Napoli,IPN Lyon)

New R&D developments: PETIROC

- SiPM readout in 0.35µm SiGe, for physics applications (high resolution time measurements) and therefore also for TOF PET MRI and pre clinical applications,
- 12 channels with 3 different architectures (end of 2011)
- High bandwidth preamp (GBWP> 10 GHz), <3 mW/ch, internal TDC (step=25 ps)
- Dual time and charge measurement up to 2500 pe-





Performance

- Good testbench performance: **jitter < 10 ps rms**
- Patented input stage for dual time and charge measurement
- Strong industrial interest
- Test boards with bonded die available for academic applications

- 16 channels chip to be submitted

- Startup Weeroc http://weeroc.com/ created from OMEGA for industrial applications contact person: Julien Fleury

WEEROC
High-end analogue & mixed microelectronics design

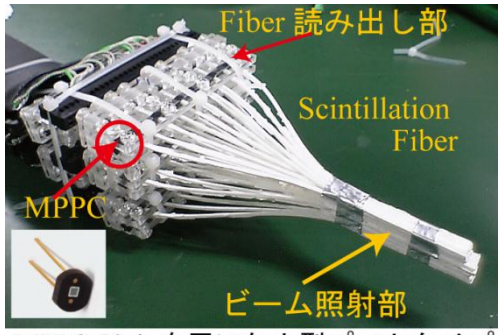
Conclusion

MAROC *(and also SPACIROC , HARDROC, MICROROC)* , PARISROC : for PMTs

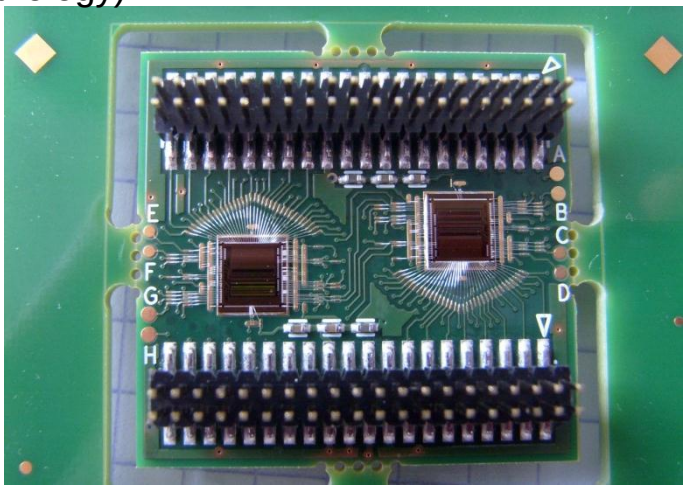
SPIROC, EASIROC for SiPM

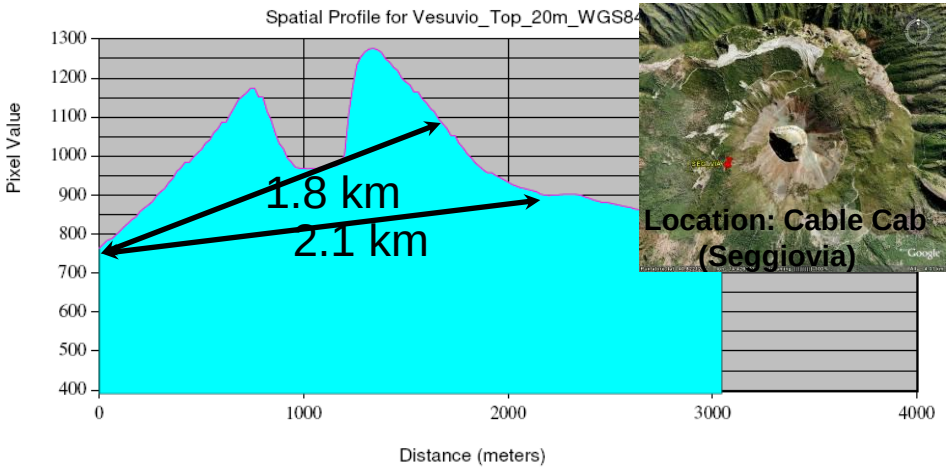
- ✓ Low power multichannel System on Chips, smart detectors
- ✓ Versatility allows these chips to be used in various applications
  - high energy physics, nuclear physics, medical imaging, vulcanology)

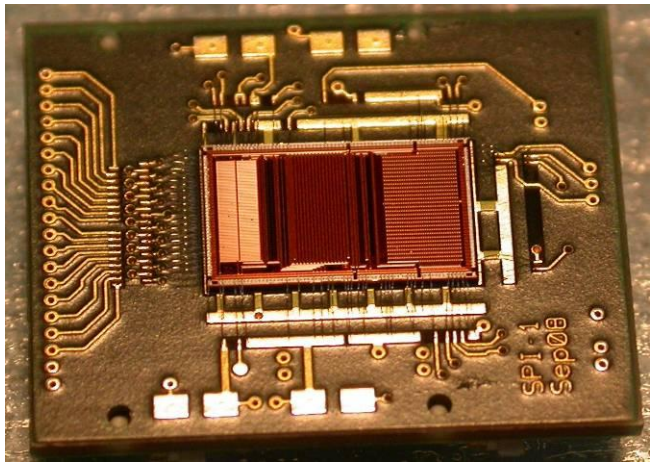
http://omega.in2p3.fr/ and http://weeroc.com/



MPPC 50ch を用いた小型プロトタイプ







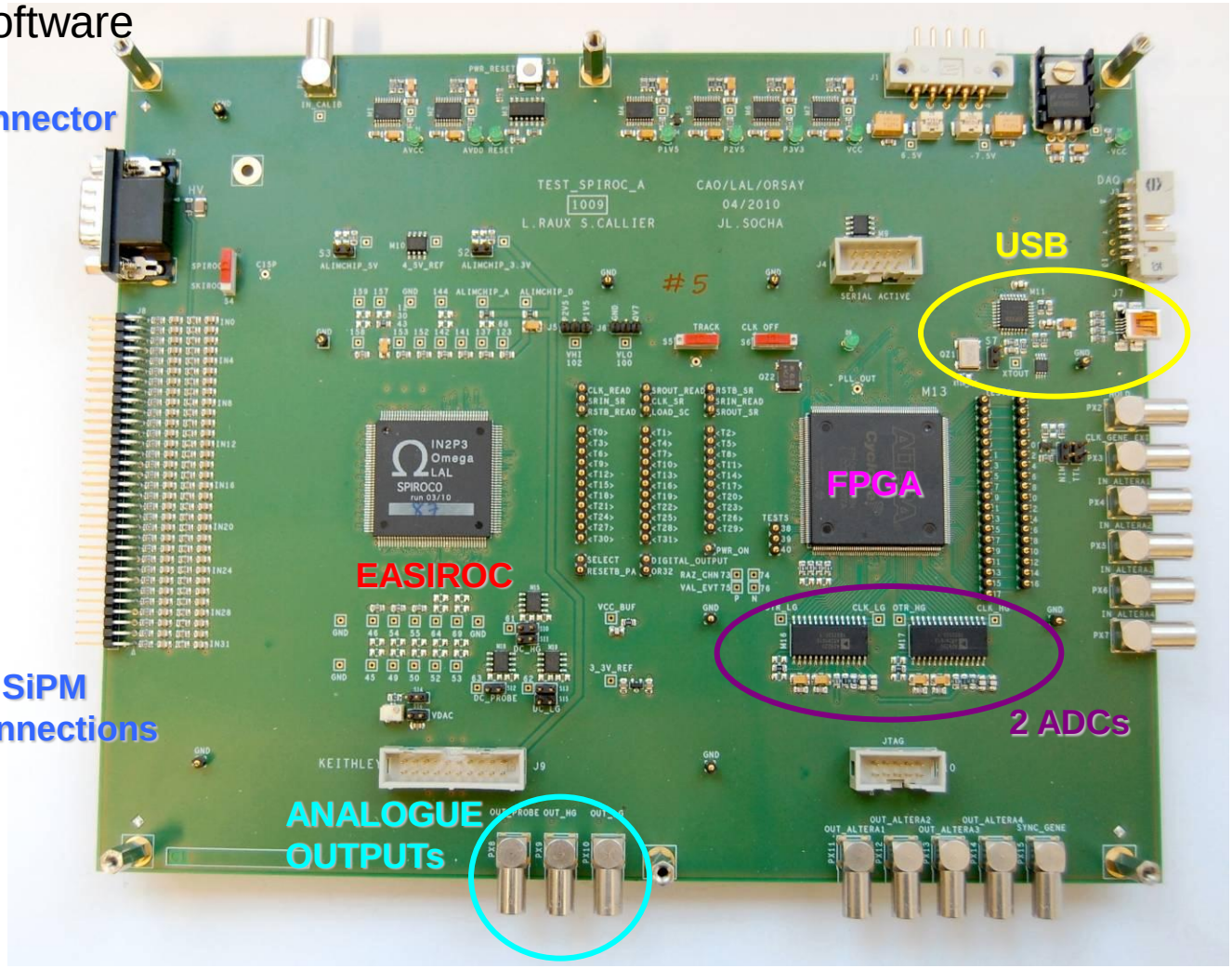
ROC family

	MAROC	SPIROC	EASIROC	HARDROC	MICROROC	SKIROC	PARISROC	SPACIROC
Technology	0.35µ SiGe	0.35µ SiGe	0.35µ SiGe	0.35µ SiGe	0.35µ SiGe	0.35µ SiGe	0.35µ SiGe	0.35µ SiGe
Packages available	•Naked •QFP240	•Naked •TQFP208	•Naked •TQFP160	•Naked •TQFP160	•Naked •QFP160	•Naked •QFP240	•Naked •QFP160	•Naked •CQFP240
Detector compliant	PMT, MAPMT, SiPM, µmegas, RPC	PMT, MAPMT, SiPM, µmegas, RPC, GEM, PIN	PMT, MAPMT, SiPM, µmegas, RPC, GEM, PIN	PMT, MAPMT, SiPM, µmegas, RPC	µmegas	RPC, GEM, PIN	PM matrix	MAPMT
Optimized for	MAPMT	SiPM	SiPM	RPC	µmegas	PIN	PM matrix	MAPMT
Nmber of channels	64	36	32	64	64	64	16	64
Kind of measurement	•Threshold •Charge	•Threshold •Charge •Time	•Threshold •Charge	•Threshold •Charge	•Threshold •Charge	•Threshold •Charge	•Threshold •Charge •Time	•Threshold •Charge
Outputs	64 triggers, 1 mux charge (analogue), 1 mux charge digitized	1 digital formatted output, 1 mux charge (analogue)	32 triggers, 2 mux charge (anlogue), 1 mux trigger	1 digital formatted output, 1 mux charge (analogue)	1 digital formatted output, 1 mux charge (analogue)	1 digital formatted output, 1 mux charge (analogue)	16 triggers, 1 digital formatted output, 1 mux trigger	64 triggers, 9 mux charge
Input Polarity	Negative	Positive	Positive	Negative	Negative	Positive	Negative	Negative

Backup slides

TEST BOARD

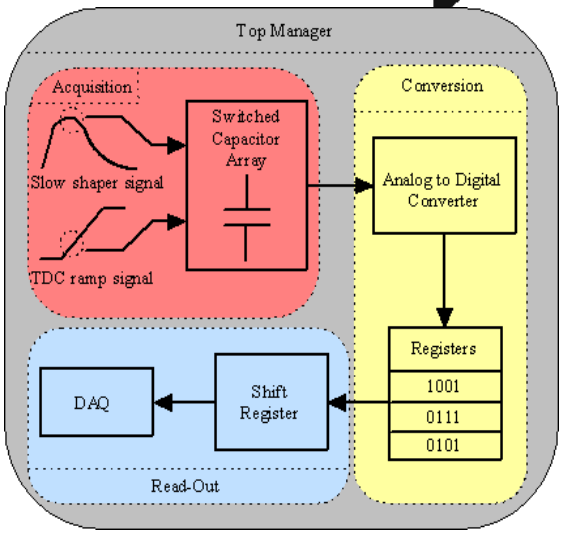
- Testboard allow easy acces to each EASIROC pin
- Testboard layout & cabling @ LAL
- Firmware using LAL USB interface
- Labview software



PARISROC: Independent channels

4 modules: ***Acquisition, Conversion, Read Out and Top manager***.

- ✓ **Acquisition**: Analog memory
- ✓ **Conversion:** Analog charge and time into 8 bits digital value saved in register (RAM)
- ✓ **Read Out:** RAM read out to an external system



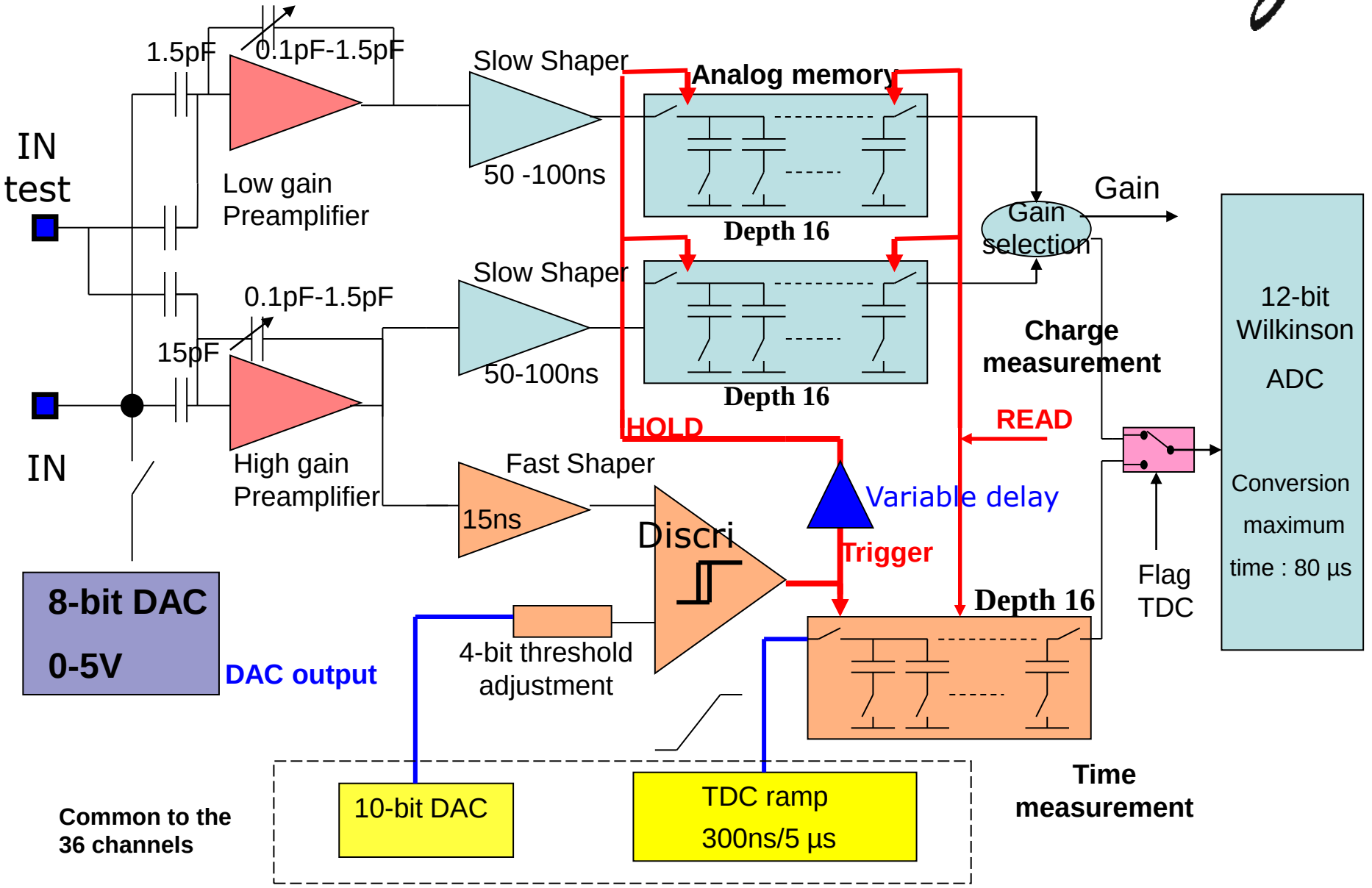
SELECTIVE READOUT

- ✓ Only hit channels are readout
- ✓ Readout clock : 40 MHz
- ✓ Max Readout time (16 ch hit) : 25 µs
- ✓ 51 bits of data / hit channel

	PARIROC 2
Conversion Time	26 µs
Readout Time	25 µs
Total cycle duration	51 µs

	PARIROC 2
Channel number	4
Coarse time counter	24
Extra Coarse time	1
Gain used	1
Charge converted	10
Fine time (TDC) used	1
Fine time (TDC) converted	10
Total	51 bits

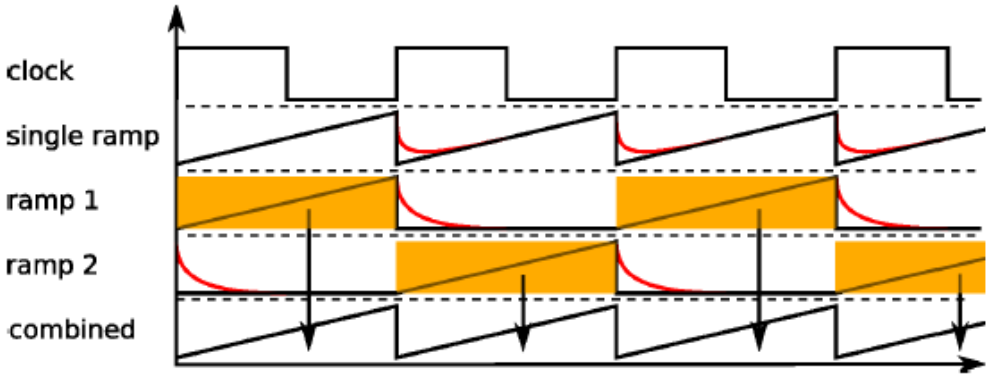
SPIROC general schematic



SPIROC: TDC measurements

Two different TDC modes called (by slow control):

- ILC mode (200 ns to match with the bunch crossing frequency at 5 MHz)
- Testbeam mode (5 µs)



PRELIMINARY RESULTS!

	ILC mode
Time dynamic range	220 ns
"Blind zone"	100 ns
linear zone	120 ns
Ramp linearity	~ ± 1 ns

Mark Terwort
CALICE collaboration meeting
Matsumoto, March 6th, 2012

TDC reconstruction in auto-trigger mode by 12-bit ADC
ILC mode