# A quadruple well CMOS MAPS prototype for the Layer0 of the SuperB SVT

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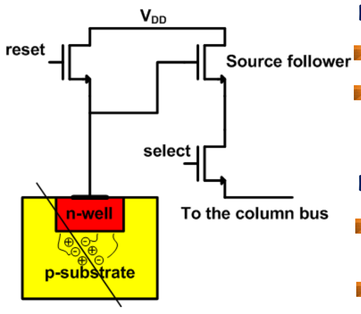
## Abstract

In the last decade, the use of standard deep submicron CMOS technologies for the implementation of monolithic active pixel sensors (MAPS) for HEP experiments has been thoroughly investigated. One of the main issues with this approach is the fact that the charge collection efficiency may be negatively affected by the presence of competitive N-wells used to integrate PMOS transistors in the readout chain. These N-wells act as parasitic collecting electrodes subtracting part of the charge generated by a minimum ionizing particle (MIP) from the sensor. On the other hand, PMOS transistors are needed to design high performance, low power analog and digital blocks. A novel approach for isolating the PMOS competitive N-wells is based on the use of a planar 180 nm CMOS process with quadruple well called INMAPS. This work introduces the channel readout design features of the chip Apsel4well developed with the mentioned approach and shows results of device simulations of a 3x3 pixel matrix charge collection performance.

## CMOS MAPS 3T



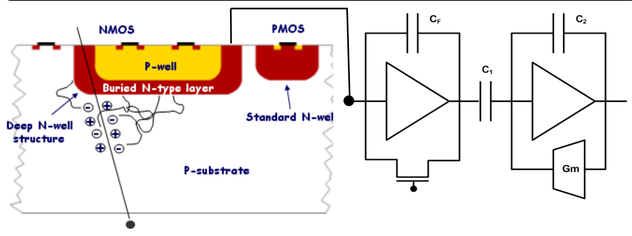

DESIGN CRITERIA:

- Fill factor maximization
- N-well area minimization (Noise proportional to $(C_D)^{0.5}$)

DRAWBACKS:

- Charge sensitivity depending on $C_D$
- **Only NMOS transistors**

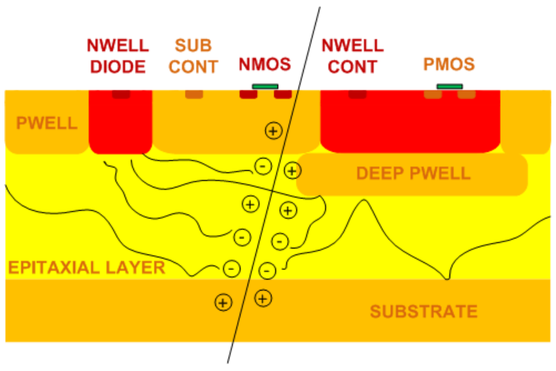
## Deep N-well CMOS MAPS




- A large DNW is used to collect the charge released in the substrate
- A capacitive readout chain performs the Q-V conversion
- PMOS transistors can be included in the front-end design
- **DRAWBACK: large detector parasitic capacitance**

## 180 nm CMOS INMAPS process

Planar CMOS technology featuring an additional processing step : a high energy deep P-well implant is deposited beneath the N-wells (except for the N-well diodes acting as collecting electrodes).




This implant creates a barrier for the charge diffusing in the epitaxial layer, preventing it from being collected by the positively biased N-wells of the in-pixel circuits and allowing a **theoretical charge collection efficiency of 100%.** The NMOS transistors are designed in heavily doped P-wells located over a lightly doped epitaxial layer.

## Epitaxial layer

The epitaxial layer, featuring a resistivity higher than both the deep P-well and the substrate, plays an important role in the improvement of the charge collection properties: in fact, the presence of two small potential barriers (deep P-well/epitaxial layer or P-well/epitaxial layer and epitaxial layer/substrate) keeps the carriers within the epitaxial layer, preventing them from diffusing through the substrate.
The foundry provides two different typologies of epitaxial layer:

- Standard resistivity (50 Ω·cm)
- High resistivity (1 kΩ·cm)

Advantages of a high resistivity epitaxial layer:

- Better charge collection properties (higher collected charge, collection speed)
- Higher bulk damage hardness expected

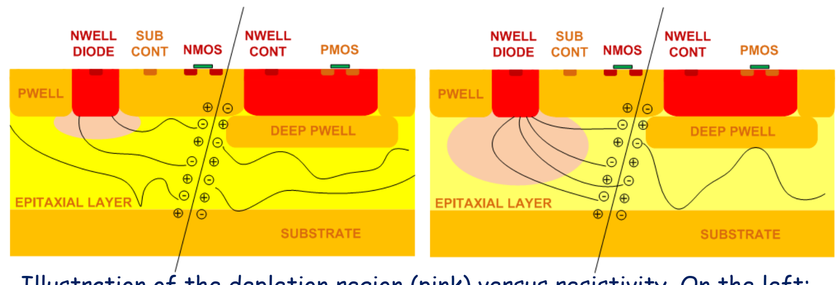
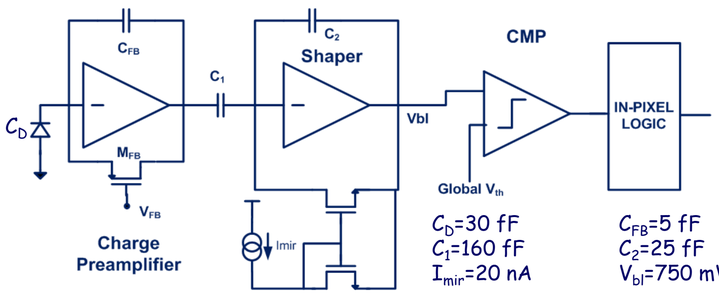



Illustration of the depletion region (pink) versus resistivity. On the left: standard resistivity silicon. On the right: high resistivity silicon.

## Front-end design and device simulations

The features of CMOS INMAPS process have been exploited in the design of the Apsel4well chip. The Apsel4well pixel features a 50 µm pitch, complying with the requirements of the SVT Layer0 of the SuperB experiment. The pixel sensor is read out by a classical channel for capacitive detectors including a charge preamplifier, a shaper and a threshold discriminator, followed by the in-pixel readout logic. Besides analog smaller (3x3) pixel matrices and single channels, the Apsel4well chip also includes a 32x32 matrix which implements a sparsified readout architecture with time stamping.

## Analog Front-end design

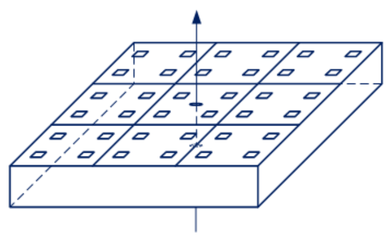


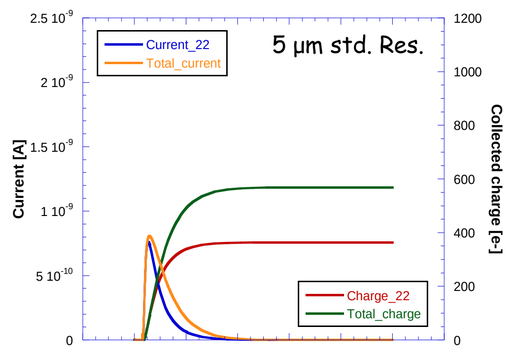

| Simul. Performance | Apsel4well |
|---|---|
| Charge sensitivity | 930 mV/fC |
| $t_p$ @ 800 injected $e^-$ | 240 ns |
| ENC ($C_D$ = 30 fF) | 26 e- |
| Threshold dispersion | 23 e- |
| NLI (@ 2000e-) | 1% |
| Analog Power cons. | 18 µW/pix |

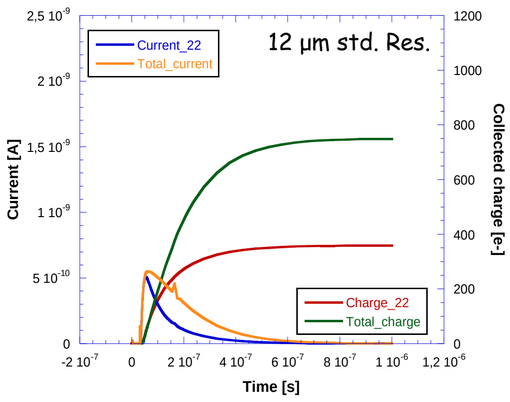
- 4 interconnected squared N-well diodes (1.5 µm side) as collecting electrode instead of a large DNW: lower noise and power consumption.
- Stage I: charge PA with a $C_{FB}$ continuously discharged by a PMOS biased in deep subthreshold region.
- Stage II: shaper with a mirror feedback configuration for $C_2$ discharge instead of a transconductor (lower noise and $V_{bl}$ dispersion).
- Stage III: active load comparator.

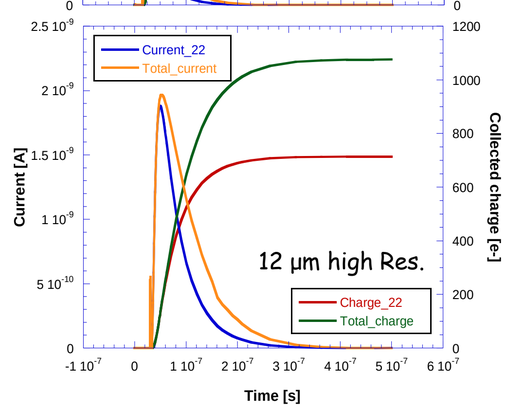
## Device simulations

Synopsys TCAD simulations of the charge collection performance of a 3x3 matrix featuring the same layout geometry and doping profiles of the one implemented in the Apsel4Well chips have been performed. The following graphs show the current and the charge collected by the central pixel (22) after the crossing of an impinging MIP in the matrix center (see figure). Simulations have been performed for different doping and thickness values of the epitaxial layer. As expected, results show a better behavior in the case of a 12 µm high resistivity epitaxial layer, in terms of both collected charge and collecting time.

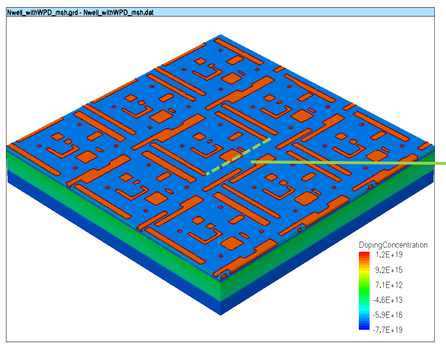


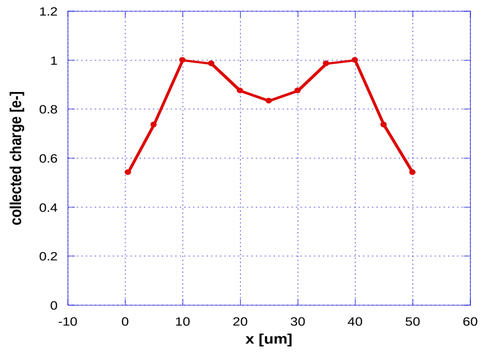


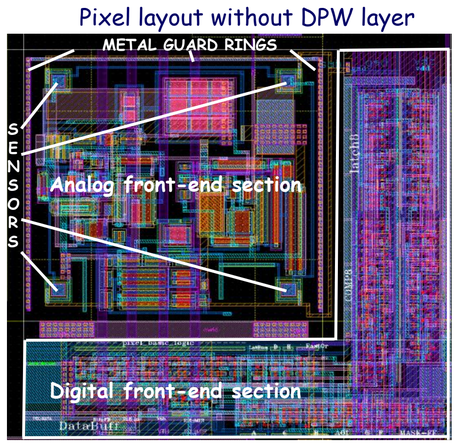

The charge collection uniformity along a section of the central pixel has been evaluated by moving the MIP impact point along the green dotted line in the case of a 12 µm thick high resistivity epitaxial layer. The plot on the right highlights the beneficial effect of the deep P-well, which prevents charge from being collected by the parasitic N-wells located under the green line. The minimum collected charge value is about the 80% of the maximum corresponding to the collecting electrode positions.



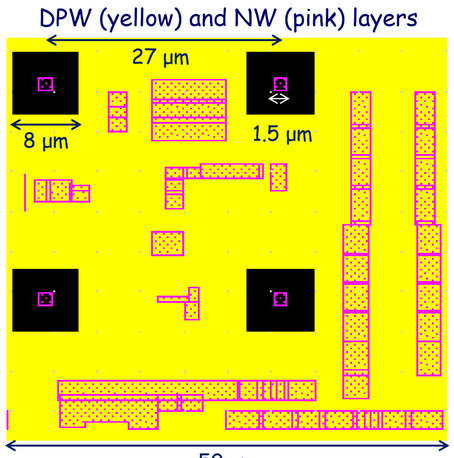




## Apsel4Well pixel layout

Pixel layout without DPW layer

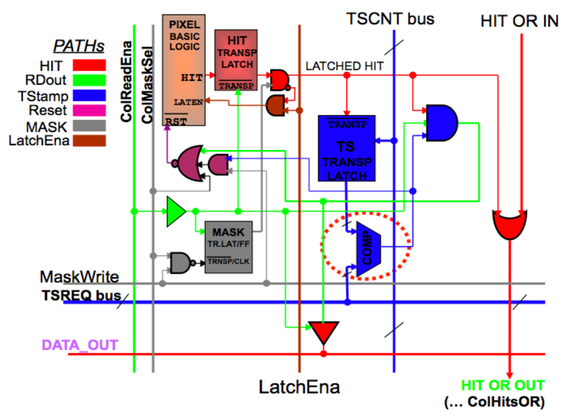



DPW (yellow) and NW (pink) layers




## Digital Front-end

Triggered readout architecture with timestamp




Timestamp (TS) is broadcast to pixels and each pixel latches the current TS when fires. The matrix readout is timestamp ordered. A readout TS enters the pixel and a HIT-OR-OUT signal is generated for columns with hits associated to that TS. A column is read only if HIT-OR-OUT=1. DATA_OUT is generated for pixels in the active columns with hits associated to that TS.