Silicon n-in-p Pixel Sensors for future ATLAS Upgrades

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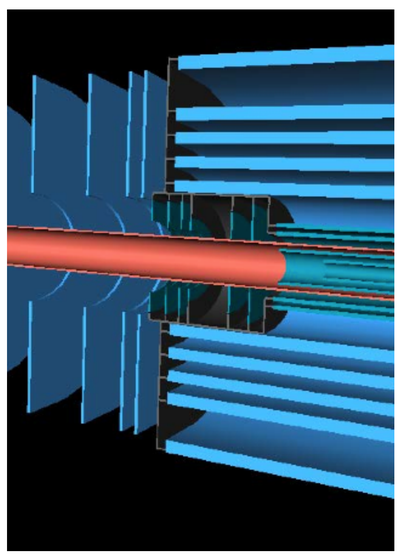
Introduction

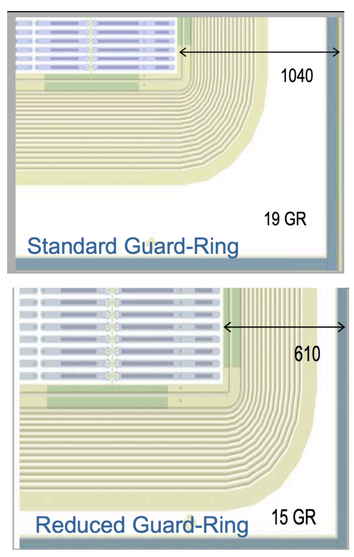
ATLAS Pixel Detector Upgrade:



- **2022 (Phase 2)**: Inner detector Tracker (ITK)
  - Complete new ATLAS tracker (Pixel and Strip detectors)
  - Much larger Pixel surface w.r.t. current Pixel Detector: ~7-10 m^2
  - Luminosity: $5x10^{34}$ $cm^{-2}s^{-1}$
  - Radiation dose (innermost layer): $2x10^{16}$ 1-MeV n_{eq} cm^{-2}
- ***Planar n-in-p as future sensor technology:***
  - Excellent candidate for large volume
  - Single side processing → reduced cost
  - Radiation hardness comparable to n-in-n

Sensor description

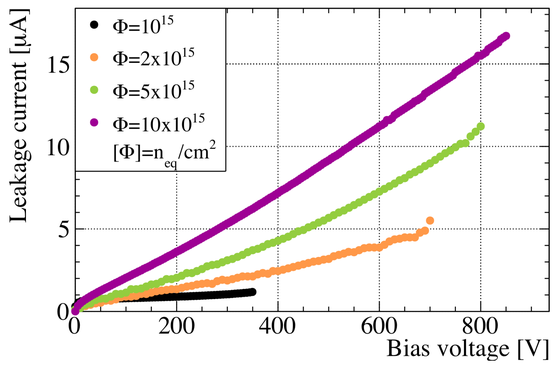
First CiS n-in-p Pixel production



- Production on 4” Fz p-type wafer, 285 um thick
- Inter-pixel isolation:
  - Moderated p-spray
  - Homogeneous p-spray
- Bump bonding to the ATLAS Pixel Front-End Chip (FE-I3) performed by IZM-Berlin
- BCB layer deposited on the sensor front side as an isolation to prevent sparks between sensor and chip

Test Results

Leakage currents (after irradiation)

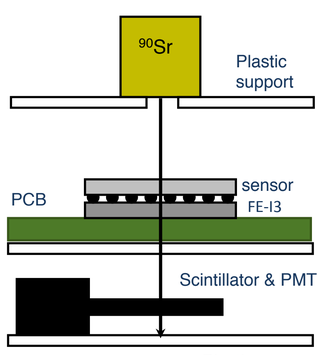


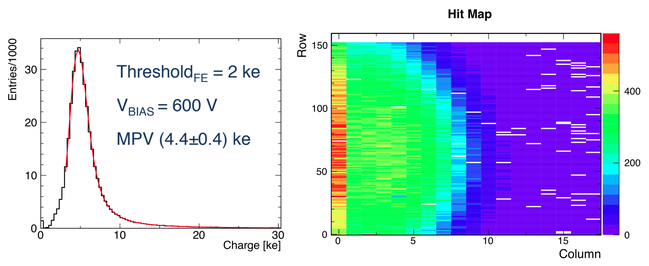
Before irradiation (at +20ºC)
All modules show leakage currents below 6 uA, with a bias voltage of 150 V [1,2,3].

After irradiation (scaled at -20ºC)
The breakdown voltages shifted to higher values and for the highest fluence it exceeds 800 V.
Also the leakage currents show higher values with increasing fluences.

External-trigger operation with ^{90}Sr source

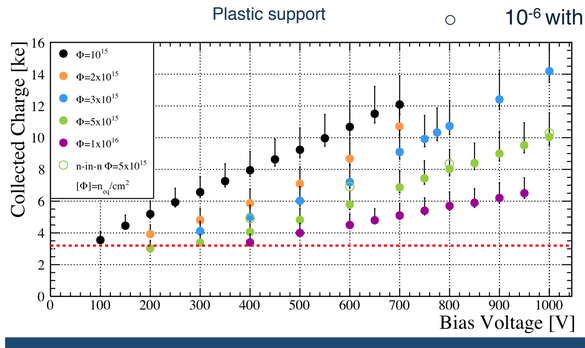
Collected charge measured with module irradiated up to $1x10^{16}$ n_{eq} cm^{-2}





Module irradiated up to $1x10^{16}$ n_{eq} cm^{-2} and biased at 600V:

- Collected charge / Front-end Threshold > 2
- Noise occupancy
  - 10^{-7} with 1% masked channels
  - 10^{-6} with 0.5% masked channels

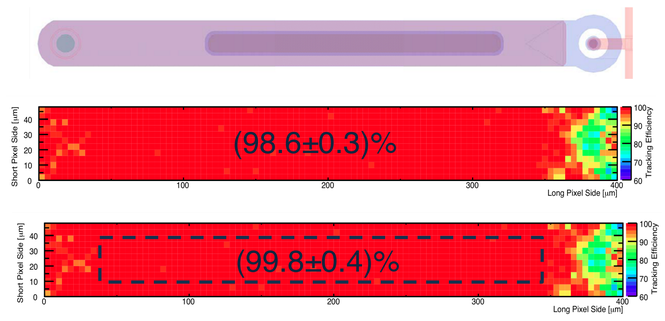


Collected charge as a function of the bias voltage with the front-end chip tuned to a threshold of 3.2ke by irradiated modules

Result from n-in-n module are from S. Altenheiner et al., NIM A678 (2011) 25

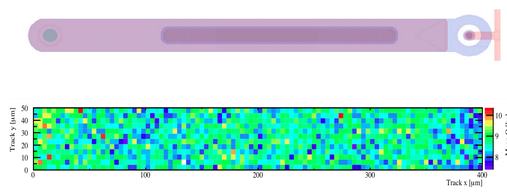
- Tracking efficiency

Mean tracking efficiency as a function of the track impact point for a module irradiated up to $5x10^{15}$ n_{eq} cm^{-2} and biased at 600V [2,4].

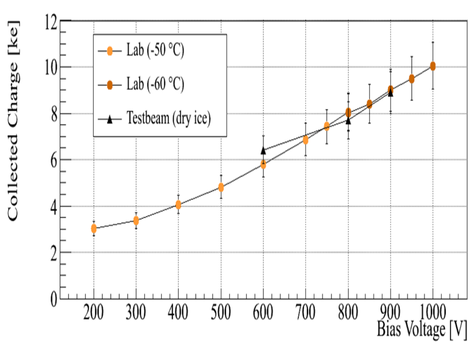


At 600 V:
Overall efficiency : 98.6%
Loss mostly around bias dot
Efficiency of 99.8% for rest of pixel

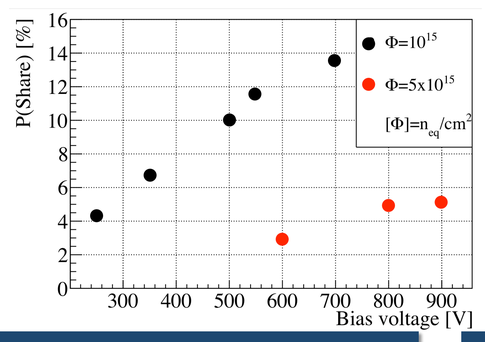
- Charge collection



Mean collected charge as a function of the track impact point for a module irradiated up to $5x10^{15}$ n_{eq} cm^{-2} and biased at 600 V.



- Charge sharing



Dependence of charge sharing P(Share) probability as a function of the bias voltage for modules irradiated up to 10^{15} n_{eq} cm^{-2} and $5x10^{15}$ n_{eq} cm^{-2}

Summary and future plans

- Excellent performance of CiS n-in-p modules irradiated up to 10^{16} 1-MeV n_{eq} cm^{-2}.
- New production on 4” FZ p-type wafer of 200um and 300um thickness compatible with ATLAS IBL front-end chip (FE-I4) processed. Source, beam tests and irradiation up to HL-LHC fluences planned.
- First production of 6” wafers on high resistivity Fz p-type material, with 4-chip and 1-chip modules is foreseen.

References

[1] P. Weigell et al., NIM A658 (2011) 36
[2] C. Gallrapp et al., NIM A679 (2012) 29
[3] A. Macchiolo et al., arXiv:1110.4468
[4] J. Weingarten et al., arXiv:1204.1266