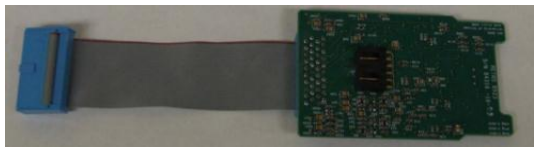
Upgrade for the ATLAS Tile Calorimeter Readout Electronics at the High Luminosity LHC

Modified 3-in-1

- University of Chicago
- Reception and shaping of PMT signals
  - Fast signal processing
    - 7-pole LC shape: 50ns FWHM shaping time
    - Bi-gain readout: gain ratio of 16
    - Digitization in MainBoards using 12 bit ADC
  - Slow signal processing
    - Integrator to read out Cesium calibration data
- Charge injection calibration and controls

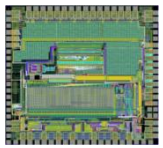


Modified 3-in-1 card

QIE

- Argonne National Laboratory (ANL)
- Current splitter with multiple ranges and gated integrator
- On-board flash ADC
- 4 different gain ranges
- 40 MHz operation
- 16-bit dynamic range
- Dead-timeless digitization
- Pipelined operation
- Charge injection for calibration
- Integrator for calibration with source

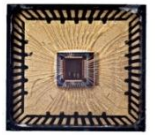
QIE7 MINOS



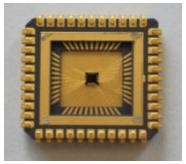
QIE 10.3

FE-ASIC

- Clermont-Ferrand (LPC)
- IBM CMOS 130 nm technology
- FATALIC 3 features:
  - Current conveyor
  - Shaping stage
  - 3 different gain ranges (1, 8, 64)
  - 80MHz operation
- TACTIC features:
  - 12-bits pipeline ADC
  - 40MHz operation



FATALIC 1 (0.8 cm)

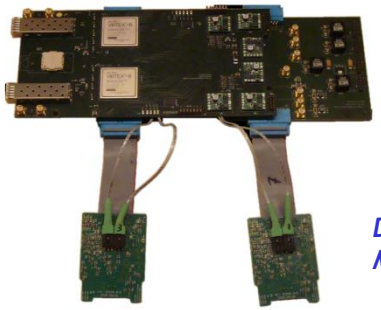


FATALIC 2 (1.7 cm)

Upgrade for the ATLAS Tile Calorimeter Readout Electronics at the High Luminosity LHC

MainBoard and DaughterBoard

- University of Chicago & University of Stockholm
- MainBoard:
  - Digitizes signals coming from 4 modified 3-in-1 cards
  - Readout of 12 PMTs
  - Sends digitized data to the DaughterBoard
  - Maintains compatibility with other Front-End Board alternatives
- DaughterBoard
  - Data processing unit
  - High speed communication between on and off-detector electronics (sROD)



DaughterBoard plugged in a MainBoard with two 3-in-1 cards

Super Read Out Driver (sROD)

- IFIC-Valencia, LIP & University of Stockholm
- sROD demonstrator board:
  - Data reception and processing from one new drawer
  - Pipeline and derandomizer memories
  - Timing, Trigger and Control (TTC) and Detector Control System (DCS) management and transmission to MainBoards
  - Data reconstruction and transmission to Read Out Subsystem (ROS)
  - Data preprocessing and transmission to L1Calo
  - Double mid-size AMC board