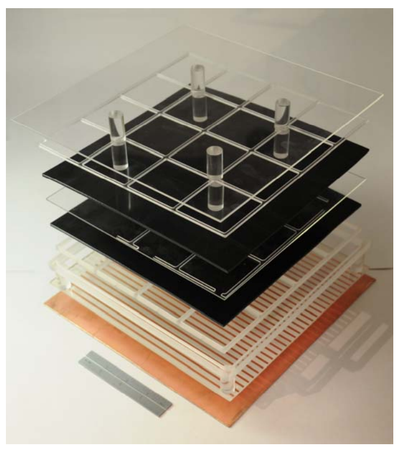
A 10-15 GSa/s Switched Capacitor Array DAQ System for a Position & Time Sensing Large-Area Photo-Detector



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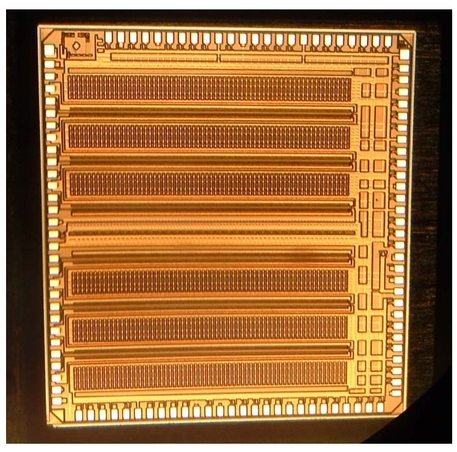
Large-Area Picosecond Photo-Detectors (LAPPD) Collaboration
(*http://psec.uchicago.edu*)

Abstract

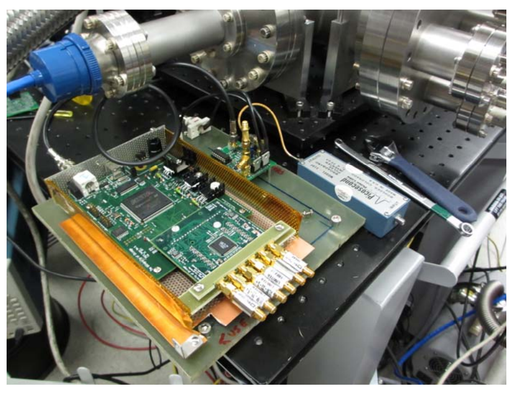
A data acquisition (DAQ) system using 10-15 Gigasamples/second (GSa/s) waveform sampling Application Specific Integrated Circuits (ASICs) for the readout of large active-area micro-channel plate photomultiplier tubes (MCP -PMTs) is presented. The development and characterization of these 20x20 sq. cm active-area MCP 'tiles' are ongoing by the Large-Area Picosecond Photo-Detector Collaboration (LAPPD). Signals from the large-area MCP tile are acquired from a 50-ohm transmission line anode comprised of 30 parallel microstrips. The position, timing, and energy of the incident pulse are extracted from the waveforms that are recorded at both ends of the anode. The target geometry of the DAQ system is the very large-active area 'Super Module', made of a 3x4 array of LAPPD MCP tiles, that requires 90 channels of compact, high bandwidth waveform sampling on both sides of the detector. For this task, a 6-channel, 15 Gsa/s, and 1.5 GHz bandwidth waveform digitizing ASIC, 'PSEC-4', was designed in 0.13 micron CMOS using a 256 sample-per-channel switched capacitor array architecture. Sampled waveforms are digitized on-chip and a region-of-interest in the data buffer is serially read off-chip for downstream analysis. The Super Module DAQ incorporates two hardware levels of FPGA-implemented ASIC control and waveform feature extraction. Ultimately, the reduced event data are sent from the Central Card to a computer via a gigabit Ethernet connection.

PSEC-4 Front-end Waveform Digitizing ASIC

	ACTUAL PERFORMANCE
Sampling Rate	2.5-15 GSa/s
# Channels	6
Sampling Depth	256 points (17-100 ns) per channel
Input Noise	<1 mV RMS
Analog Bandwidth	1.5 GHz (f_{3dB})
ADC conversion (ramp-compare)	Up to 12 bit (10 ENOB) clocked @ 1.6 GHz
Dynamic Range	0.1-1.1 V
Readout Latency	2 µs (min) – 16 µs (max)



MCP integrated testing

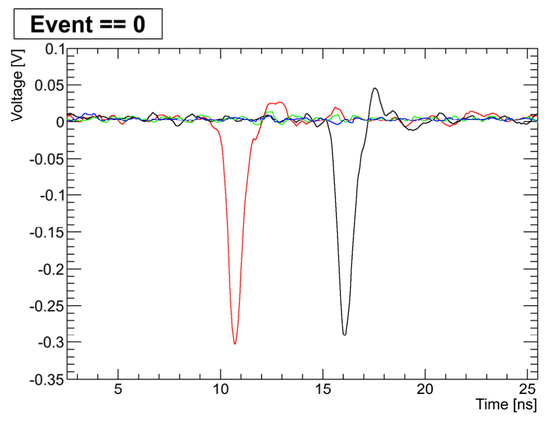


Dual-end readout of LAPPD 8" MCP w/ PSEC-4 @ 10 GSa/s

-- left anode strip
-- right anode strip

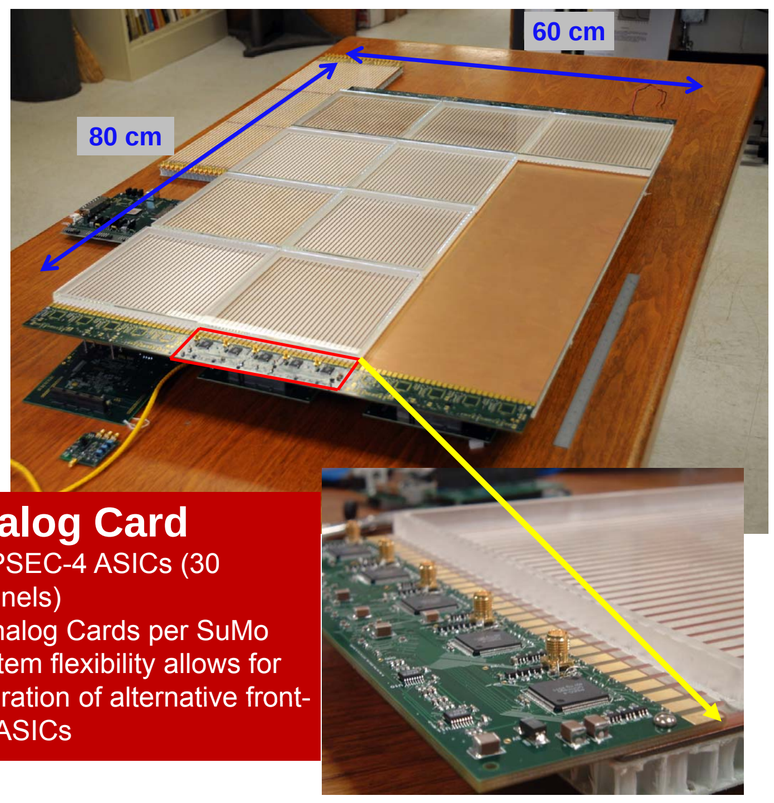
6-channel PSEC-4 evaluation board in use at LAPPD MCP test stand

The relative timing between signals captured at both terminals of the 50Ω microstrip anode is used to determine the position of a detector event.



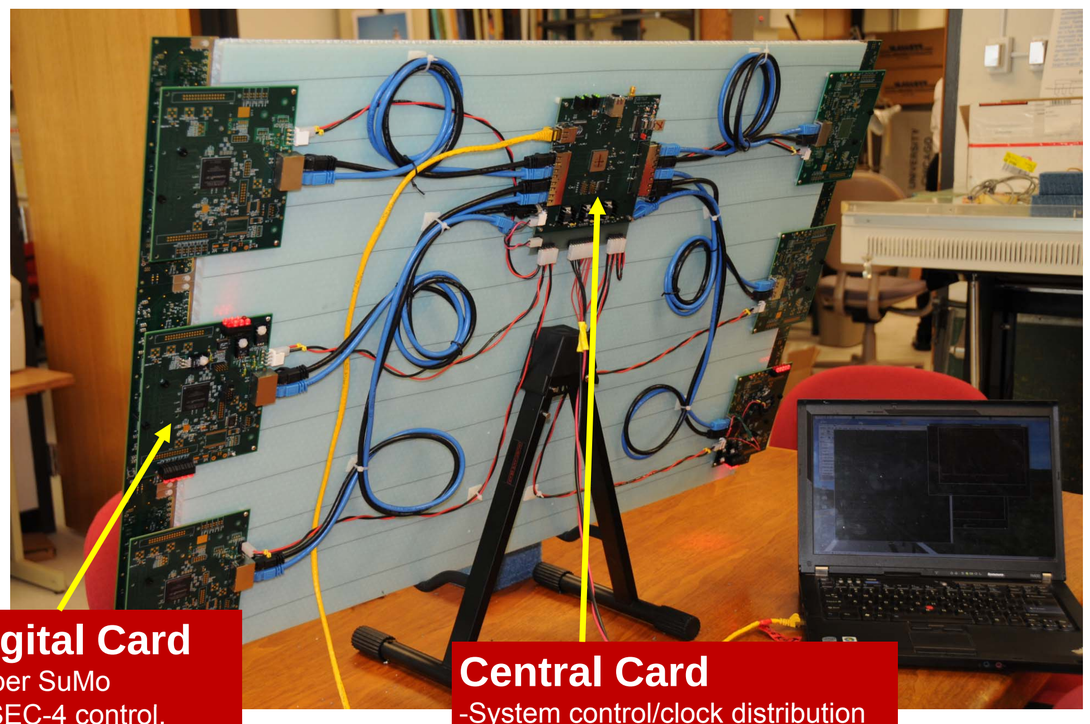
Super Module (SuMo) MCP Photodetector

Front: **0.5 m² of photosensitive area**



Analog Card
– 5 PSEC-4 ASICs (30 channels)
-6 Analog Cards per SuMo
-System flexibility allows for integration of alternative front-end ASICs

Back: **Integrated back-end electronics**



Digital Card
-6 per SuMo
-PSEC-4 control, trigger handling, local data reduction & calibration

Central Card
-System control/clock distribution
-Feature extraction & event pairing
-CPU/GPU interface
(gigabit Ethernet & USB 2.0)

System Features & Specifications

- 90 channels of custom waveform sampling (WFS) ASIC readout per module.
- Each MCP tile has a bandwidth (BW) of >1 GHz. By connecting 4 in series, the system BW drops to ~400 MHz. Should achieve <1 cm position resolution
- Back-end electronics accommodates various existing WFS ASIC designs (new Analog Card required)
- System operates from a single 5V supply (13A max).
- Digital<->Central card communication via 8 LVDS lines. SerDes data transfer may be performed at up to 800 Mbps per line.
- Flexible readout system for an arbitrary arrangement of 8" MCP tiles.
- Robust FPGA algorithms for feature extraction and data reduction under development.
- **Large active photodetector area + highly integrated, compact DAQ system**

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