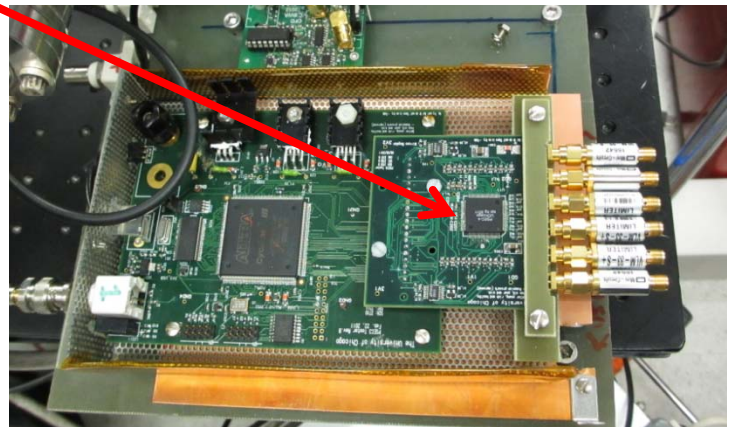
A 10-15 GSa/s Switched Capacitor Array DAQ System for a Position & Time Sensing Large-Area Photo-Detector

PSEC-4 ASIC (*University of Chicago*)

10-15 GSa/a Waveform Sampling ASIC

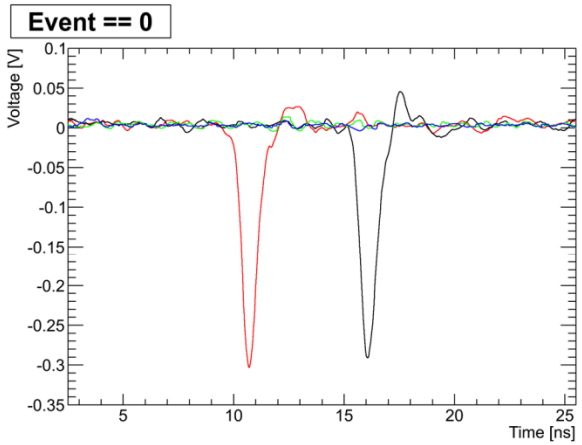
Designed as part of the Large-Area Picosecond Photo-Detector **(LAPPD)** project

	ACTUAL PERFORMANCE
Sampling Rate	2.5-15 GSa/s
# Channels	6
Sampling Depth	256 points (17-100 ns) per channel
Input Noise	<1 mV RMS
Analog Bandwidth	1.5 GHz (f_{3dB})
ADC conversion (ramp-compare)	Up to 12 bit (10 ENOB) clocked @ 1.6 GHz
Dynamic Range	0.1-1.1 V
Readout Latency	2 µs (min) – 16 µs (max)



6-channel PSEC-4 evaluation board in use at LAPPD micro-channel plate (MCP) test stand

Signals from the large-area MCP tile are acquired from a 50-ohm transmission line anode. The relative timing between signals captured at both terminals of the microstrip anode is used to determine the position of a detector event.



Dual-end readout of LAPPD 20x20 cm² MCP w/ PSEC-4 @ 10 GSa/s

-- left anode strip
-- right anode strip

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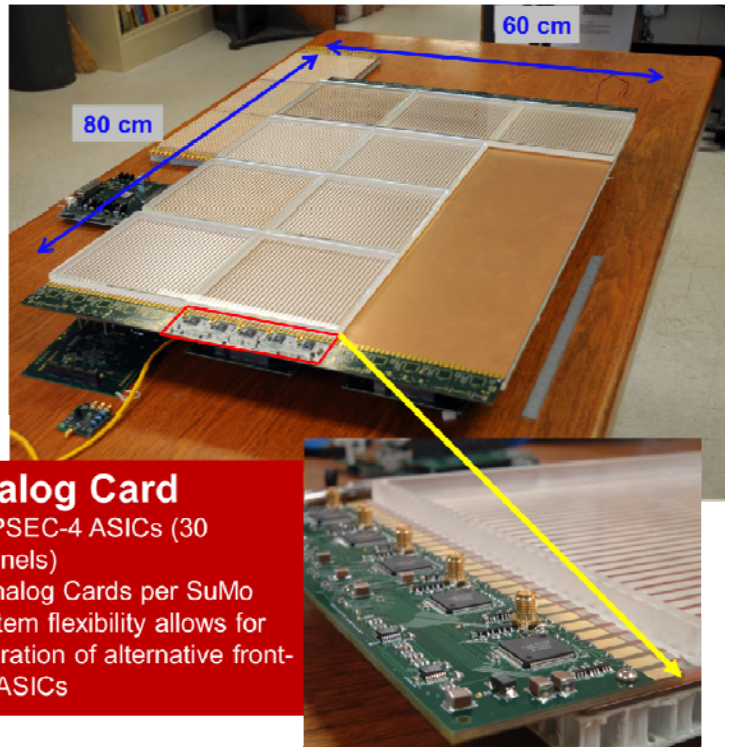
Super Module (SuMo) Photodetector DAQ

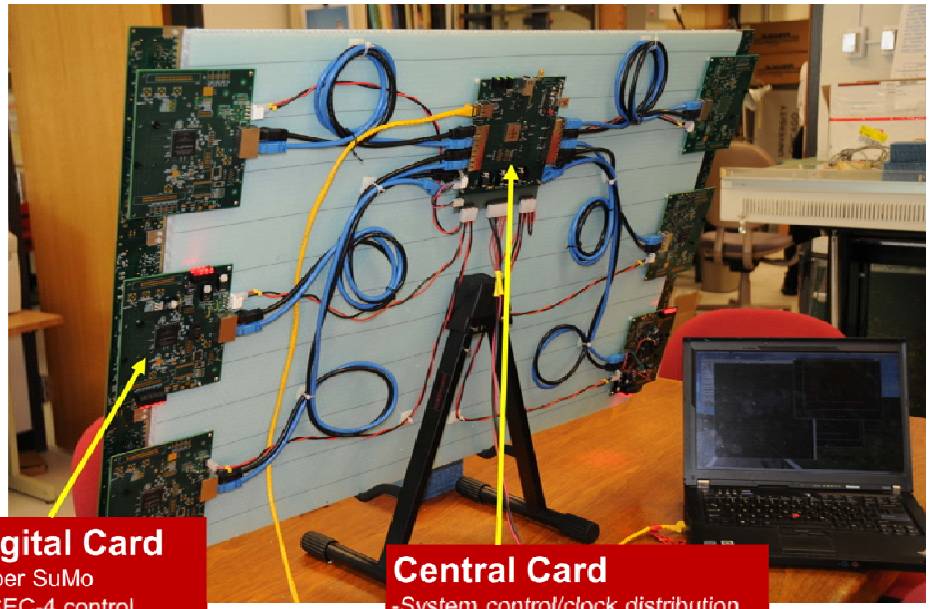
The **SuMo** photodetector, made from a 3x4 array of LAPPD MCP tiles, requires 90 channels of compact, high bandwidth waveform sampling on both sides of the detector. Integrated to the detector, the **PSEC-4** ASIC based DAQ incorporates two hardware levels of FPGA-implemented ASIC control and waveform feature extraction.

Front: **0.5m^2 of photosensitive area + front-end PSEC-4 (10GSa/s) waveform recording**



Analog Card
– 5 PSEC-4 ASICs (30 channels)
-6 Analog Cards per SuMo
-System flexibility allows for integration of alternative front-end ASICs

Back: **Integrated back-end electronics**



Digital Card
-6 per SuMo
-PSEC-4 control, trigger handling, local data reduction & calibration

Central Card
-System control/clock distribution
-Feature extraction & event pairing
-CPU/GPU interface
(gigabit Ethernet & USB 2.0)

Large active photodetector area + highly integrated, compact DAQ system