High rate particle tracking and ultra-fast timing with a thin hybrid silicon pixel detector

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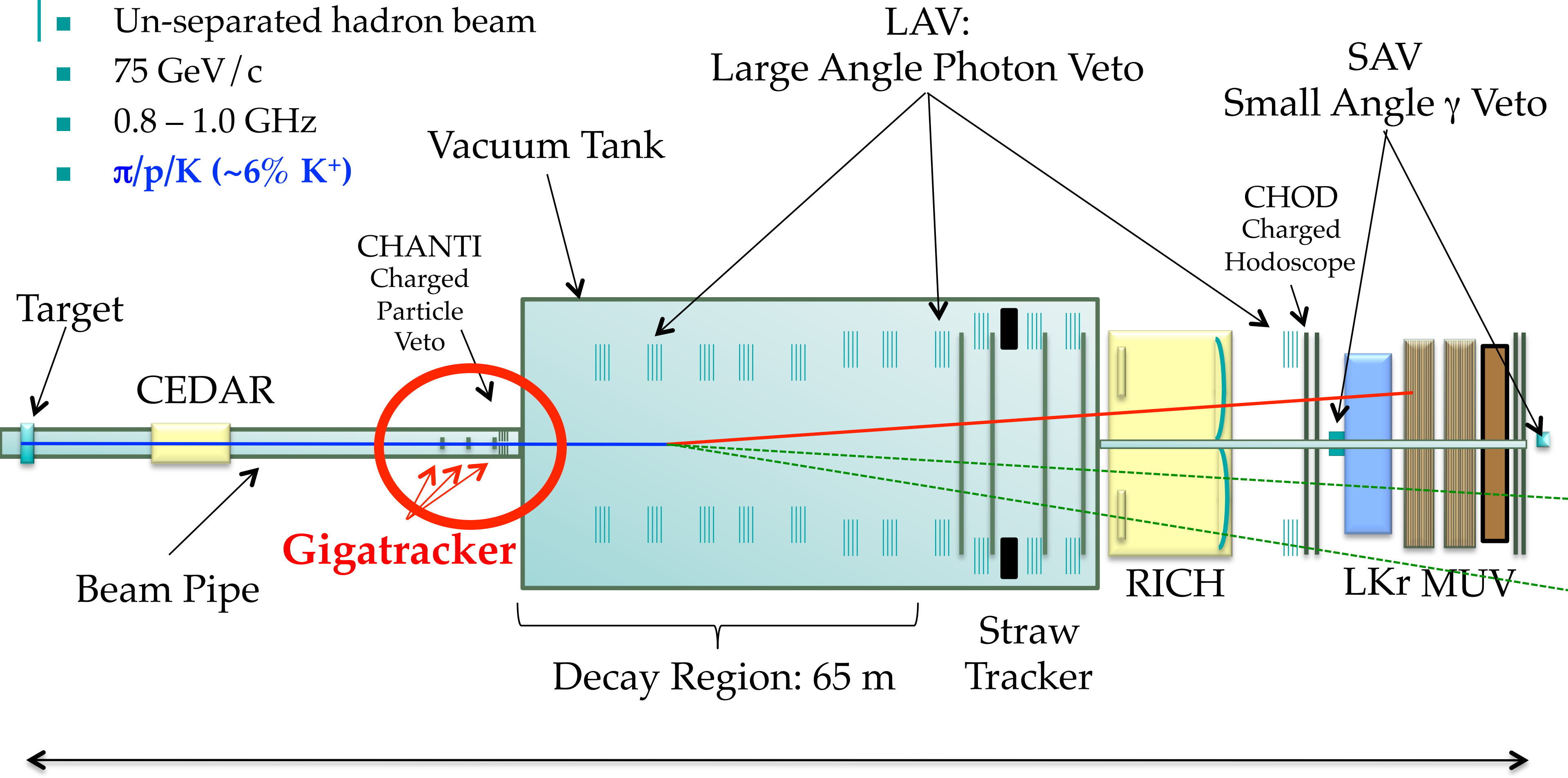
Outline

- The Gigatracker detector system
  - The NA62 experiment at the CERN SPS
  - The beam spectrometer: physics requirements
  - Sensors and bump-bonding
  - Low-mass cooling system (micro-channels)
  - Read-out architecture
- Results of prototype bump-bonded assemblies test
  - Infra-red laser setup
  - Test-beam
  - Contributions to detector time resolution
- Conclusions

NA62 detector layout

- Measurement of **$K^+ \to \pi^+ \nu \bar{\nu}$** at the CERN SPS
- Un-separated hadron beam
- 75 GeV/c
- 0.8 – 1.0 GHz
- **$\pi/p/K$ (~6% K^+)**



LAV:
Large Angle Photon Veto

SAV
Small Angle γ Veto

Vacuum Tank

CHOD
Charged
Hodoscope

CHANTI
Charged
Particle
Veto

Target

CEDAR

Gigatracker

Beam Pipe

RICH

LKr MUV

Straw
Tracker

Decay Region: 65 m

Total Length: 270 m

NA62 detector layout

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- Un-separated hadron beam
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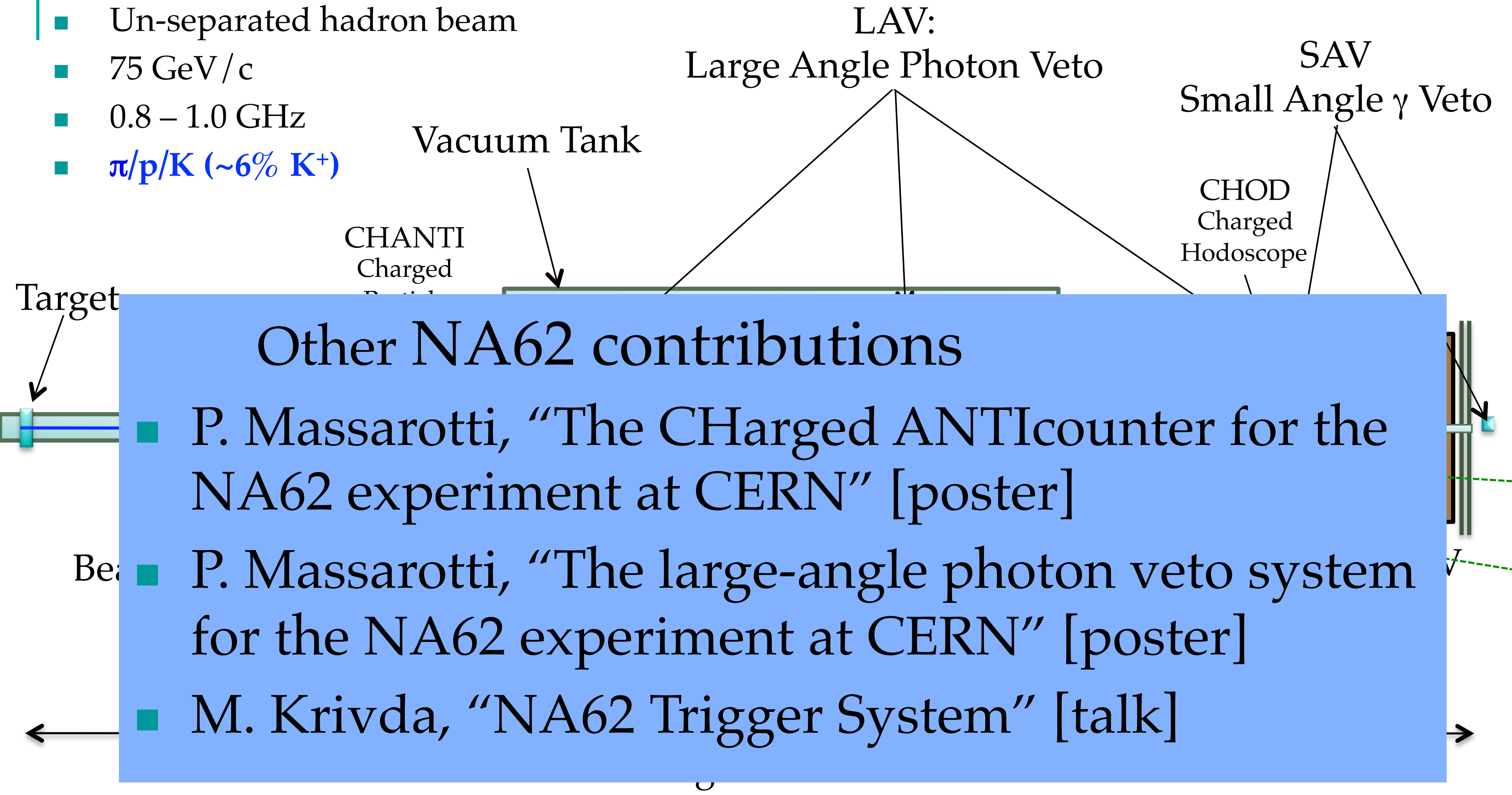
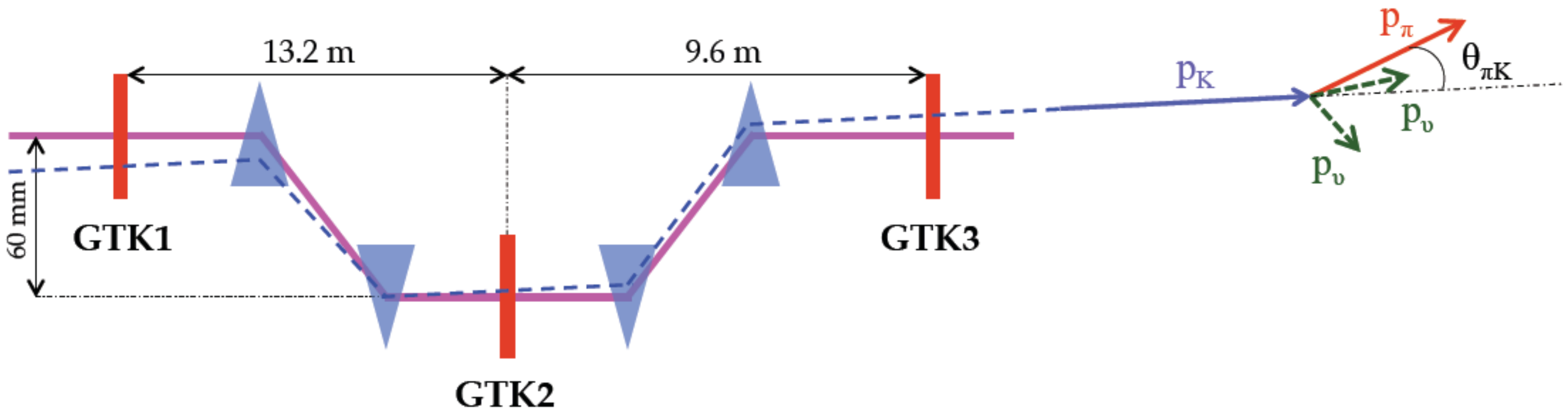
- $\pi/p/K$ (~6% K^+)



Other NA62 contributions

- P. Massarotti, “The CHarged ANTIcounter for the NA62 experiment at CERN” [poster]
- P. Massarotti, “The large-angle photon veto system for the NA62 experiment at CERN” [poster]
- M. Krivda, “NA62 Trigger System” [talk]

The GigaTracKer (GTK)

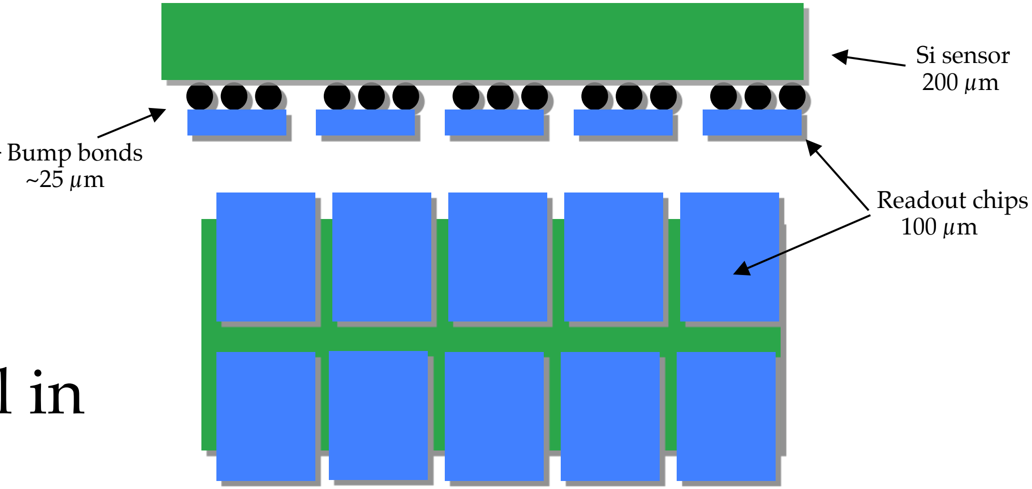


- Beam spectrometer
  - provide precise momentum, time and angular measurements on all beam tracks
  - sustain high and non-uniform rate (~1.5 MHz/mm^2 in the center, 0.8-1.0 GHz total)
  - reduce multiple scattering and beam hadronic interactions

- X/X_0 <0.5% per station
- $\sigma(p_K)/p_K$ ~0.2%
- $\sigma(\theta_K)$ ~16 μrad
- pixel size 300 μm × 300 μm
- **$\sigma(t)$ ~150 ps** on single track

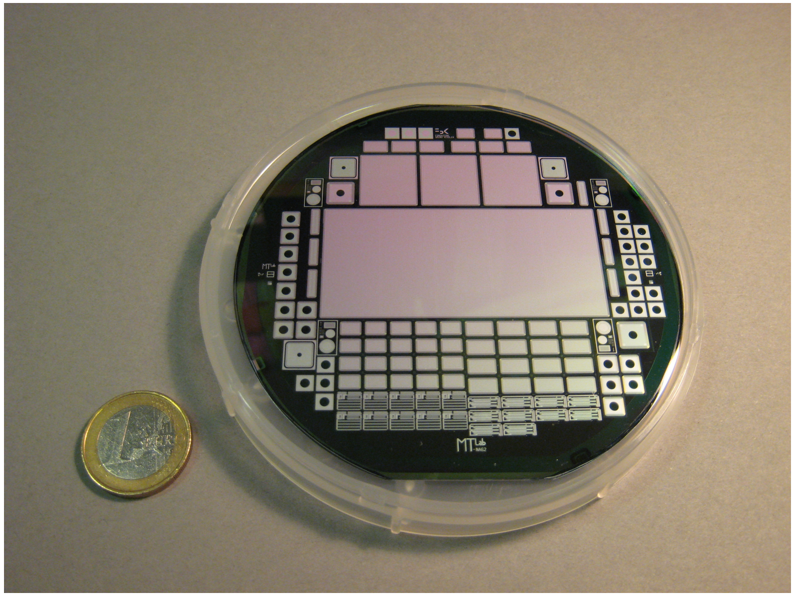
Gigatracker assembly

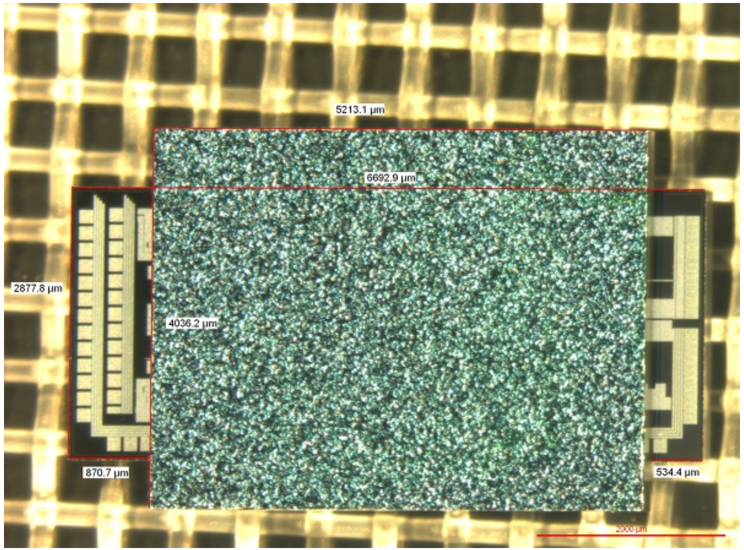
- Hybrid pixel detector
  - 300 μm × 300 μm pixels
  - 1 sensor (60 × 27 mm^2) bump-bonded to 10 read-out chips
- Material budget:
  - 200 μm sensor + 100 μm read-out chip → ~0.32% X_0
  - Bump bonds ~0.01% X_0
  - Mechanical support and cooling ~0.15% X_0
  - **Total** **< 0.5% X_0**
- Minimization of material in active beam area
  - beam profile adapted: two rows of read-out chips
  - wire connections to R/O chip outside active area



Sensors and bump-bonding

- 200 μm thick p-in-n sensors (produced at FBK, Trento, Italy)
- Over-depleted operation of the detector required to achieve target time resolution (300 V over-bias)
  - fast charge collection
- Irradiation of test structures
  - annealing study following expected run scenario

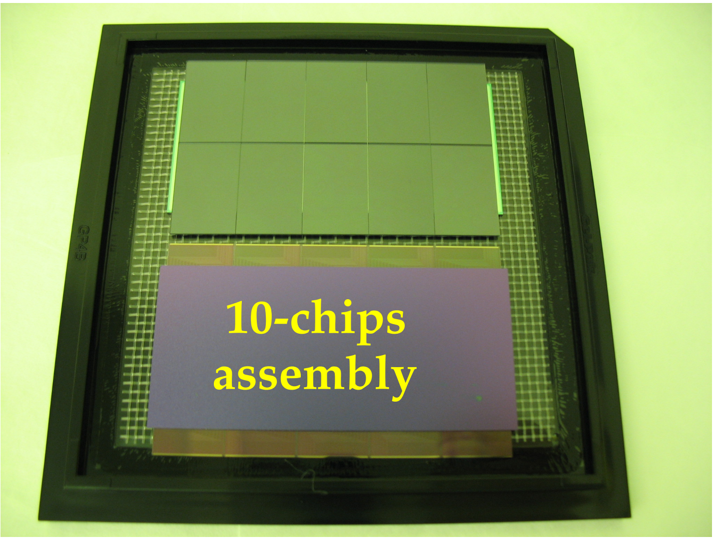


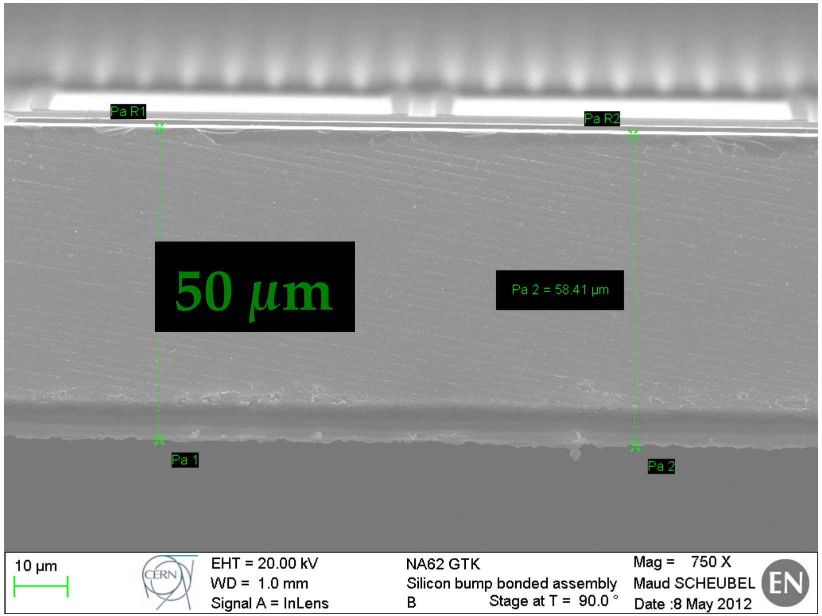


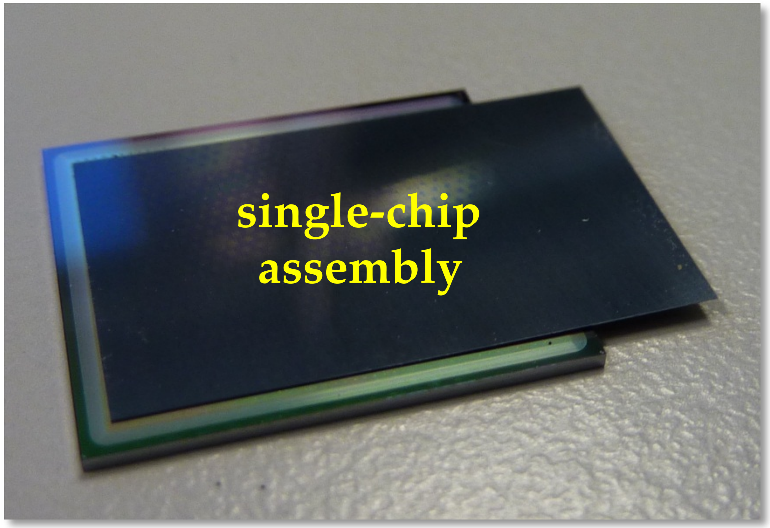
- Flip-chip bonding for prototypes done at IZM (Berlin, Germany)
- Target read-out wafer thickness is <100 μm for final production

Thinned assemblies

- Thinning and bonding studies on dummy components at IZM
  - synergy work with ALICE ITS upgrade
- R/O chip thinned to 50 μm

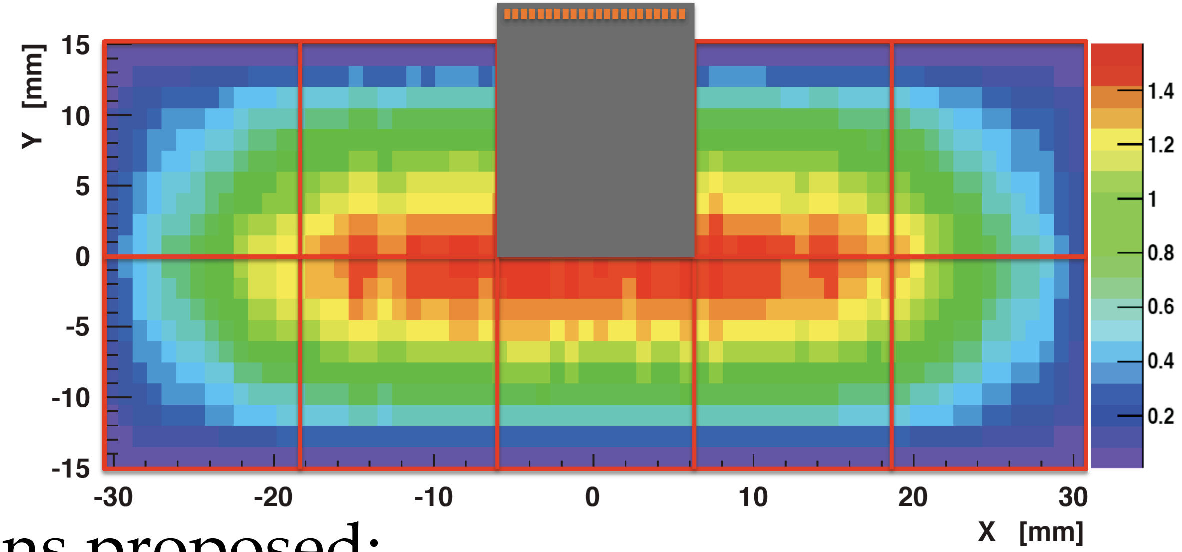






Operating environment

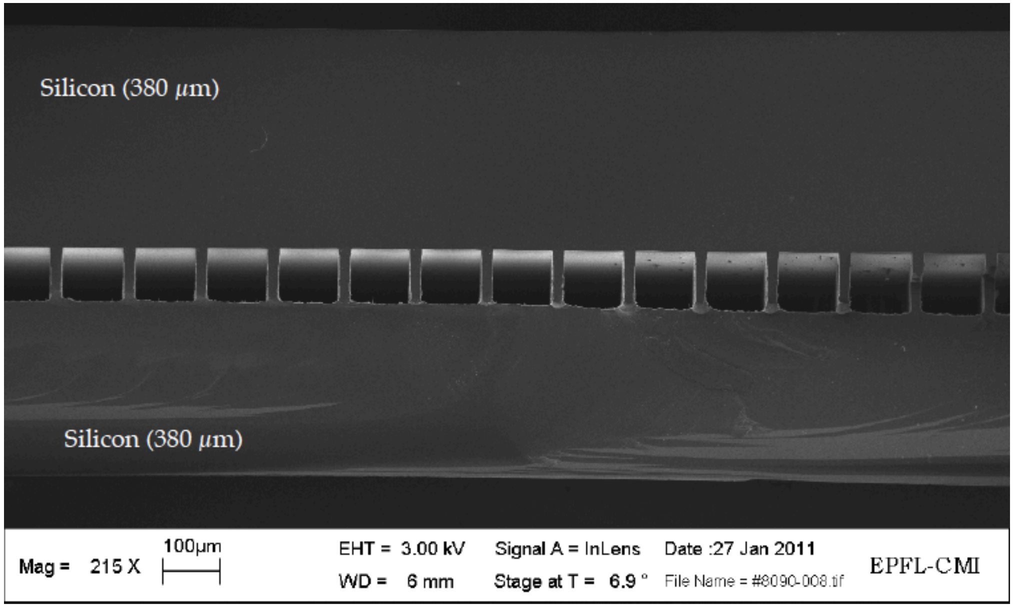
- GTK stations installed in **vacuum**
- High and non-uniform radiation levels
  - expected fluence is ~2×10^{14} (1 MeV n_{eq}/cm^2) during one year of operation (100 days) in the sensor center
- Efficient cooling necessary for stable detector operation
  - Very low material budget (**~0.15% X_0**) in the active beam area

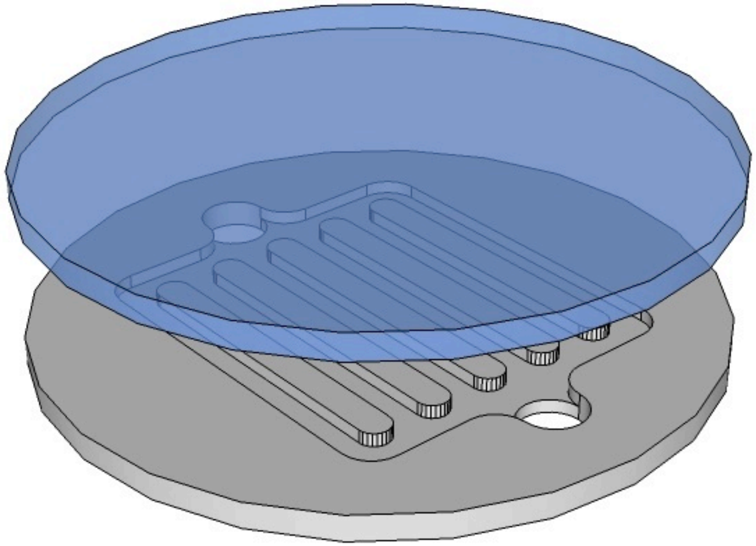


- Two cooling solutions proposed:
  - gas cooling in a vessel and micro-channel cooling
  - mc cooling chosen by the NA62 Collaboration as baseline solution

Micro-channel cooling (1)

- Micro-channel cooling plate: 2 bonded Si wafers (150 μm total thickness in the active detector area)
  - ❑ channels plus opening for inlet and outlet manifolds





- ~(100 μm)^2 micro-channels
- liquid coolant (C_6F_{14})
- full-scale prototype and vacuum test stand built and characterized
  - ❑ manifold optimization to reduce pressure plus wafer thinning

Micro-channel cooling (2)

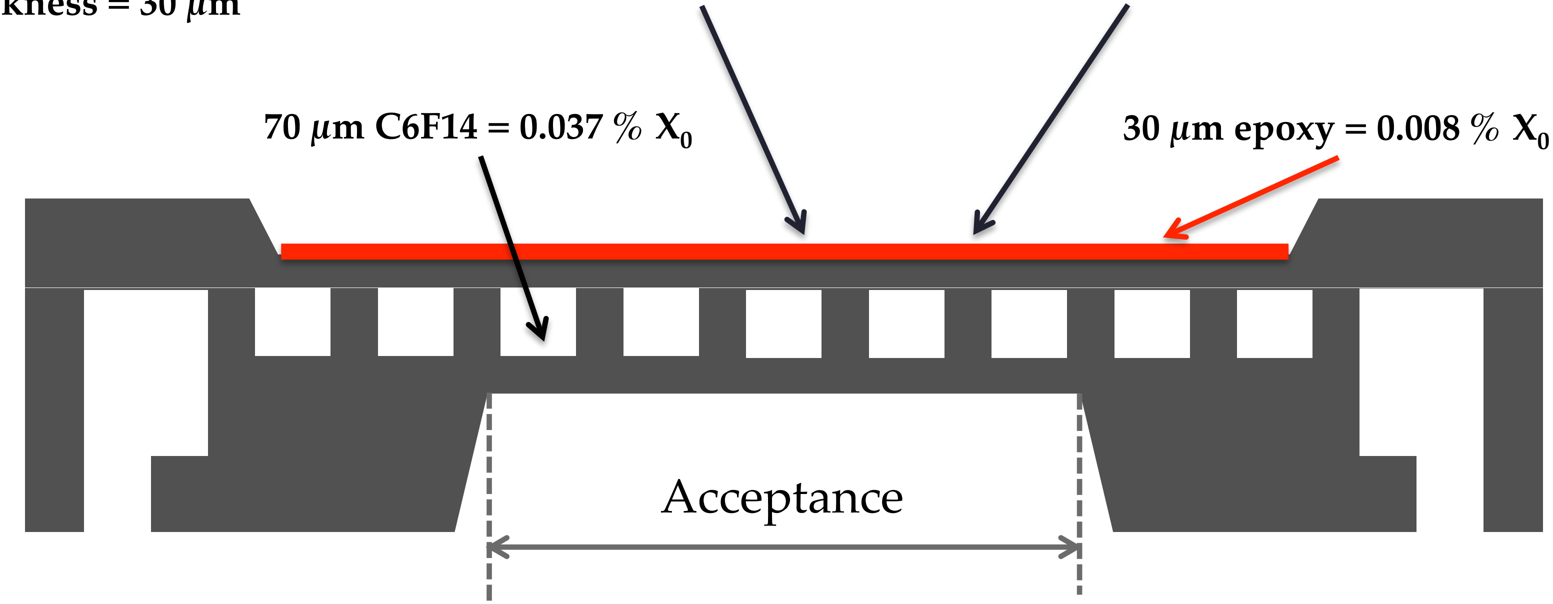
Channels = 200 × 70 μm
Wall thickness = 200 μm
Cover thickness = 30 μm

30 + 30 μm Silicon = 0.064 % X_0
(above and below channels)

30 + 30 + 70 μm Silicon = 0.139 % X_0
(between channels)

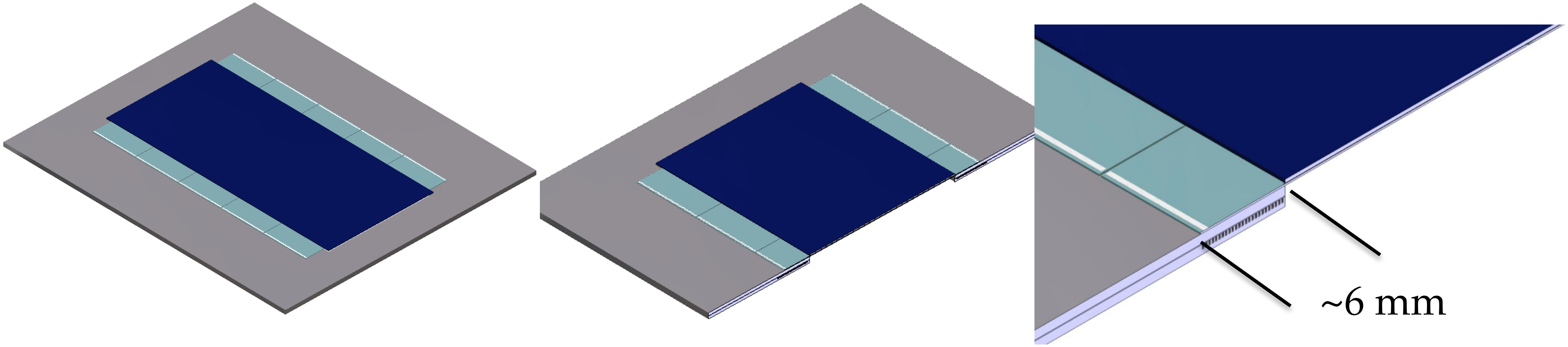
70 μm C6F14 = 0.037 % X_0

30 μm epoxy = 0.008 % X_0

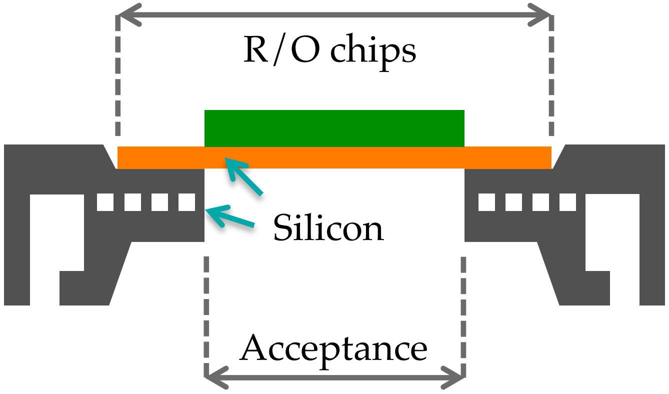


Total material budget in the acceptance area = 0.13 % X_0
(min 0.11% X_0- max 0.15% X_0)

Micro-channel cooling (3)



- Alternative solution: frame with micro-channels for cooling
- No material at all in the active area
- Thermal contact only on read-out chips terminal part (highest power dissipation)
- Relax constraints on R/O thinning



Read-out alternatives

- Time-walk compensation necessary to achieve the required timing resolution (16:1 dynamic range)

“On-pixel” TDC option	**“End of column” TDC option**
CFD filter + on-pixel TDC based on TAC	ToT discriminator + DLL based TDC shared among a group of pixels

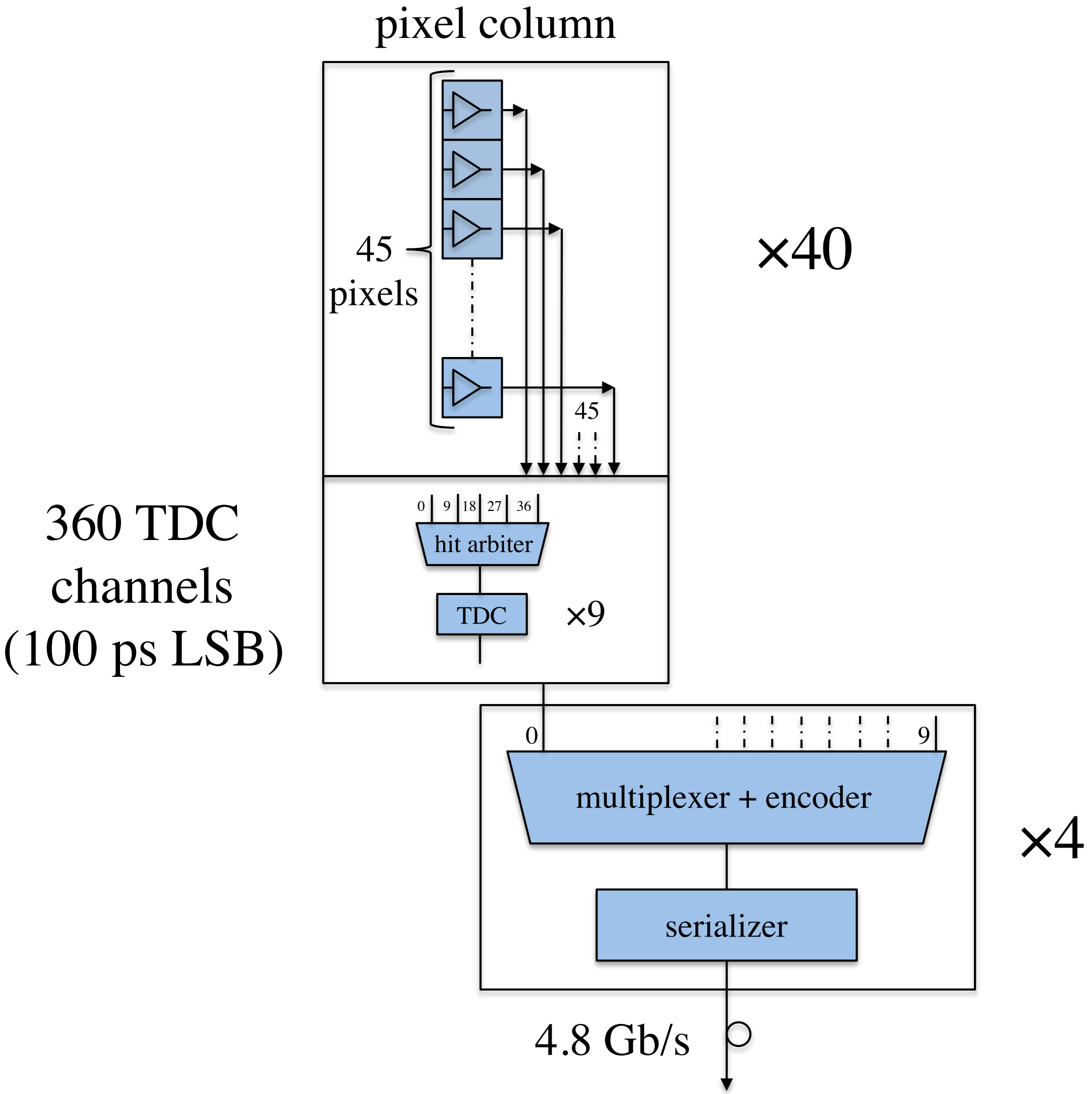
- Small area prototype chips produced in 0.13 μm IBM CMOS technology in 2009, bump-bonded in 2010
- The NA62 Collaboration, after a careful design review, decided to adopt the “End of column” architecture as the baseline option
  - decision based on performance of prototype assemblies and the tight time schedule of the experiment

R/O chip specifications

Pixel matrix	40 columns × 45 pixels
Pixels per chip	1800
Chip size	12 mm × ~19 mm
Dissipated power	~2 W/cm^2
Dynamic range	3600 – 60000 e^- (0.6 – 10 fC)
Expected dose	~10^5 Gy
Time resolution	< 200 ps
Peaking time	5 ns
Efficiency per station	> 99%
Maximum rate per pixel	140 kHz
Maximum rate per chip	130 MHz
Maximum data bandwidth	~8 Gb/s

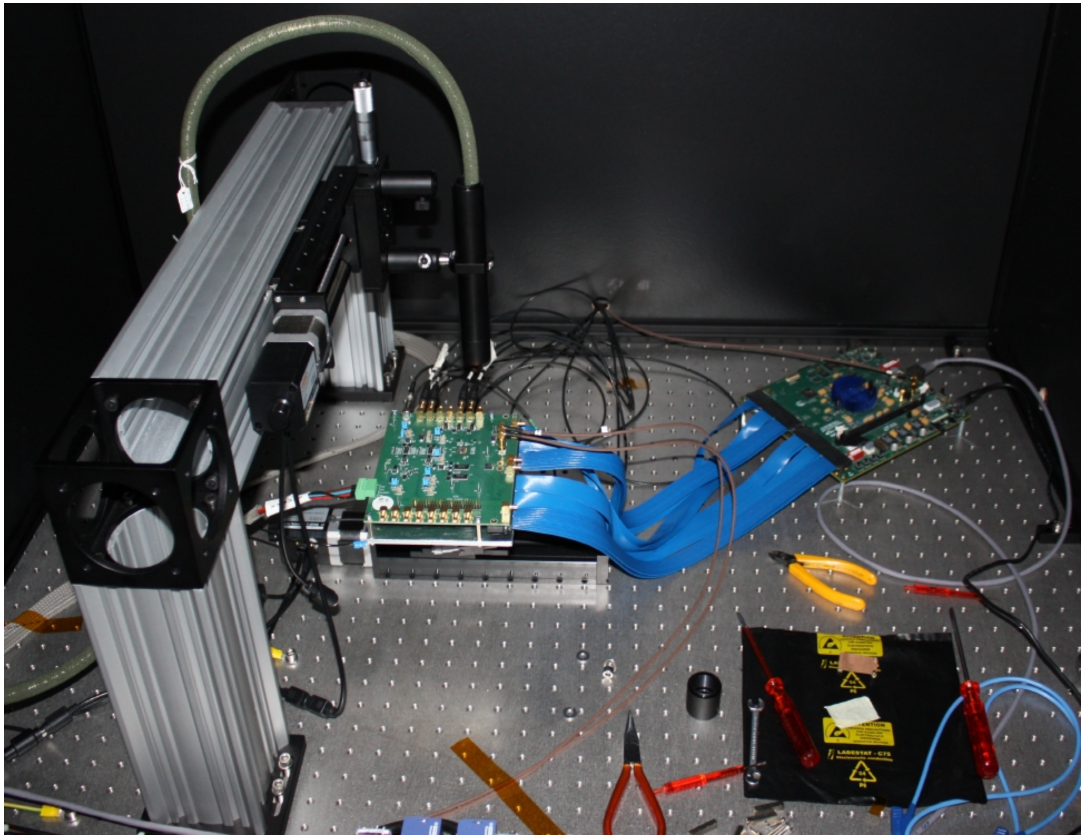
R/O chip architecture

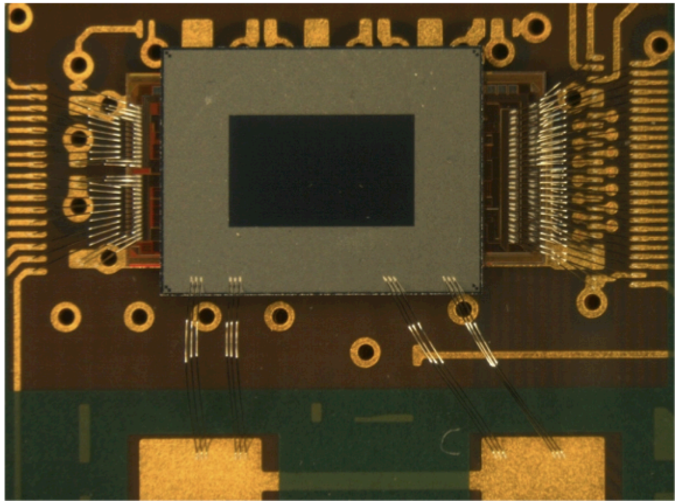
- data driven architecture
- fast preamplifier
- asynchronous transmission lines from pixels
- hit information (address, T1, T2, pileup)
- 4.8 Gb/s serializer (×4)
- triplicated digital logic (SEU protection)
- final chip under design



Laser test setup

- IR light (1060 nm) to mimic minimum ionizing particles
- Characterize GTK bump-bonded assemblies on laboratory bench

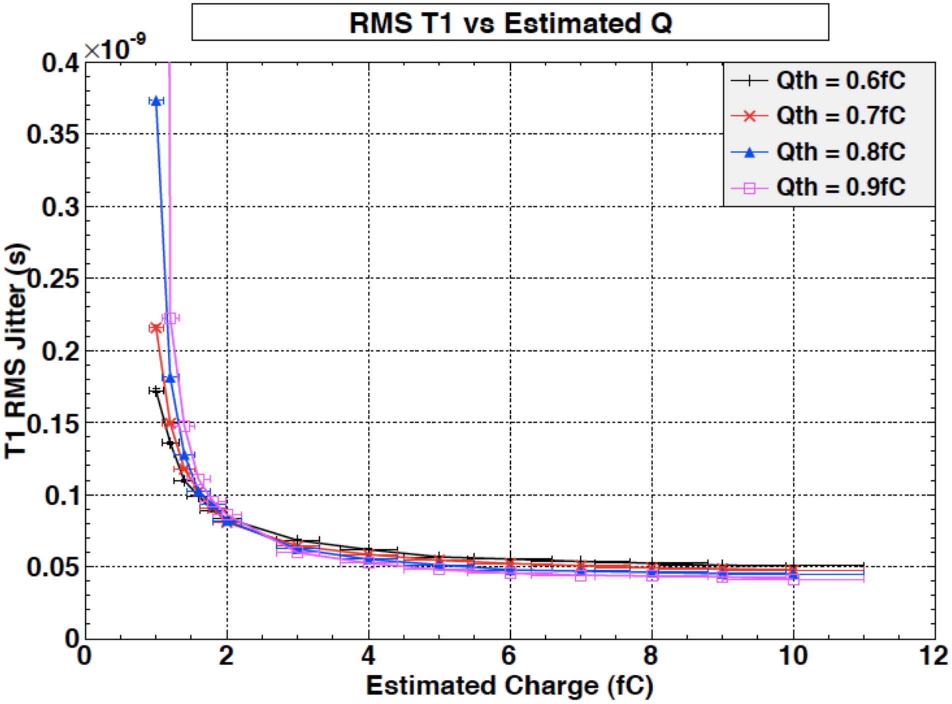


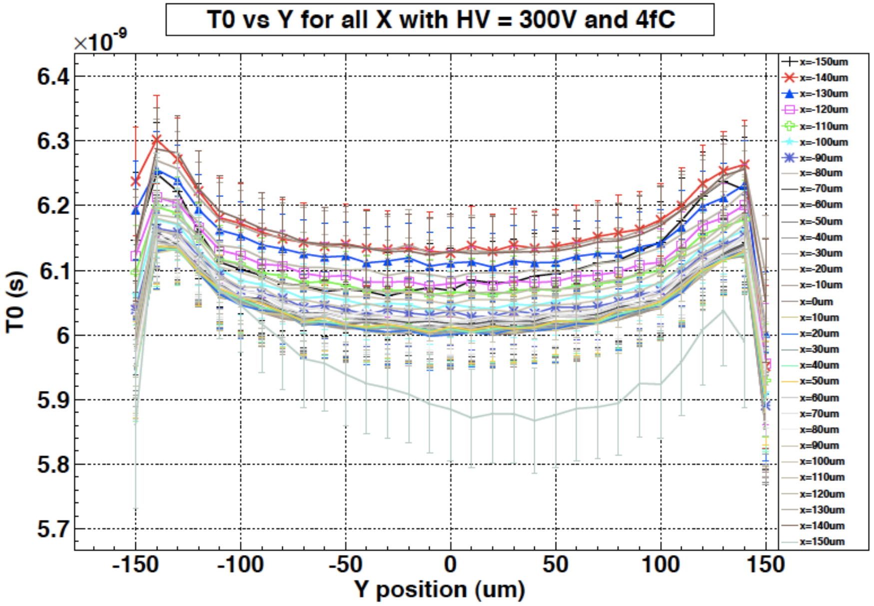


- 5 ps time precision
- Absolute calibration of injected charge
  - radioactive sources (^{241}Am, ^{109}Cd)

Results from laser test

- Time resolution (jitter) of ~75 ps at 3 fC (average charge created by minimum ionizing particle)
  - charge injected at the pixel center

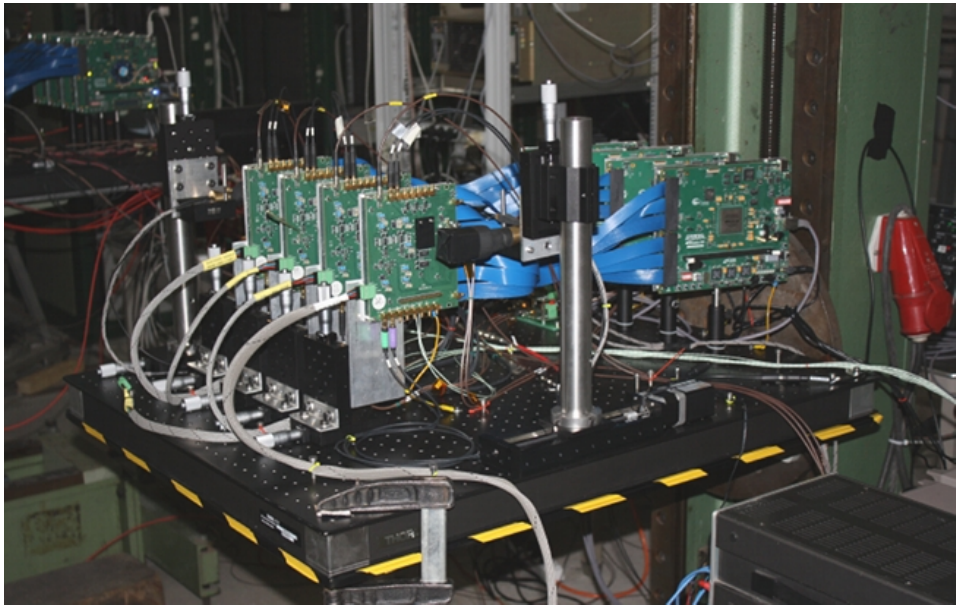


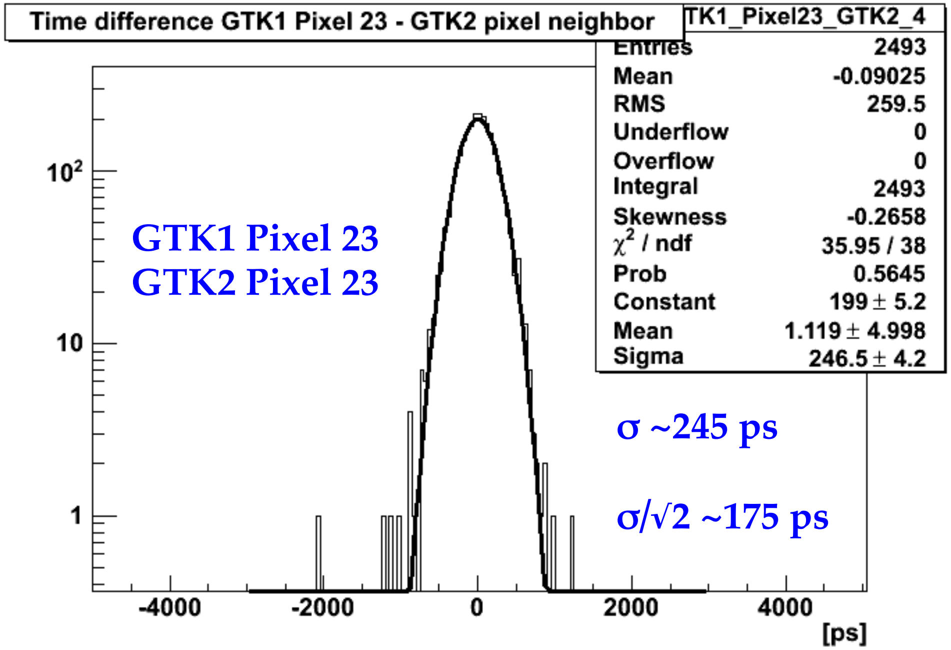


- Precise X-Y scan of pixel matrix
  - variation of measured time with impact position inside pixel
  - geometrical effect (weighting field)

Test-beam at CERN PS

- test-beam at CERN T9 (10 GeV/c π^+ and p)
- 4 consecutive GTK planes
- fast scintillators used for timing reference





GTK1 Pixel 23
GTK2 Pixel 23

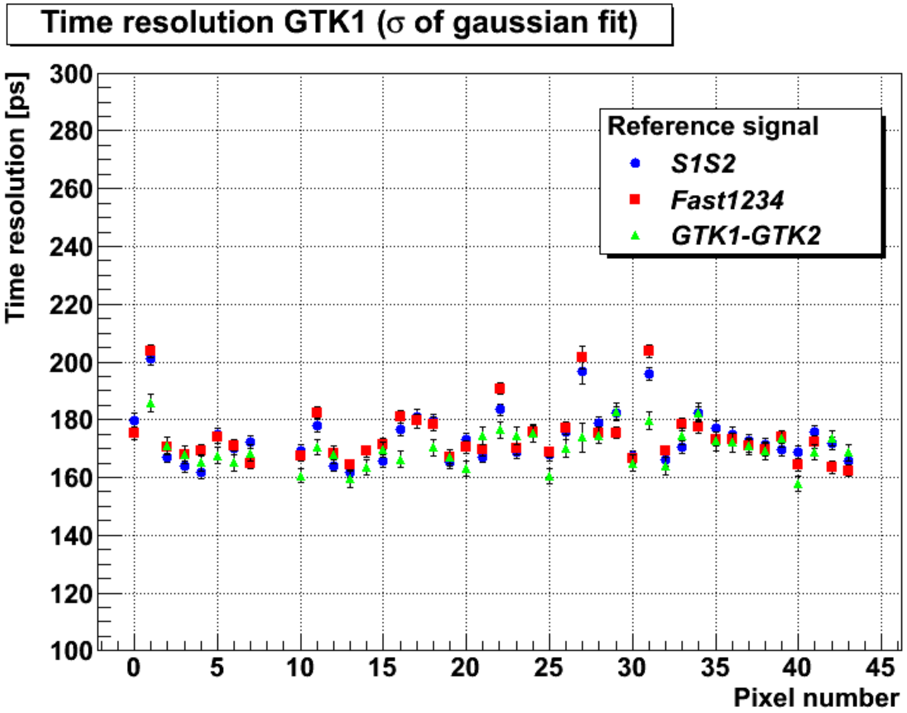
σ ~245 ps

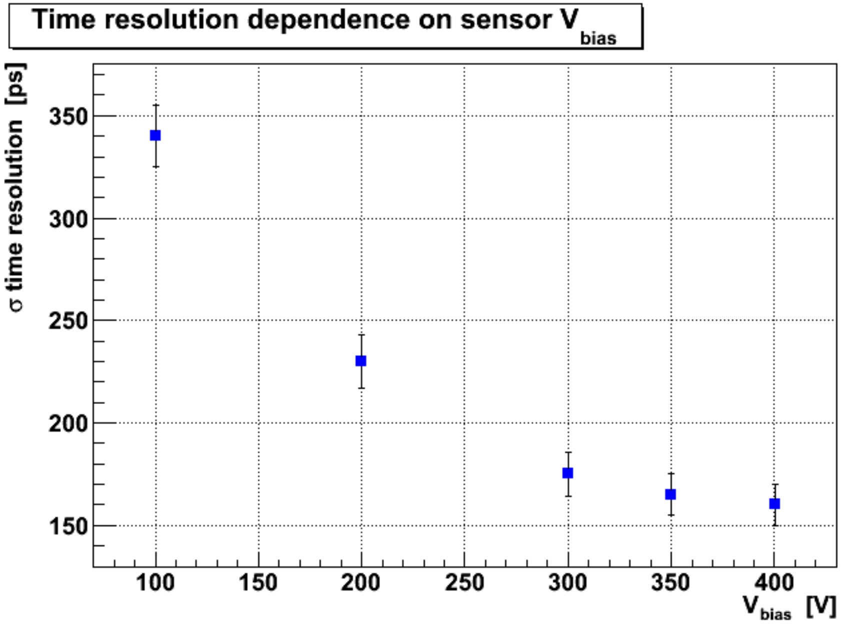
σ/√2 ~175 ps

- applied Time-over-Threshold correction (pixel-by-pixel) using scintillator information
    - procedure validated for NA62
- measured **time resolution of ~175 ps** at 300 V sensor bias

Results from test-beam

- Time resolution measured for every pixel (45 per GTK prototype assembly)
  - variations mainly due to pixel-by-pixel threshold variation (no trimming)





- Clear dependence on sensor bias voltage
  - approaching plateau at ~400 V
  - high-over depletion mandatory

Contributions to σ_{time}

- Electronic noise from front-end chip
  - measured ~180 e^- (ENC) with sensor
- Sensor bias voltage
  - variation of charge collection time (signal slope)
- Impact position on pixel sensor
  - weighting field variation (geometrical effect)
- Energy straggling in the sensor bulk
  - non-uniform energy release along track and delta rays
- Alternative sensor technologies under consideration for possible improvements
  - 3D sensors could be advantageous for time resolution (will be tested with prototype assemblies)

Conclusions

- Excellent timing performance has been obtained on very thin hybrid pixel detectors (200 μm sensor)
  - a time resolution of ~175 ps has been measured with minimum ionizing particles at 300 V bias voltage (~160 ps at 400 V)
  - strong dependence of time resolution on sensor bias has been verified
- An innovative and very-low mass cooling system (<0.15% X_0) is under construction
  - micro-channel cooling plate as baseline option for NA62
  - alternative solution (frame structure) looks promising

SPARES

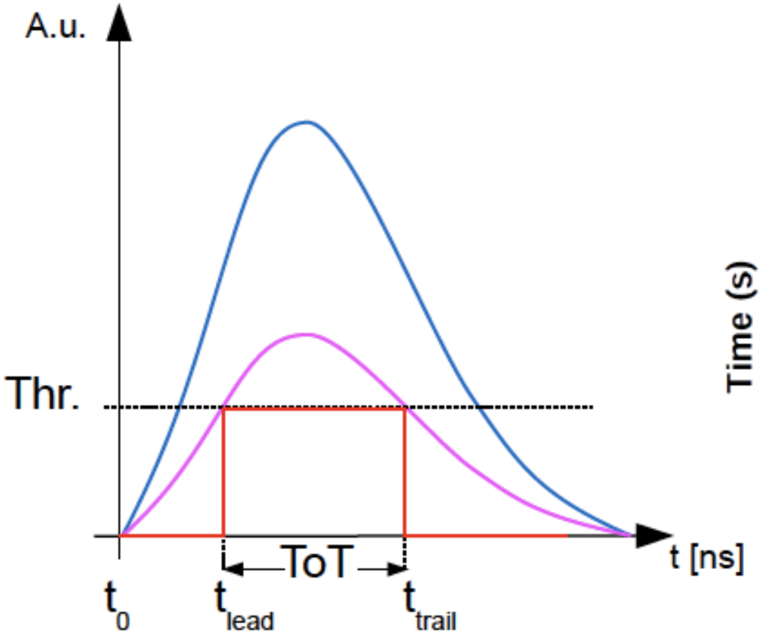
Time-walk

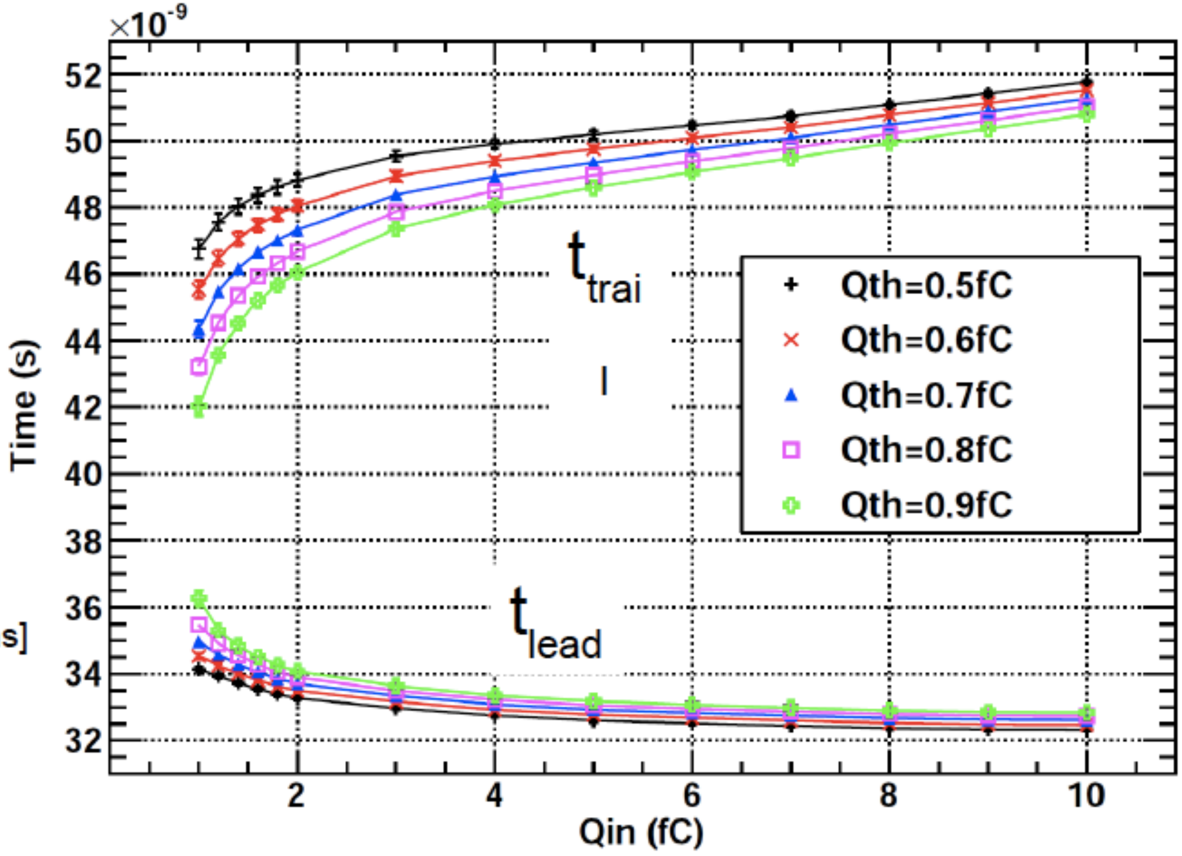
- To achieve the required timing accuracy, time-walk compensation has to be applied due to the 16:1 dynamic range

Two alternatives considered:

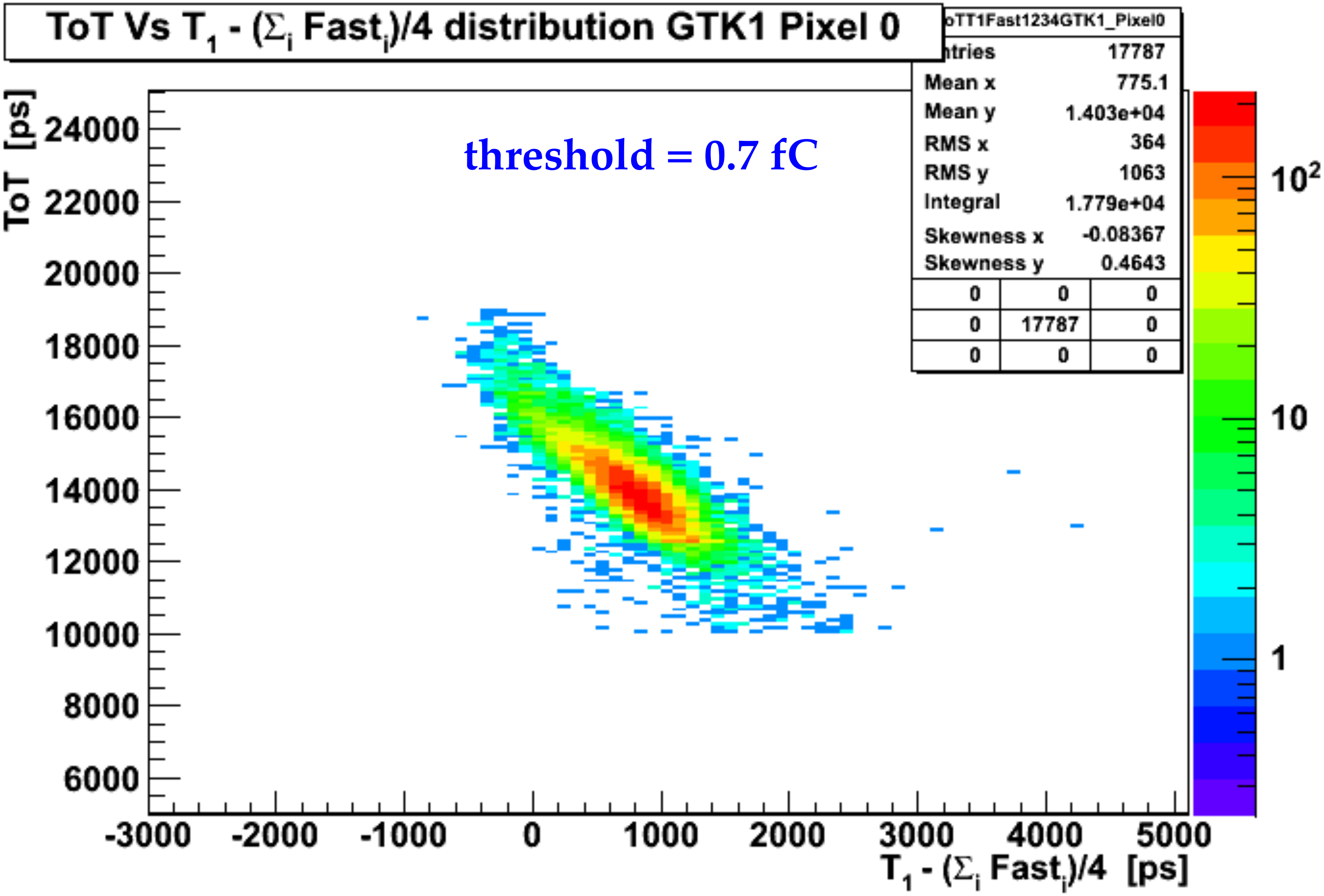
- Use of a low power Constant Fraction Discriminator (CFD)
  - analog signal processing technique of time information without time-walk
  - single time measurement, complicated analog design
- Correction via the Time over Threshold (ToT) method
  - time-walk correction algorithm based on the signal time over threshold (pulse width), obtained by measuring leading and trailing edges of the pulse
  - accurate calibration of the system is required to define the correction algorithm

Time-walk measurement





Time-walk correction



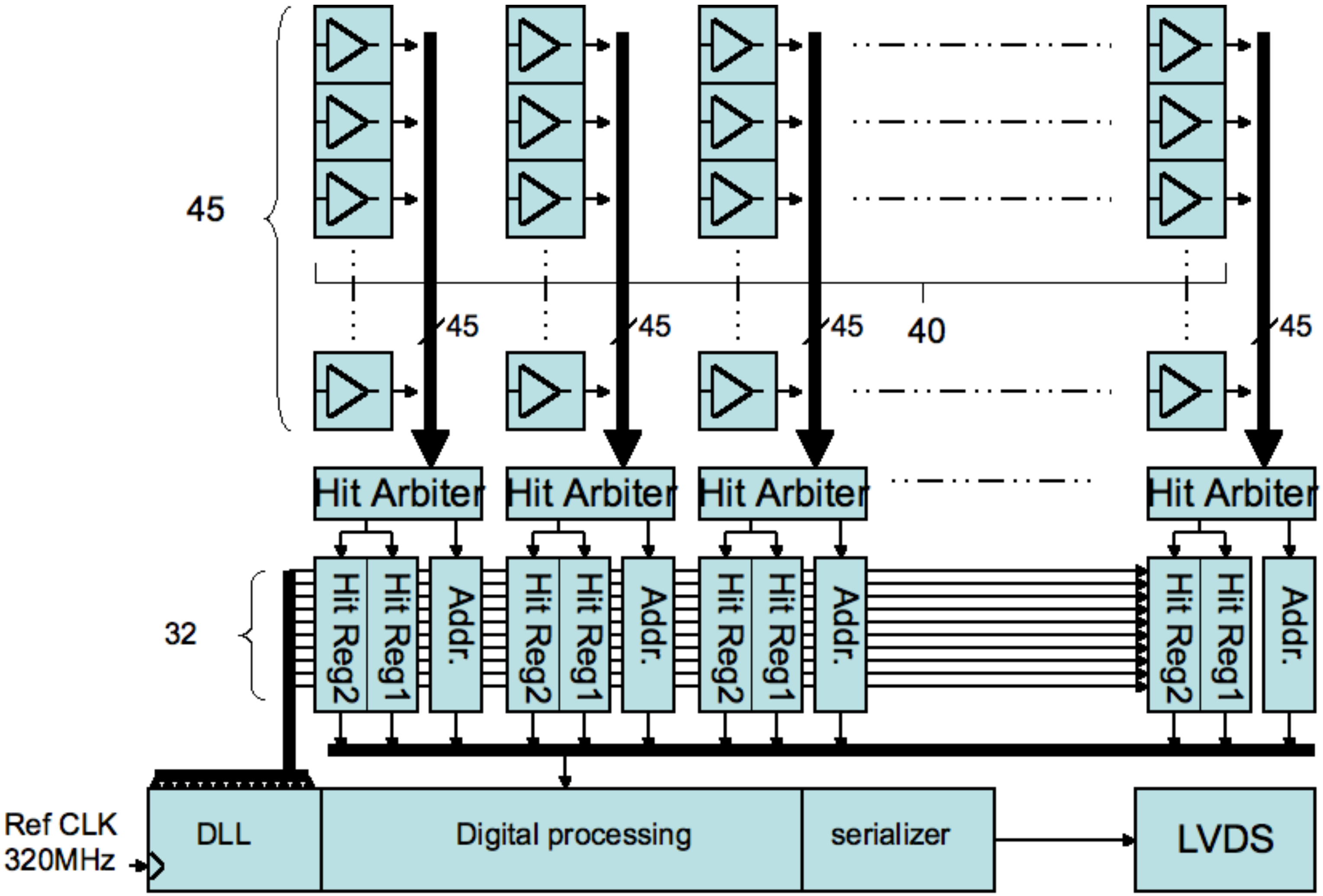
TDC options

- Coarse time measurement by counting clock pulses
- Fine measurement obtained with a Time to Digital Converter (TDC)

Two possible solutions:

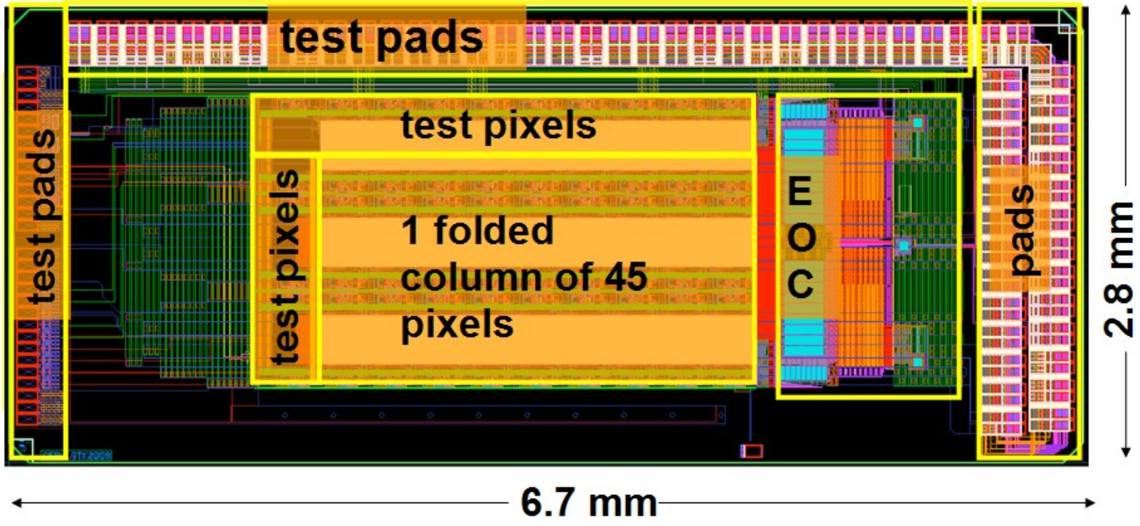
- On-pixel TDC system
  - maximize signal processing on the pixel cell (including TDC) and distribute clock to the pixel matrix (digital noise)
  - minimize complexity of end of column logic (no need to propagate the comparator signal outside the pixel)
  - must be designed to be radiation-tolerant (total dose and SEU aspects), due to the high radiation dose received in the pixel area
- End of Column (EoC) architecture
  - use high precision digital TDC in the end of column, shared by a group of pixels
  - minimize on-pixel processing for minimum noise
  - pixel comparator signals should be propagated to the chip periphery (communication of ultra-fast signal in column transmission lines)

EoC architecture

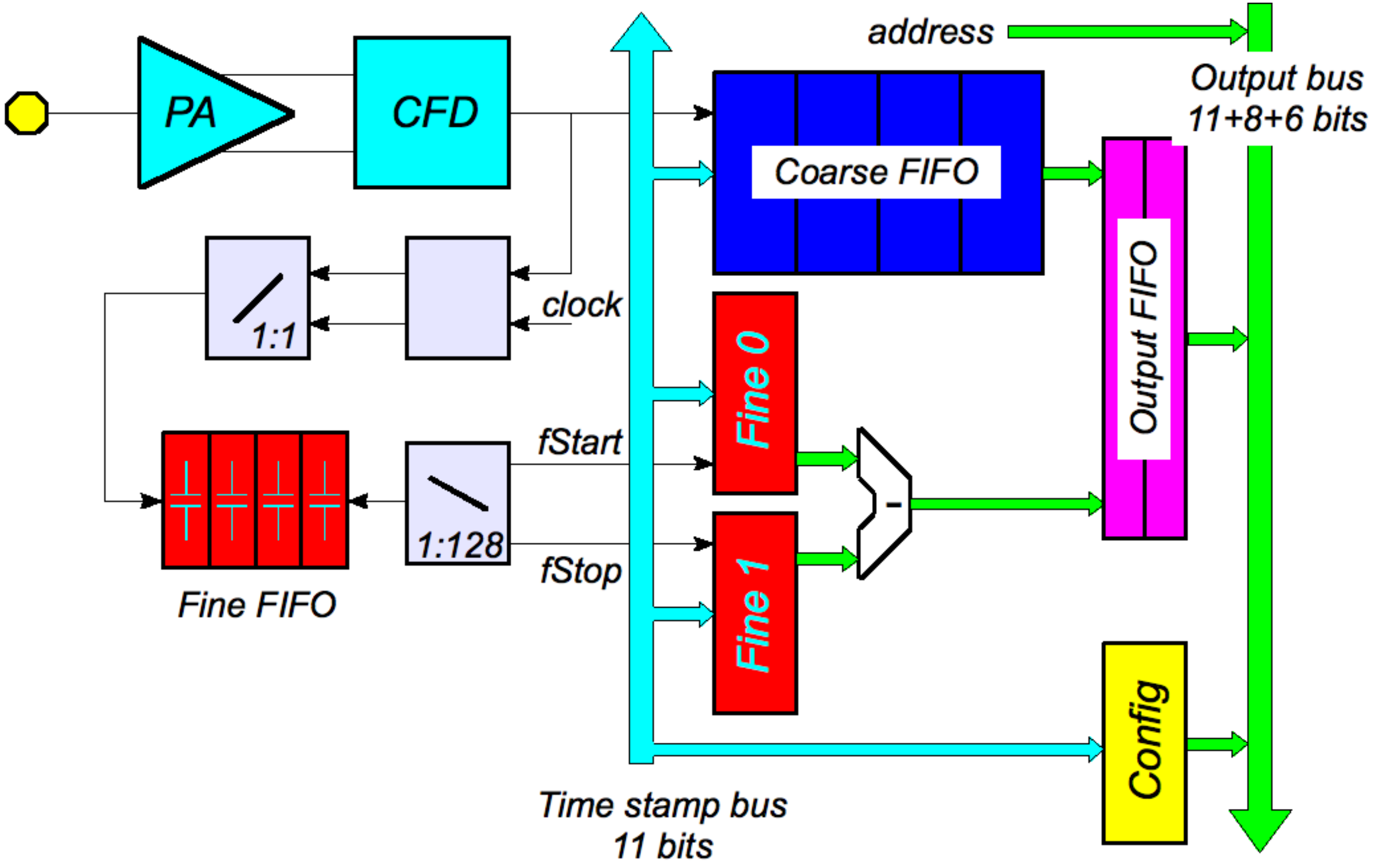


EoC Prototype

- 2.8 mm × 6.7 mm total size
- 320 MHz reference clock
- 60 pixels divided into 3 groups
- Main array: 45 pixels with 9 EoC readout blocks, each one serving the 5 pixels through the arbiter block
- Small array: 9 pixels
- Test column: 6 pixels with analog output
- Hit Arbiter: defines first arriving pixels out of 5 (asynchronous latch)

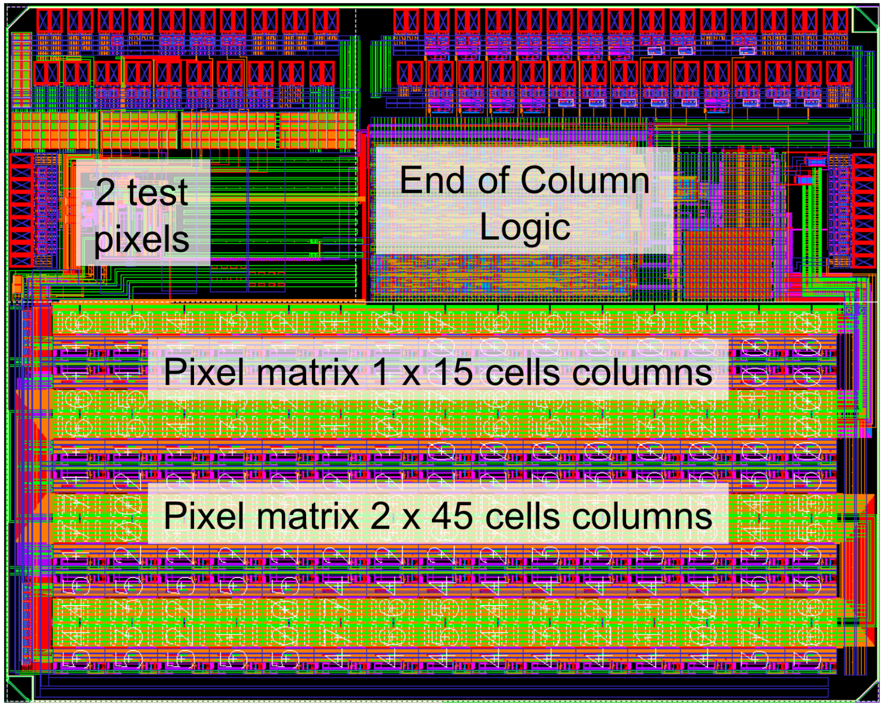


On-pixel architecture



On-pixel Prototype

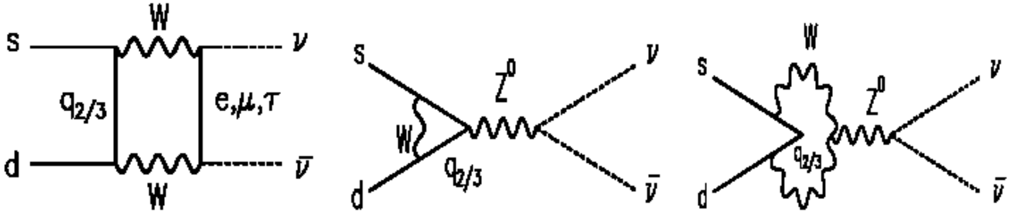
- 5 mm × 4 mm total size
- 105 + 2 pixel cells
- 160 MHz clock
- 2 folded columns (45 pixels each) and one smaller column with 15 pixels, plus two test pixels
- For each column a totally independent End-of-Column Controller is implemented



- SEU protection both in the pixel cells and the End of Column controller
- Fine time measured by starting calibrated voltage ramp at CFD rising edge and stopping at next clock rising edge

The $K^+ \rightarrow \pi^+ \nu\bar{\nu}$ decay

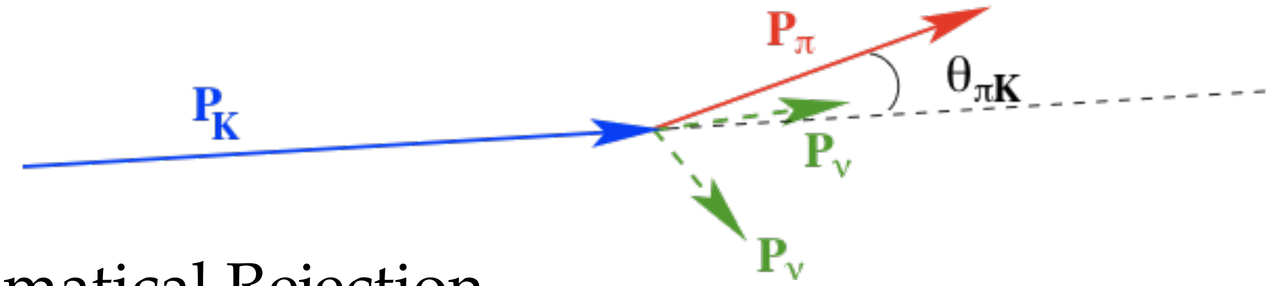
- FCNC loop processes



- Theoretically very clean: hadronic matrix element can be related to measured quantities
- SM predictions (uncertainties from CKM elements):
  - BR($K^+ \rightarrow \pi^+ \nu\bar{\nu}$) ≈ $(1.6\times10^{-5})|V_{cb}|^4[\sigma\eta^2+(\rho_c-\rho)^2]$ → **$(8.5 \pm 0.7)\times10^{-11}$**
  - BR($K_L \rightarrow \pi^0 \nu\bar{\nu}$) ≈ $(7.6\times10^{-5})|V_{cb}|^4\eta^2$ → **$(2.6 \pm 0.4)\times10^{-11}$**
- The $K \rightarrow \pi\nu\bar{\nu}$ decays represent a theoretically clean environment sensitive to new physics

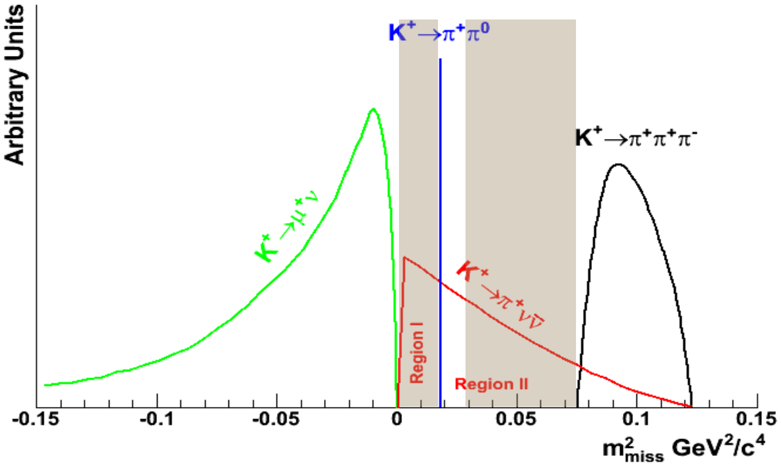
- The NA62 Collaboration (former NA48) aims to measure $\mathcal{O}(100)$ $K^+ \rightarrow \pi^+ \nu\bar{\nu}$ events with ~10% background at the CERN SPS in two years data taking period

Principle of the experiment



- Kinematical Rejection

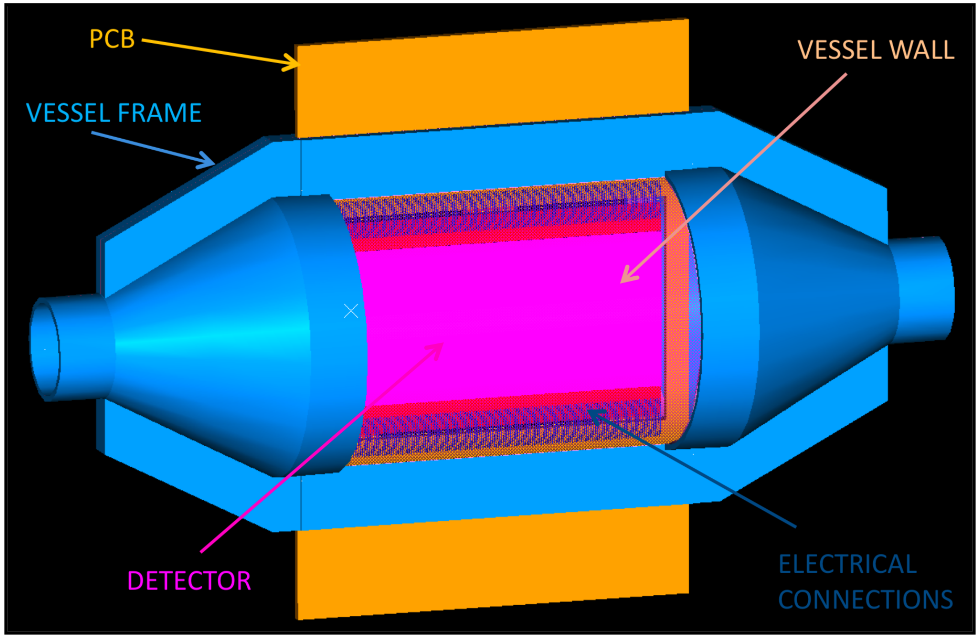
$$m^2_{miss} \approx m^2_K\left(1-\frac{|P_\pi|}{|P_K|}\right)+m^2_\pi\left(1-\frac{|P_K|}{|P_\pi|}\right)-|P_K||P_\pi|\vartheta^2_{\pi K}$$

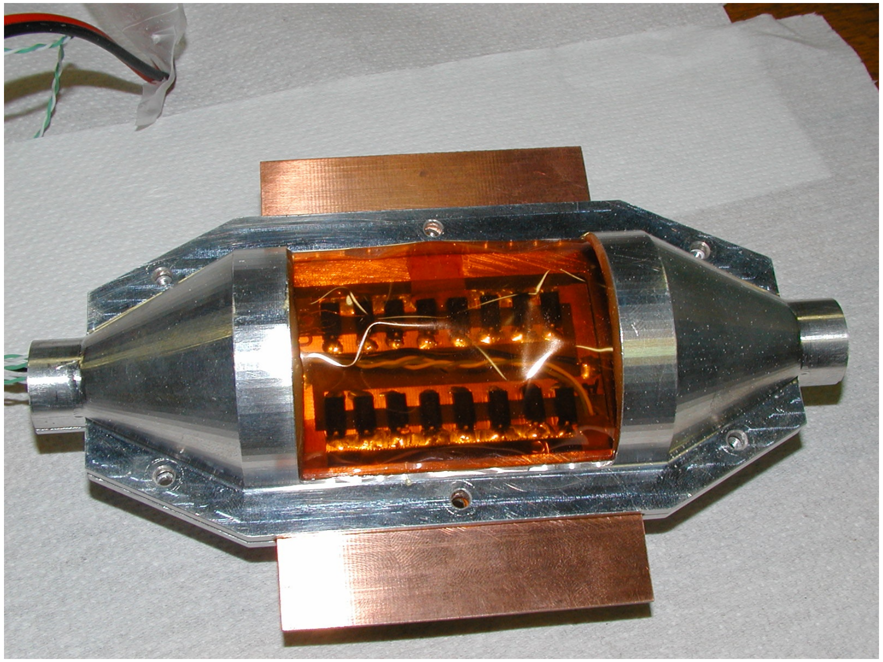


- Photon vetoes to reject $K^+ \to \pi^+\pi^0$
  - $p(K^+) = 75$ GeV/c
  - Requiring $p(\pi^+) < 35$ GeV/c
  - $p(\pi^0) > 40$ GeV/c
    It can hardly be missed in the calorimeters
- PID for $K^+ \to \mu^+\nu$ rejection

Gas cooling

- cooling via flow of cold gaseous nitrogen (100 K)
- thin cylindrical kapton windows (100 μm total)
- aluminum vessel frame

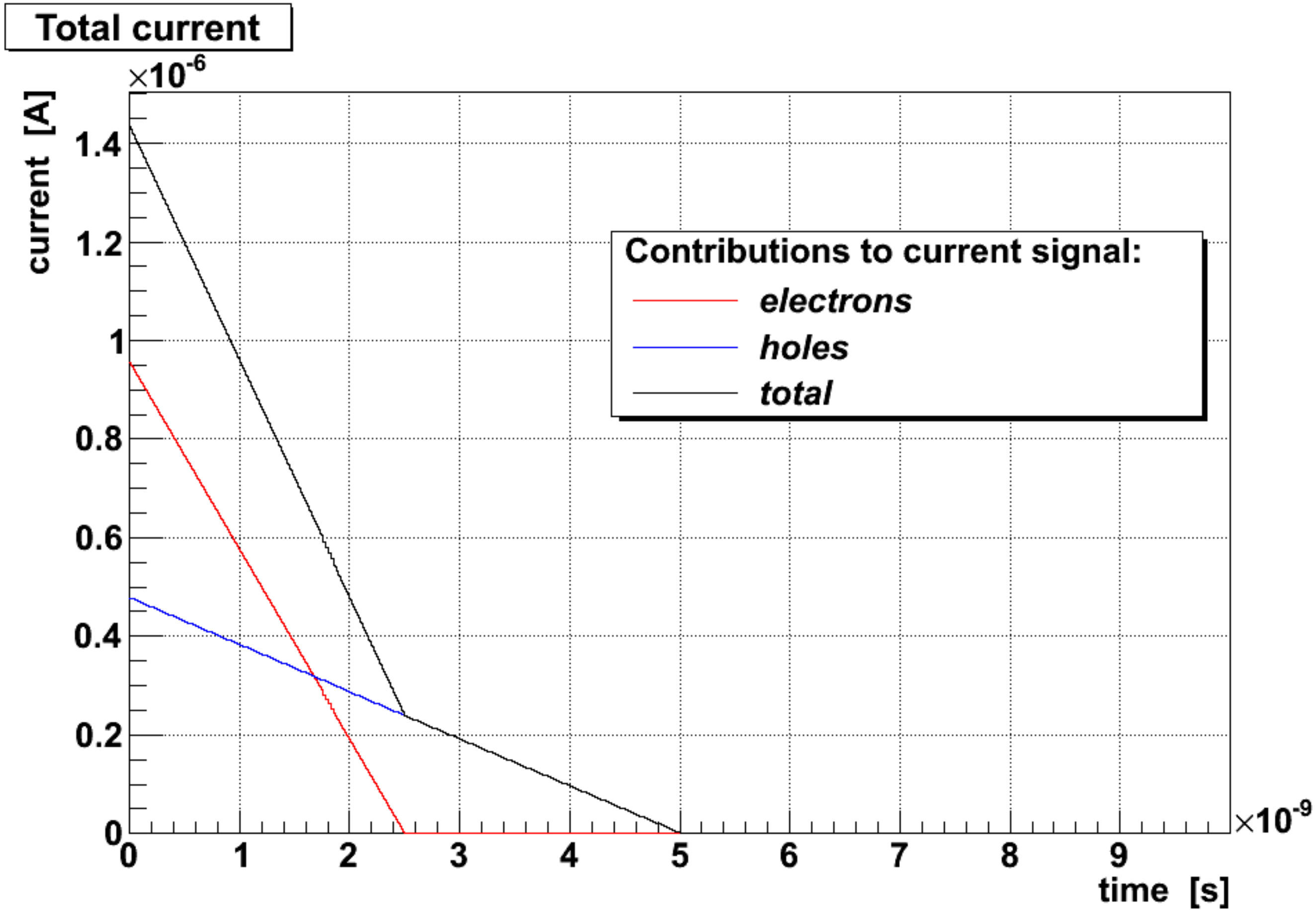




- full size prototype built
- optimization to improve uniformity of temperature distribution across sensor area

Signal formation

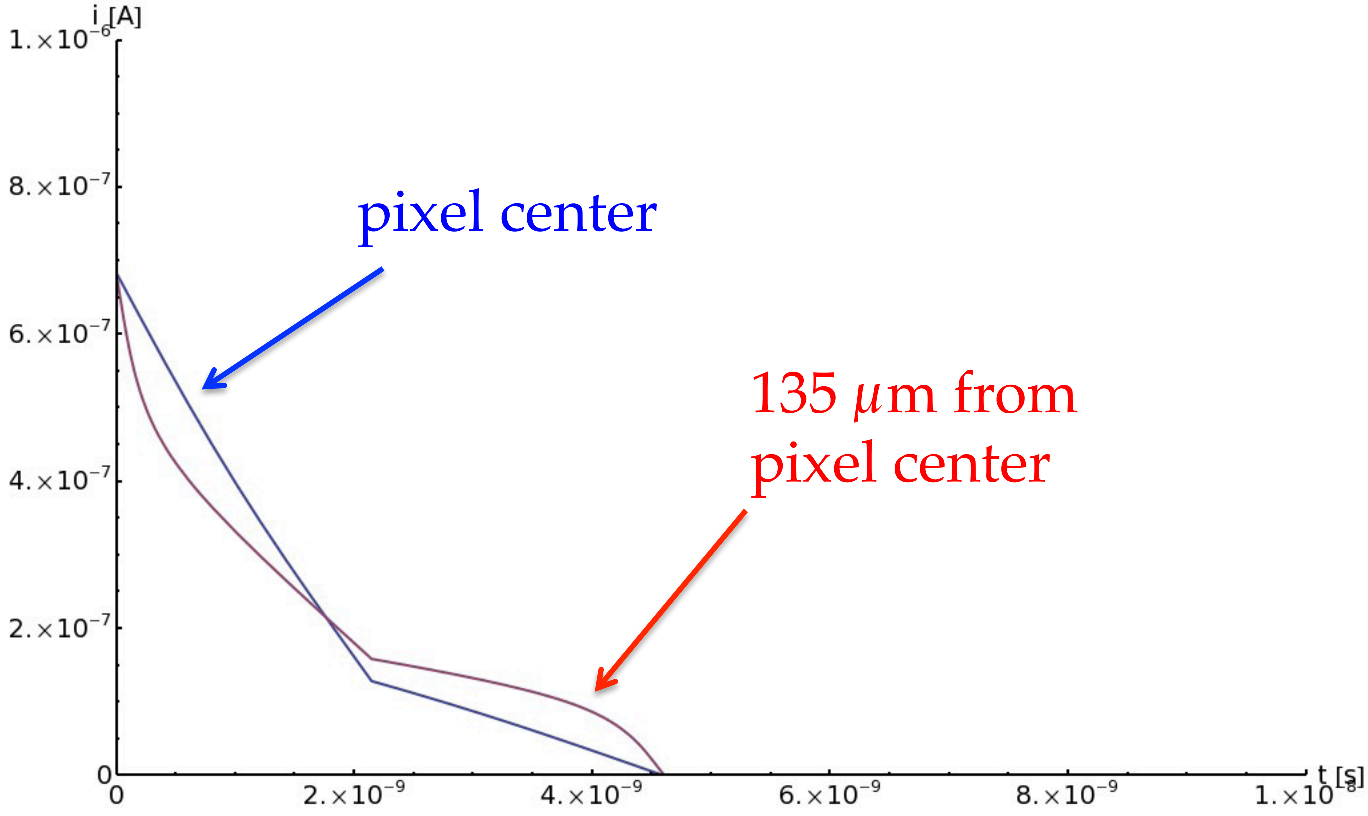
- Ramo-Shockley theorem applied
  - $i = q\,\mathbf{v} \bullet \mathbf{E}_w$



- uniform release of 2.4 fC along the sensor thickness
- charge is divided in 200 layers (1 μm each)

Weighting field effect (1)

- uniform release along the sensor thickness
- injection at the pixel center and close to the edge (135 μm from center)

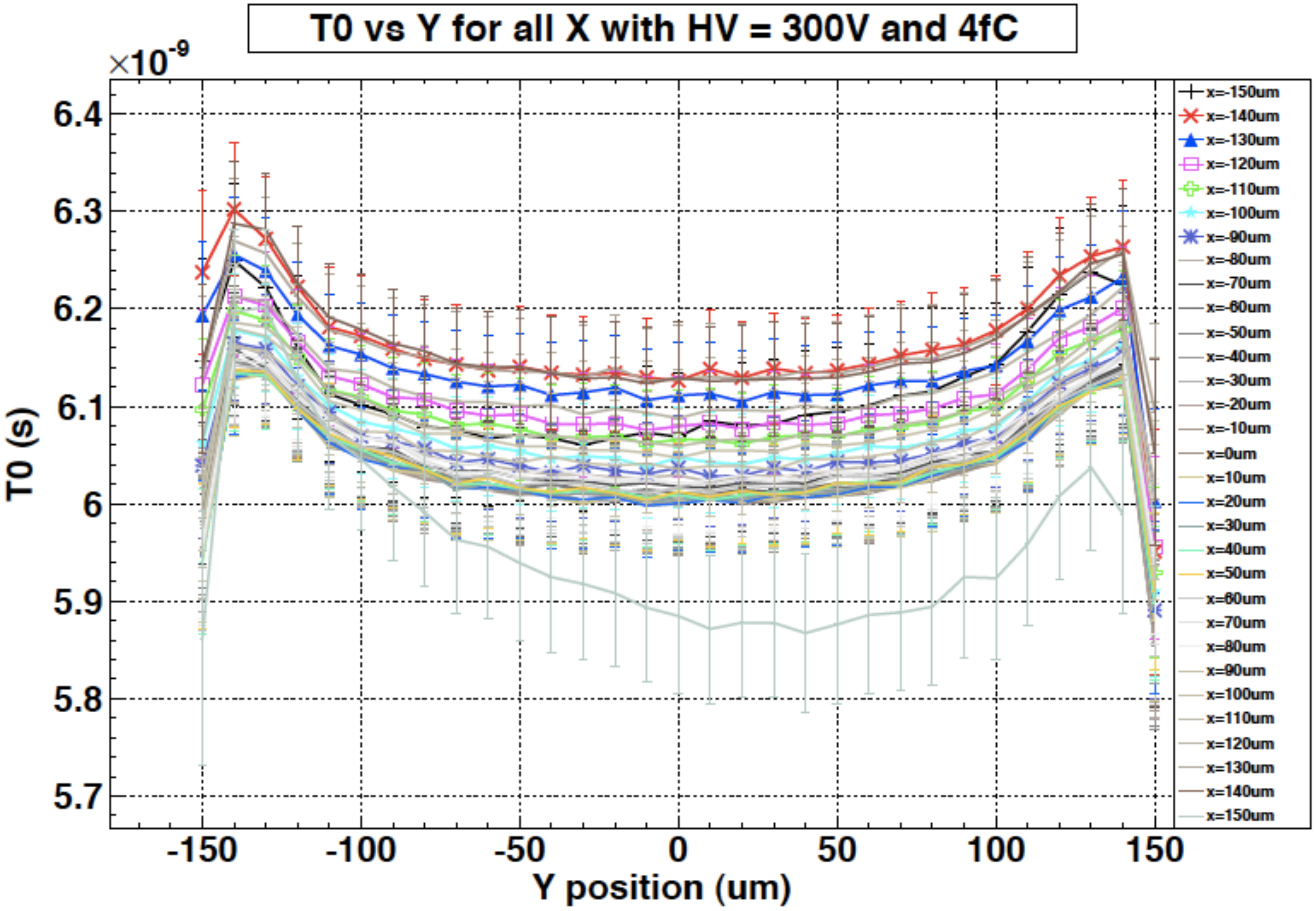


pixel center

135 μm from pixel center

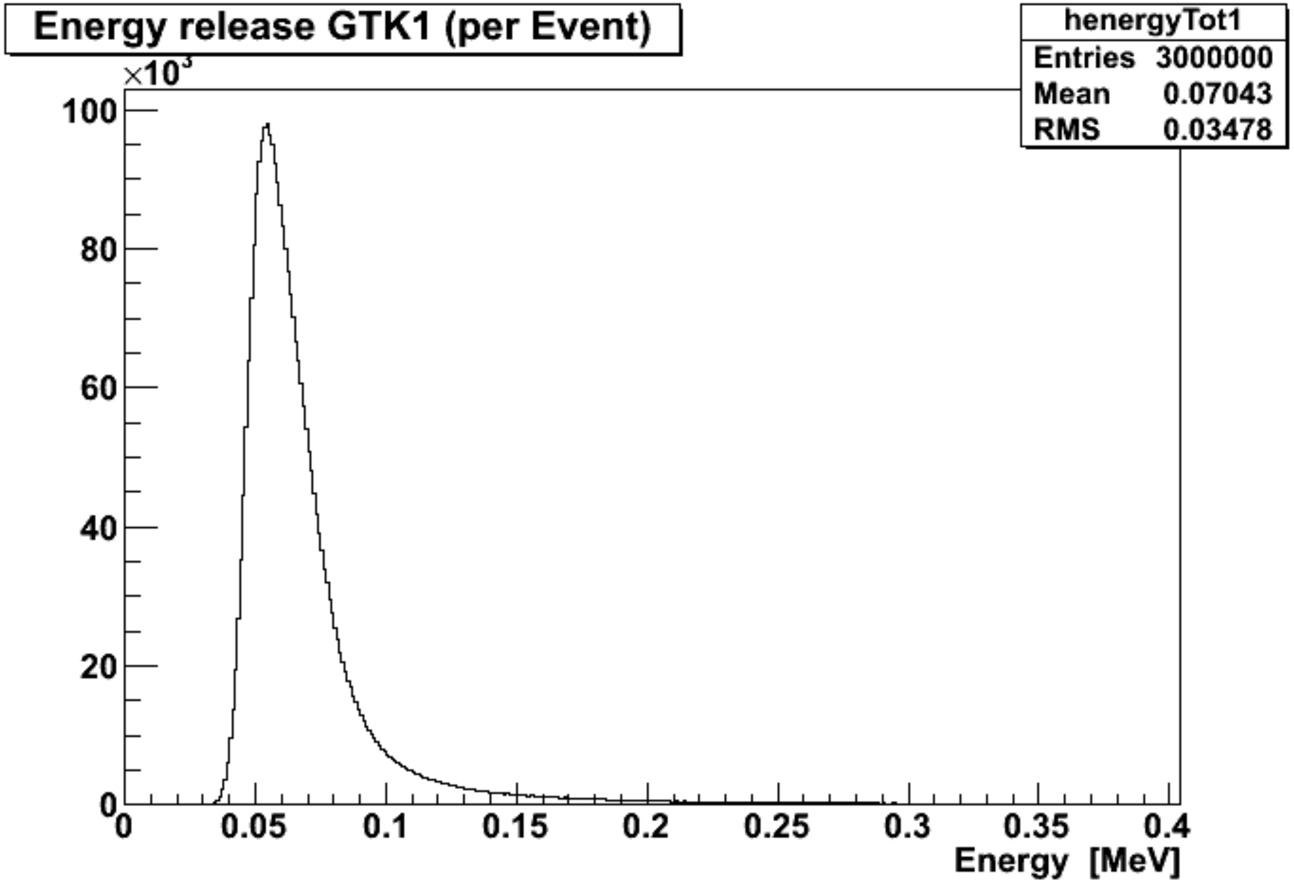
Weighting field effect (2)

- Precise X-Y scan of pixel matrix with laser charge injection
  - ❑ variation of measured time with impact position
  - ❑ geometrical effect
  - ❑ ToT correction



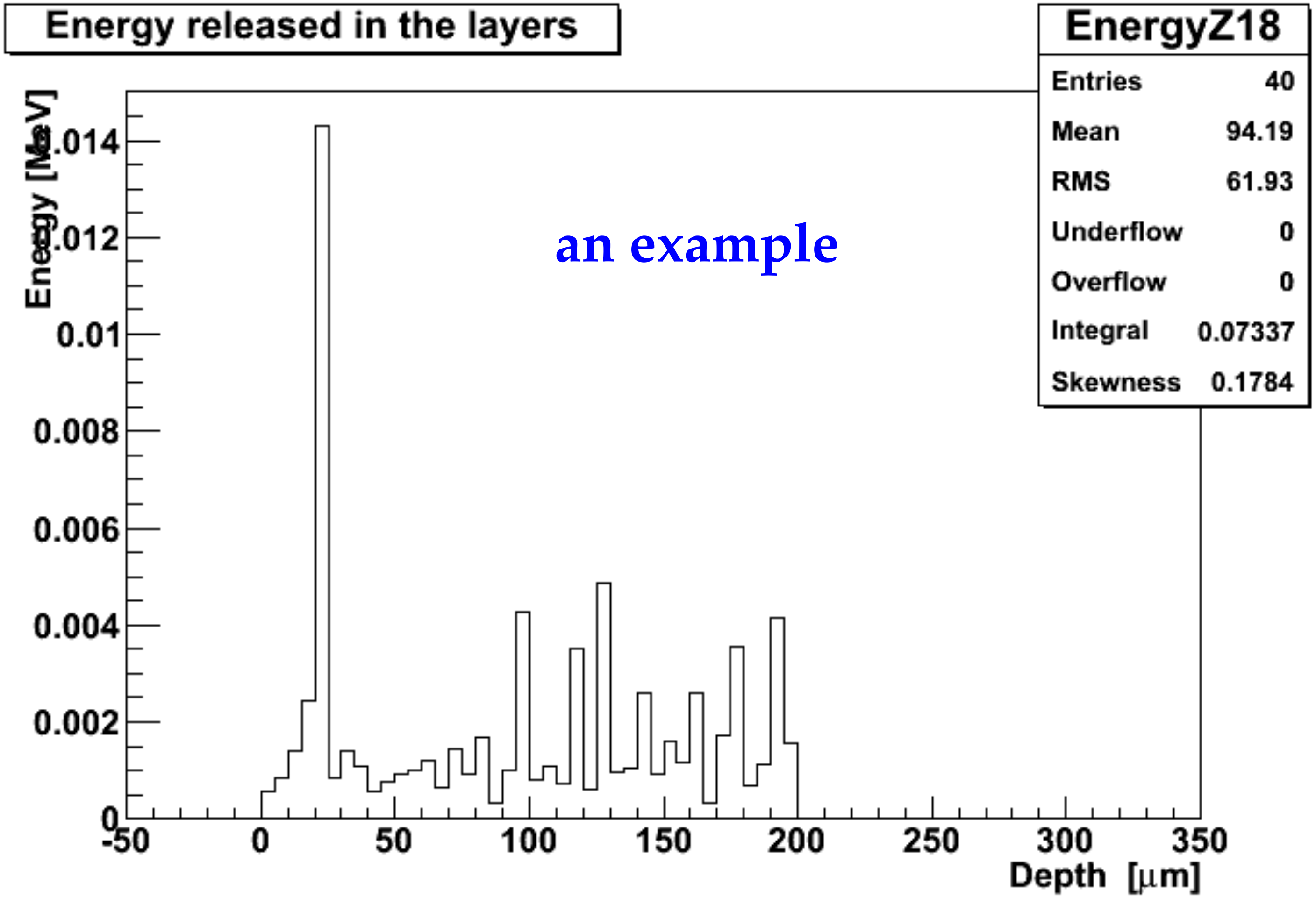
Energy deposited

- Simulation of energy deposited in 200 μm silicon
  - GEANT4
- mean energy: 72 keV (~20 k e-h) → 3.2 fC
- most probable energy: 54 keV (~15 k e-h) → 2.4 fC



Energy straggling (1)

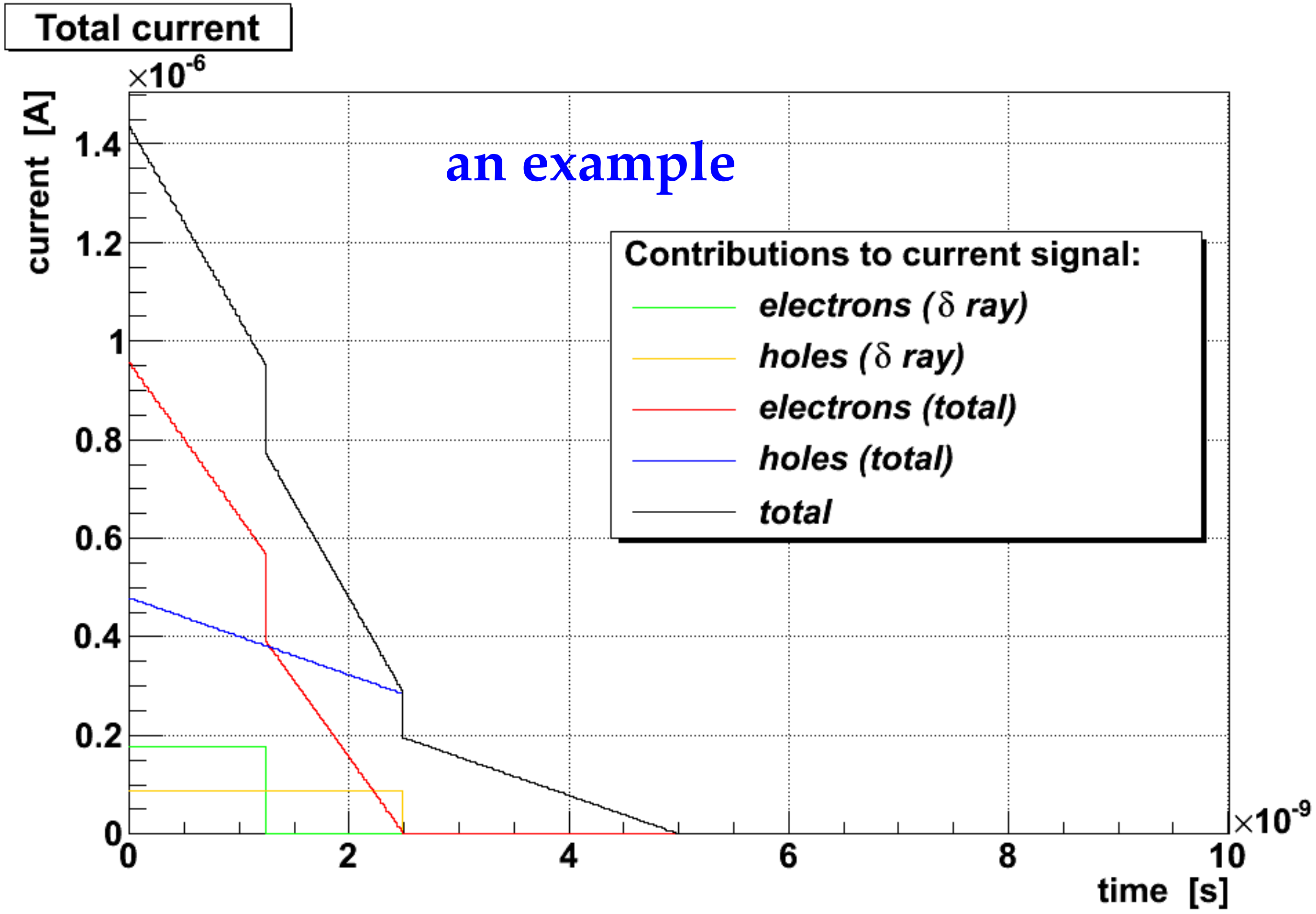
- Energy released as a function of depth in silicon
- 200 μm thick silicon divided in 40 layers (5 μm each)
  - GEANT4



an example

Energy straggling (2)

- total charge release of 54 keV (2.4 fC)
- one δ ray emitted at 100 μm
- δ ray energy is 10 keV (~0.4 fC)



an example