Silicon Buried Channels for Pixel Detector Cooling

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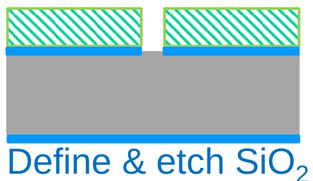
Introduction

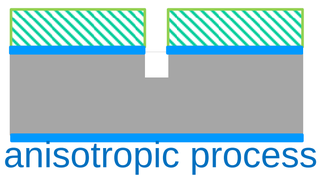
In High Energy Physics experiments pixel detectors require a cooling system with a high heat-exchange efficiency in order to evacuate the power dissipated in the active region by the front-end electronics.
To minimize the material budget, the innovative idea is to integrate into the silicon itself a cooling system, based on microchannels made by DRIE technology. The embedded microchannels feature a peculiar geometry: in the final step a thin oxide layer is deposited to seal the channels, resulting reliable under the operating high-pressure conditions.

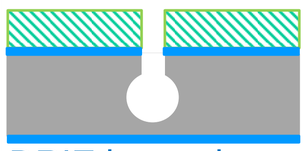
This technique permits the integration of the cooling system within the detector with obvious advantages on the optimization of thermal bridges and transparency to the incident particles.

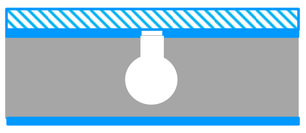
Technology

Process flow





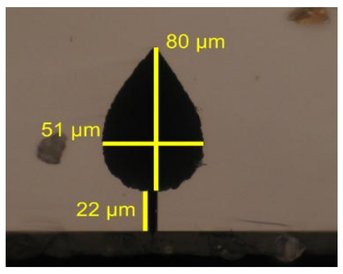


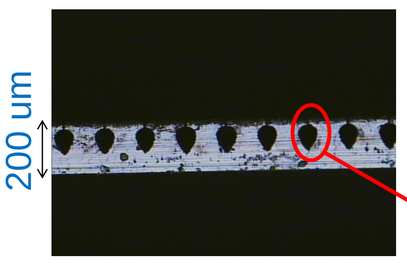


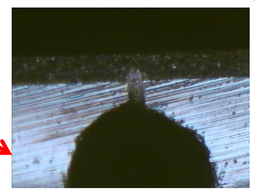
Avoiding high temperature steps, the process is compatible with a CMOS device.

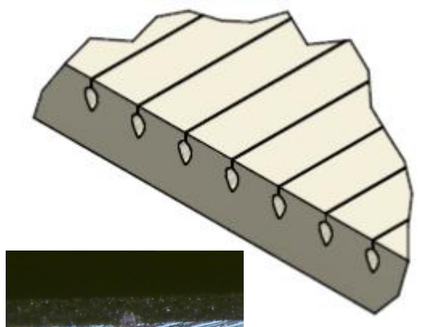
Layout 1

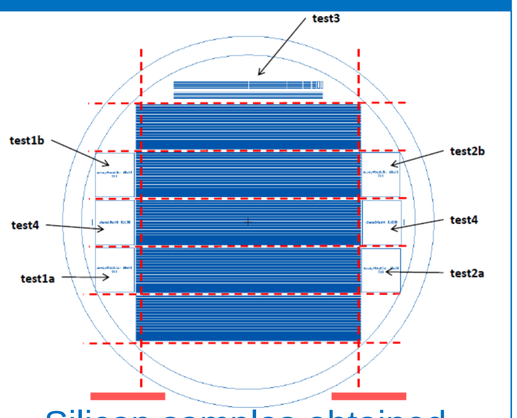
Channels made with individual holes:
The section is determined by the DRIE process, the length by the layout







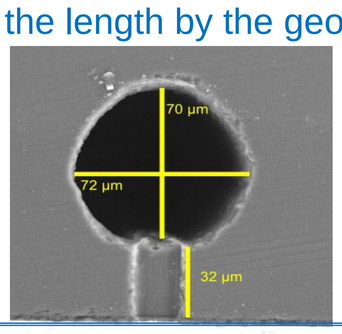


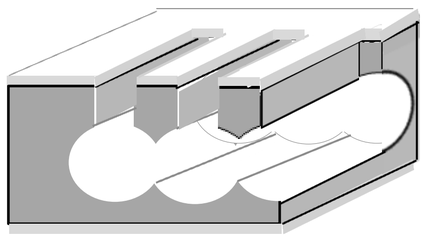


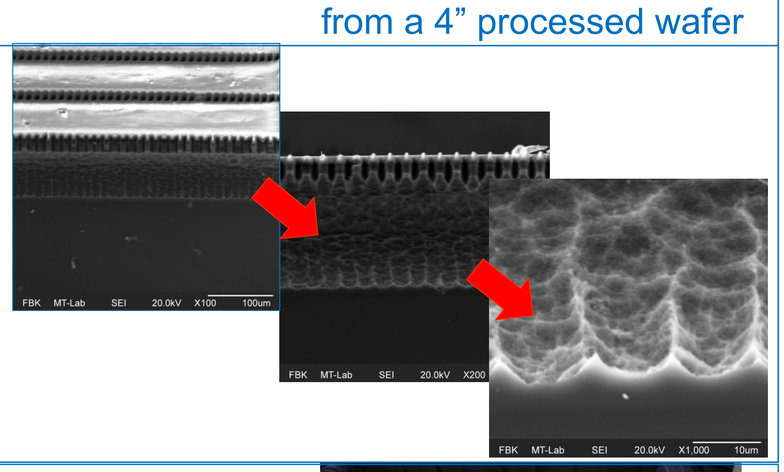
Silicon samples obtained from a 4” processed wafer

Layout 2

Channels realized as a sum of individual holes:
The section is determined by the process and by layout, the length by the geometry

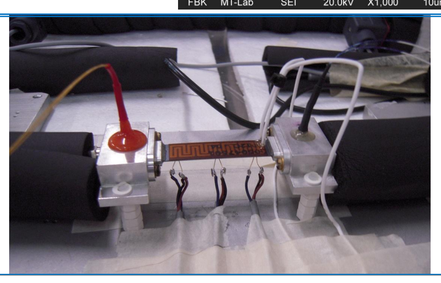






Microchannel silicon prototype test set-up

In the test-stand we used kapton/copper heather on one side of the sample and N.3 temperature probes on the opposite side. Coolant: water-glycol mix. 50% @ 10° C at the inlet.



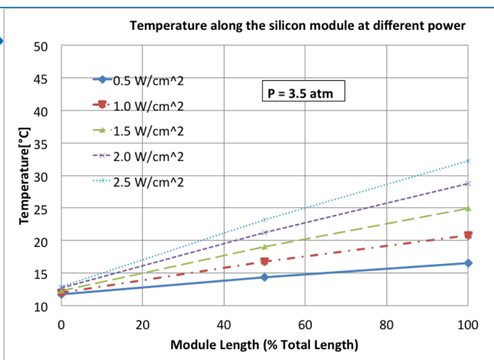
Experimental Tests

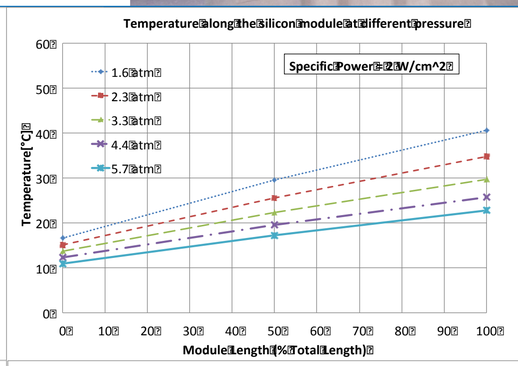
The aim is to keep the sample at a temperature below 50°C with a dissipated power up to 2.5W.

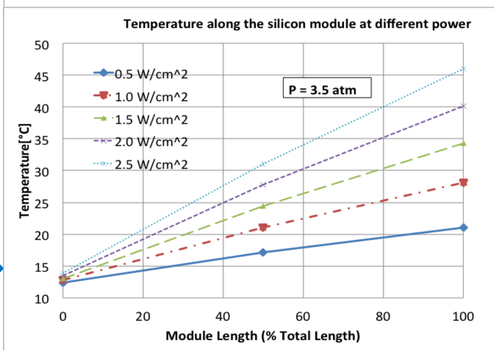
The experimental results of the tests made in the TFD Laboratory @INFN-Pisa show a general compliance of the temperature of the sample with the spec’s.
The average temperature of the samples strongly depends, as expected, on the pressure drop for both the tested geometries.

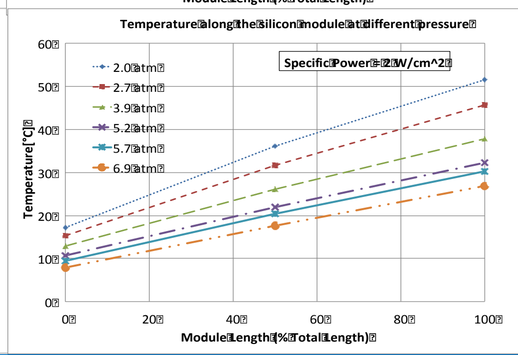
Layout 1 (die 12.8 x 60 mm²):
- 80 channels/ hydr. diameter ~70um
- pitch 150um

Layout 2 (die 12.8 x 60 mm²):
- 80 channels/ hydr. diameter 70um
- pitch 150um









Structural Test

Structural tests were made at high pressure using a dedicated set-up. The test consisted in increasing the pressure in step of 10atm every 10 minutes, and to remain for 1.5 h at the maximum reached pressure.
The oxide layer that seals the microchannels resists at pressures greater than 100 atm (limit of the pump of the circuit).
No damage is observed on the sample, setting a safety factor of about 30 compared to the pressure used in standard test.

Conclusions and Perspectives

Achieved capability to realize microchannels into silicon wafers, using DRIE technology to dig the channels and PECVD to seal them. The tests show:

- ✓ **Efficient cooling of power up to 2.5W/cm²**
- ✓ **Mechanical resistance to high pressure drops**

Further developments:

- ✓ Optimize microchannel design: hydraulic diameter/pitch
- ✓ Special **microchannels with bidirectional flow** to be used to improve performance (decrease the temperaure gradient along the module)
- ✓ Realize **microchannels on single silicon die**
- ✓ Electrical characterization of microchannel-cooled CMOS FE chip

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