

Stefano Bettarini^b, Maurizio Boscardin^a, Filippo Bosi^b, Paolo Conci^a, Michele Crivellari^a, Sabina Ronchin

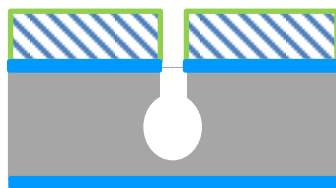
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- ✓ The innovative idea is to **integrate**, into silicon electronics, of the cooling system based on a microchannels made by DRIE technology.
- ✓ The DRIE processes have the capability to create a geometry of the **microchannel** completely original which allows a subsequent step of **sealing** safer and more efficient in the pressure conditions expected during the hydraulic tests.
- ✓ This tech. permits the integration of the cooling system within the same detector with obvious advantages on the optimization of thermal bridges and transparency to the incident particles. Avoiding high temperature steps, the process is compatible with a CMOS device

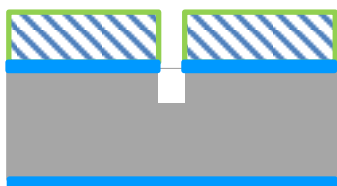
Fabrication Process



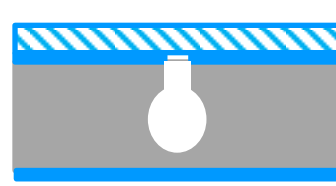
Define & etch SiO₂



DRIE isotropic process



DRIE anisotropic process

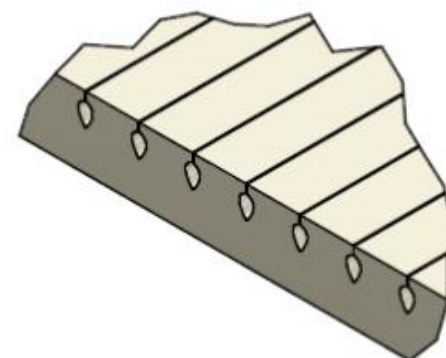
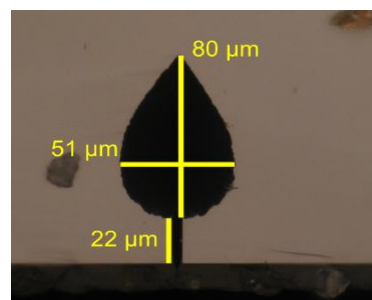


Sealing: PECVD deposition

Microchannel Geometry

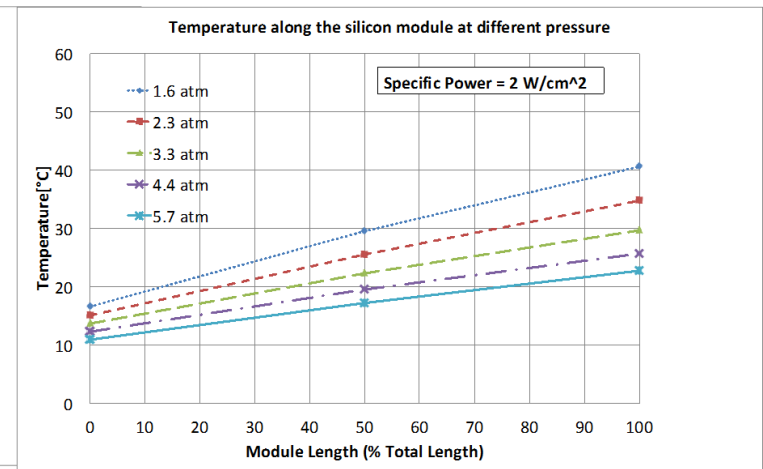
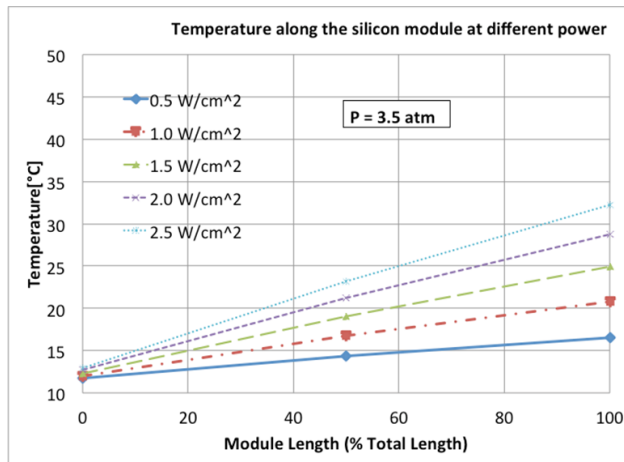
Channels made with individual holes

section is determined by the DRIE process,
length determined by the layout



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- ✓ The **experimental results** show a general compliance of the temperature of the sample to the specific fixed at least up to a power of about 2.5 W/cm² and also indicate at the same power, a strong dependence of the average temperature of the sample from the supply pressure of the fluid.
- ✓ **Structural tests.** The oxide layer that seals the microchannels resists at pressures greater than 100 atm (limit of the pump of the circuit). No damage is observed on the sample, setting a safety factor of about 30 compared to the pressure used in standard test.



Layout 1 (die 12.8 x 60 mm²):

- 80 channels
- hydr. diameter ~70um
- step 150um

Further developments:

- ✓ Optimize microchannel design: hydraulic diameter/pitch
- ✓ Special **microchannels with bidirectional flow** to be used to improve performance
- ✓ Realize **microchannels on single silicon die**
- ✓ Electrical characterization of microchannel-cooled CMOS FE chip