LUDWIG-MAXIMILIANS-UNIVERSITÄT MÜNCHEN

Development of a MicroMegas ReadOutDriver for ATLAS

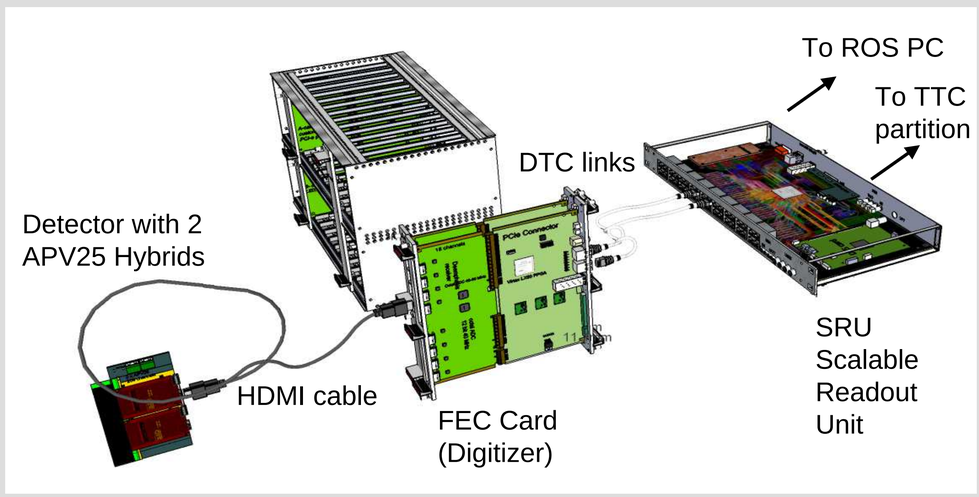
A. Zibell, LMU, LS Schaile
on behalf of the MAMMA collaboration

MicroMegas Chambers at ATLAS / LHC

- The MicroMegas technology has been chosen for the precision chambers for the upgrade of the ATLAS Small Wheel. (see *M. Byszewski, Development of large-area resistive-strip micromegas chambers for the ATLAS muon system upgrade*)
- Two MicroMegas prototype detectors have been installed in February 2012, one in the MBTS (Minimum Bias Trigger Scintillators) region (left) and one on a Small Wheel CSC detector (right), regions of highest and high background rates.
- The Small Wheel detector consists of four strip layers, 9x9 cm² each, with different pitch, the active area of the MBTS detector is 9x4.5 cm².
- The detectors are connected to the readout electronics via 30m HDMI cables. From there, data are sent via 100m optical SLINK fibre to the Read Out System (ROS) in cavern USA15, where the low voltage power supplies are situated as well.
- Slow control is realised via optical fibre gigabit ethernet.

The Scalable Readout System (SRS)

H. Müller, S. Martoiu, RD51

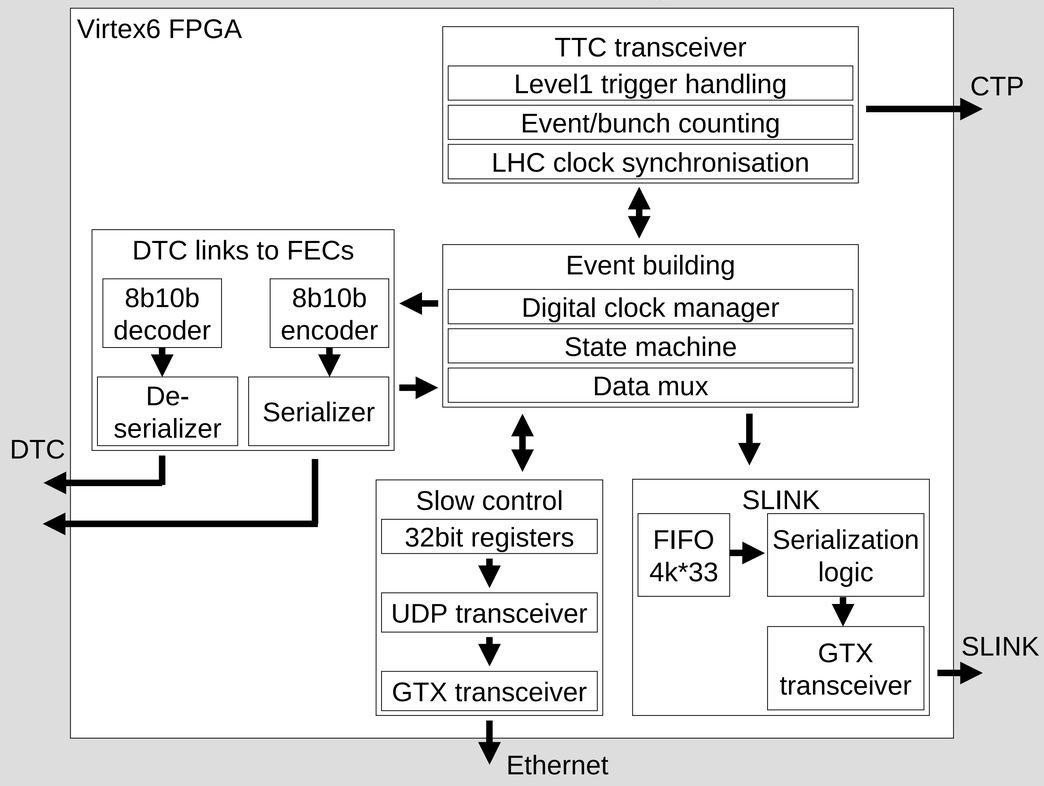


- The SRS can use APV25 frontendchips with 128 channels each, or several other chips, using different adapter cards
- Digitization and zero suppression is done on the Front End Concentrator (FEC) Card (housing a Virtex5 FPGA)
- A 19“, 1HE Scalable Readout Unit (SRU) can be used for data collection from FEC cards and connection to the data aquisition system (housing a Virtex6 FPGA). FEC cards can also send data directly to a DAQ PC via ethernet.
- ~81k channels can be read out with one single SRU: 16 APV25 chips per FEC card, up to 40 FEC cards per SRU.
- The APV25 is a 128 channel charge sensitive amplifier chip with 192 cell pipeline and multiplexed analoge readout. It was developed for the CMS microstrip detector.

DTC Links from FEC cards to SRU *A. Martinez*

- LHC clock and Level1 triggers are transmitted via DTC to the FEC cards / APV25 chips
- The links for detector data work with 1Gbit/s over 5m CAT7 S/FTP cable
- Using 8bit/10bit encoding and differential transmission, no transmission errors were observed during several days of running

FPGA Firmware Design *A. Zibell*



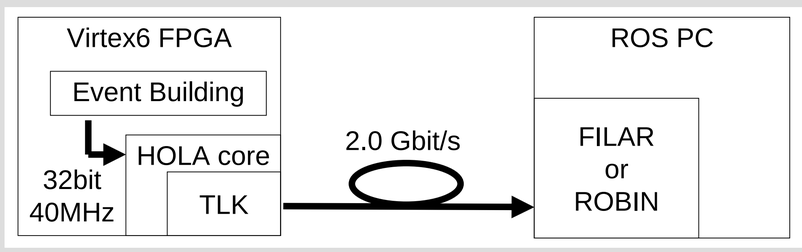
- The FPGA firmware has to manage a variety of tasks for stable operation in the ATLAS data aquisition chain
- These are: Level1 trigger reception and forwarding, data collection, event building, data formatting, SLINK serialization, slow control and error handling
- The SRU‘s onboard TTCrx transceiver chip allows direct connection of the SRU board to a TTC partition (Trigger, Timing and Control)
- The APV25 chip is not the final choice for the readout of MicroMegas detectors, since the mutliple readout of the chip per event to extract timing information from the pulse shape does not allow to read out the system with the Level1 trigger frequency.
- Since the ROS awaits data words for every trigger, the firmware replies empty events with just header and trailer for each trigger that could not be served by the APV25 chips due to the above limitation.
- For this reason, a new frontend chip VMM1 is being developed in BNL, prototypes to be tested during test beams in July 2012 (*G. De Geronimo et al, subm. to TWEPP and IEEE/NSS 2012 meetings*)

ATLAS event data format (32bit words)

Start of header	Run number	Det. event type	No. of status el.
Header size	Ext. L1 ID	Data elements	No. of data el.
Format version	Bunch cross. ID		Status bl. pos.
Source Identifier	L1 trigger type	Status elements	

SLINK Connection to ROS

M. Della Volpe, R. Giordano, V. Izzo, S. Perrella



- Data are transferred between Read Out Driver (SRU) and the ATLAS data aquisition system via standard optical SLINK: 32bit data width, 40MHz transfer rate, 160MByte/s and autonomous link synchronization.
- No need for separate SLINK daughter card (HOLA, with TLK2501 transceiver chip), since the SRU‘s modern Virtex6 FPGA can handle SLINK protocol and encoding/serialization in addition to its other tasks with help of the FPGAs logic resources and GTX transceivers.
- Data transfer with a standard Read Out System PC was tested successfully. The transmitted data frames were correctly received with both FILAR and ROBIN PCI-cards, which are used in the ATLAS DAQ system.

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