64-Channel, 5 GSPS ADC Module with Switched Capacitor Arrays

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We present a 5 GSPS ADC/Data processing Module with up to 64 channels and 2,048 cells per channel, designed for fast-sampling, front-end applications. This is a 6U VME board, that incorporates 16 pieces DRS4 switched capacitor array chips developed at Paul Scherrer Institut, Switzerland. The 16 DRS 4 chips are grouped in four independent input blocks. A block, with a geometric size of 43 by 120 mm, has 4 pieces DRS 4 chips, 4 pieces AD9222 converters, and one Altera Stratix III FPGA. Each DRS 4 chip has 8 channels and each channel has 1024 sampling cells, which can be daisy-chained for larger sampling depth. This feature allows for a great level of flexibility in choosing the number of channels relative to capacitor array size, for a particular application. The first prototype PCB was designed for a sampling depth of 2,048 cells and 16 channels in a 42mm wide block, i.e. 64 channels for the 6U VME board. This compact form factor allows for these input blocks to be used as front-end electronics for the Cherenkov Telescope Array (CTA) cameras. In this VME board, the four blocks are fully independent and can run each in different modes without any conflict. A global FPGA, also a Stratix III device, provides control and interfacing. The module can run with a local oscillator or with input system clocks in the range of 20MHz to 550MHz. The front panel is fitted with a 2.5Gbps serial link transceiver.

This 6U VME Module was designed to incorporate 16 pieces DRS4 Custom Integrated Circuits (IC) developed at PSI, Switzerland. The DRS4 is a fast sampling front-end chip with a Switched Capacitor Array (SCA) of (8+1) channels, with 1024 sampling cells each. The channels can be daisy-chained for larger sampling depth. In this application the chips were configured with 2048 sample/channel, for a total of 64 channels in one 6U VME board.

The Block Diagram of the Module is presented in Figure 1. The board receives single-ended inputs which are turned into differential with local transformers, and passed along to the DRS4 chips. These analog signals are sampled inside the chip with a sampling rate controlled between 700 MSPS and 5 GSPS. Upon a trigger, sampling is stopped, and all channels are digitized and read out in parallel, with an Octal, 12-Bit, AD9222-40 Converter. Serial LVDS data streams are sent to the Block FPGA. The dead time is determined by the number of samples per trigger and the readout clock frequency (20 to 30 MHz).

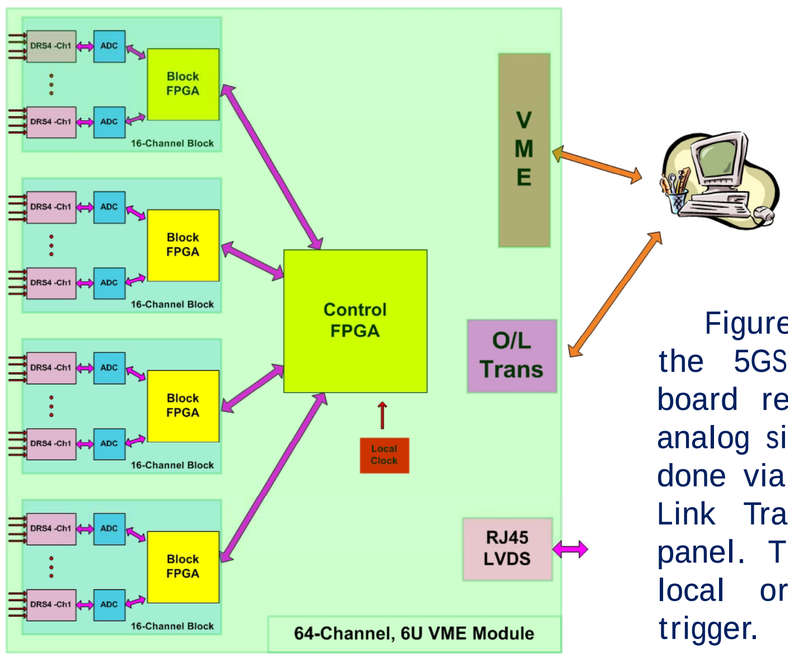

Figure 1. Block Diagram of the 5GSPS ADC Module. This board receives 64 single-ended analog signals. Readout can be done via VME or via an Optical Link Transceiver at the front panel. The Module can run on local or external clock and trigger.

This module is hard-wired to daisy-chain every two channels and accepts 4 analog inputs per DRS4 chip. In this configuration, the module has a total of 64 channels, with 2048 sampling cells per channel. The daisy-chaining of channels can be further increased on-line to achieve a larger sampling depth or channel density.

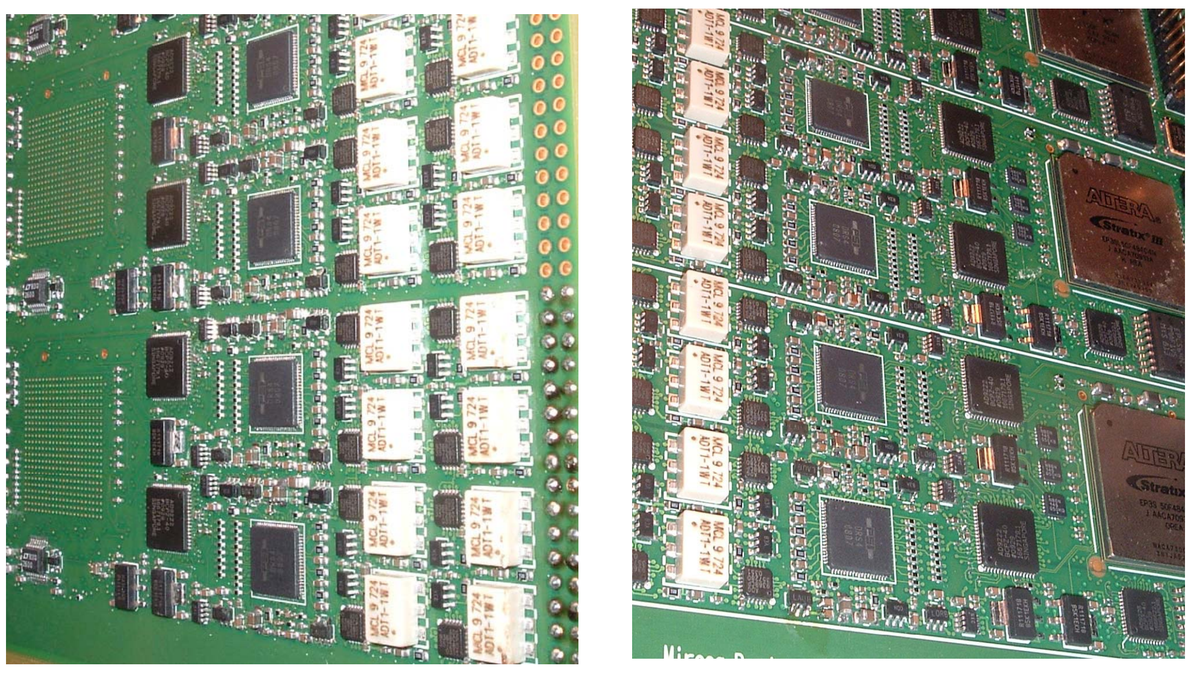

Figure 2. Prototype ADC Module, Top and Bottom sides. To achieve the required channel density, the Printed Circuit Board (PCB) was designed with all components from one front-end block being placed on the same side of the board, resulting in an almost identical top and bottom component placement.

The 16 DRS4 chips are grouped in four independent blocks, 4 chips on each block. Different blocks can run at different sampling rates and on different triggers, without conflict. Triggers can be generated at the block level from the Block FPGA, at the module level from the Control FPGA, or the board can run on external triggers via the RJ45 front panel connector. Similarly, there are independent clock oscillators in each block and one at the board level, or the board accepts an LVDS system clock at the front panel.

Figure 2 shows the prototype that has been designed and built at The University of Chicago. It accepts a single-ended input of 0-1V on each channel. The Input bandwidth (-3dB) is about 200 MHz. This is below the actual performance of the DRS4 chip, and further upgrades with active input buffers will improve this characteristic.

This Module was tested at sampling rates from 0.7 GSPS to 5 GSPS, with a readout speed of 25 MHz, and 0 – 2048 samples per readout. The random noise measured was about 1 mV RMS after offset correction, and the adjacent channel crosstalk measured was below -40dB.

12th Pisa Meeting on Advanced Detectors
La Biodola, Isola d'Elba, Italy
May 20 - 26, 2012