64-CHANNEL, 5 GSPS ADC MODULE WITH SWITCHED CAPACITOR ARRAYS

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- This 6U VME Module incorporates16 pieces DRS4 Custom ICs developed at PSI, Switzerland.
- Each DRS4 chip has 8 channels with 1024 sampling cells each. This Module is hard-wired to daisy-chain every two channels. Larger sampling depths can be programmed.
- Total of 64 channels at 2048 sampling cells per channel.
- Inputs are grouped in 4 Blocks of 16 that can run independently (separate clock, trigger).
- Interfaces:
  - VME64;
  - Optical Link Transceiver (2.5GBPS);
  - LVDS (external clock, trigger, control).

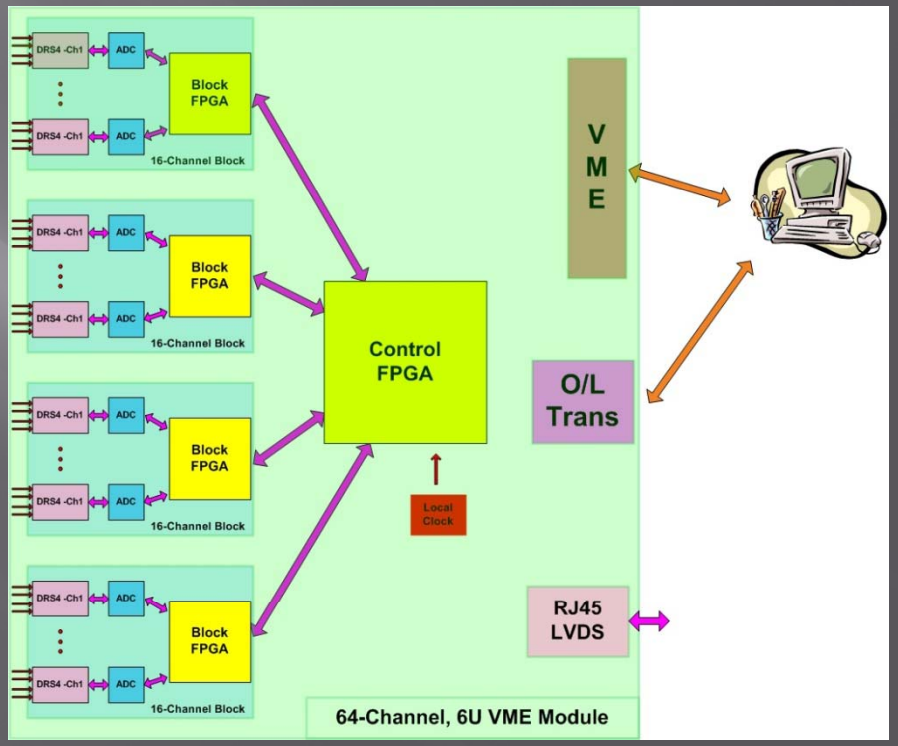

Figure 1. Block Diagram of the 64-Ch, 5GSPS ADC Module.

64-Channel, 5 GSPS ADC Module

Specifications:

- 64 Analog Inputs: 0-1V single-ended;
- Input Bandwidth: 200 MHz;
- Sampling depth: 2048 samples;
- Sampling rate: 700 MSPS - 5 GSPS;
- Sampling Cell readout: 25-30 MHz;
- Samples per readout: 0 – 2048;
- Channel Crosstalk: - 40dB;
- Random Noise: 1mVrms (with offset correction);
- Nonlinearity: 0.5 mV (with offset correction);
- Power per channel: 0.75W.

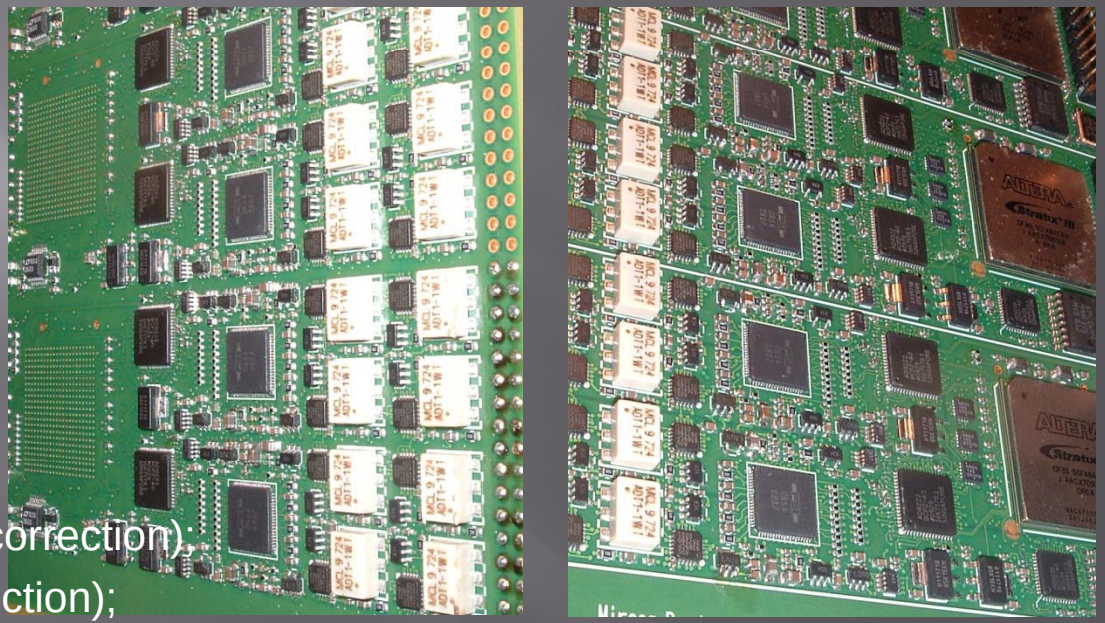

Figure 2. Prototype ADC Module, Top and Bottom sides. The PCB was designed with all components from one front-end block being placed on the same side of the board, resulting in an almost identical top and bottom component placement.