PAUL SCHERRER INSTITUT

PSI

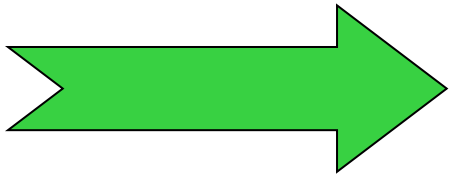
Paul Scherrer Institute

Stefan Ritt

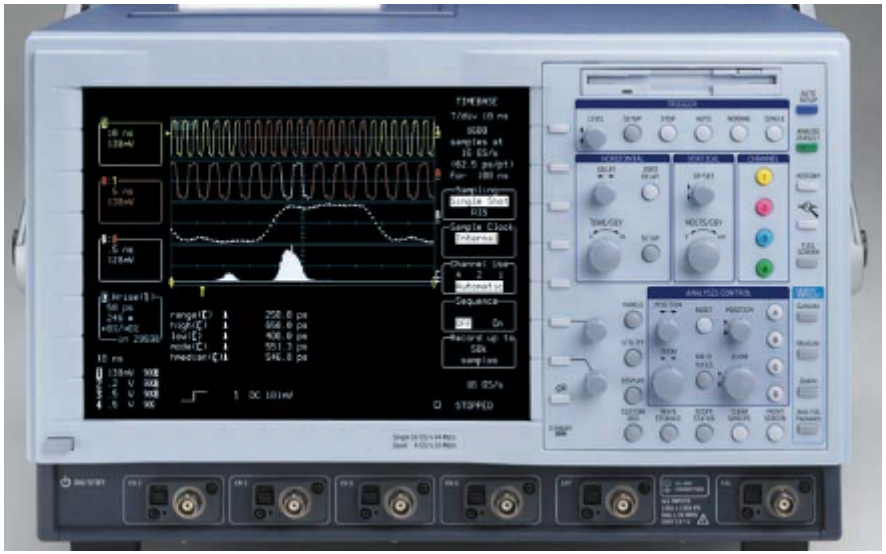
Gigahertz Waveform Sampling: An Overview and Outlook

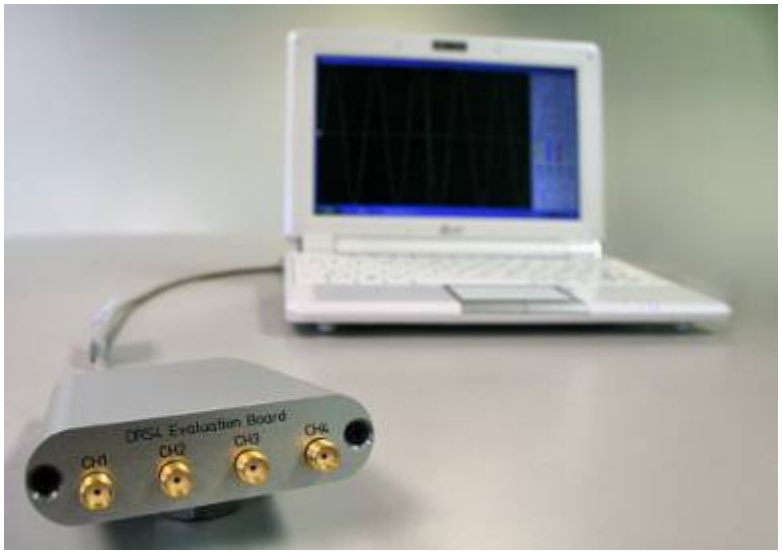
Question ?

4 channels
5 GSPS
1 GHz BW
8 bit (6-7)
15k€



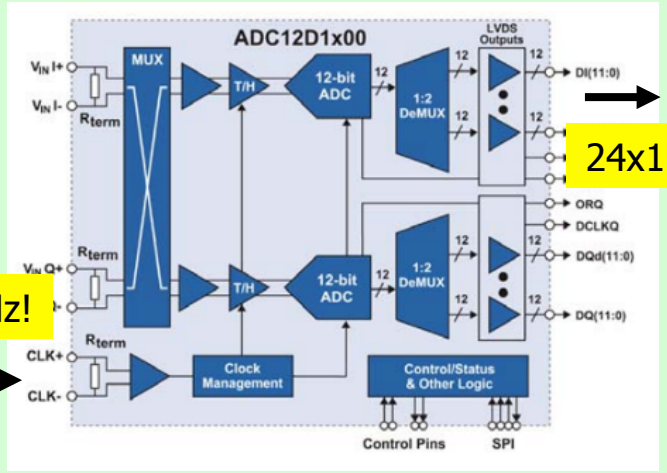
4 channels
5 GSPS
1 GHz BW
11.5 bits
900€
USB Power





Can it be done with FADCs?

- 8 bits – 3 GS/s – 1.9 W → 24 Gbits/s
- 10 bits – 3 GS/s – 3.6 W → 30 Gbits/s
- 12 bits – 3.6 GS/s – 3.9 W → 43.2 Gbits/s
- 14 bits – 0.4 GS/s – 2.5 W → 5.6 Gbits/s

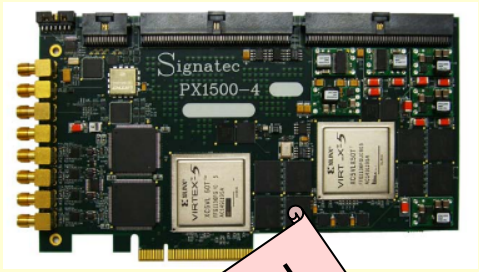


1.8 GHz!

24x1.8 Gbits/s

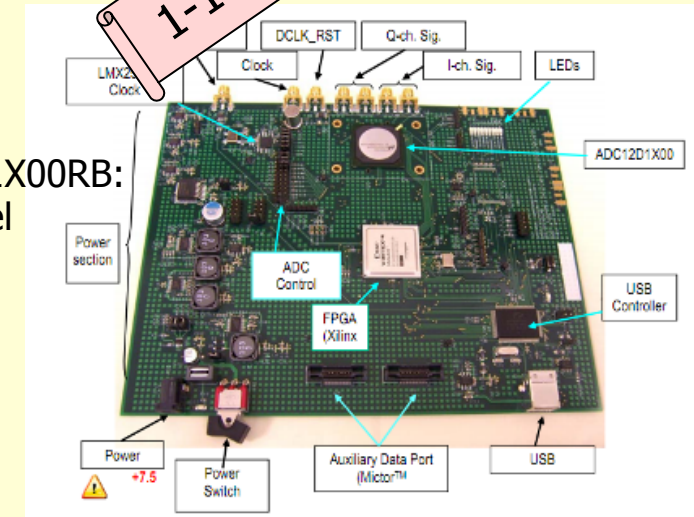
- Requires high-end FPGA
- Complex board design
- FPGA power

PX1500-4:
2 Channel
3 GS/s
8 bits



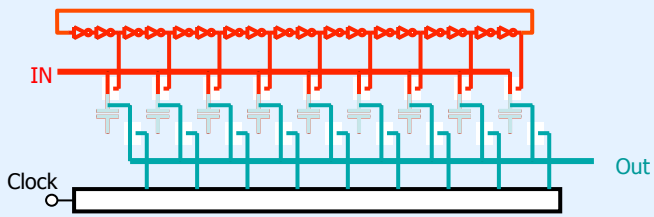
1-10 k€ / channel

ADC12D1X00RB:
1 Channel
1.8 GS/s
12 bits

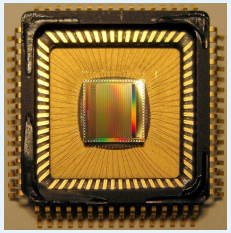


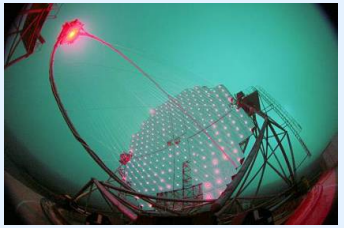
Overview

- Design Principles and Limitations of Switched Capacitor Arrays

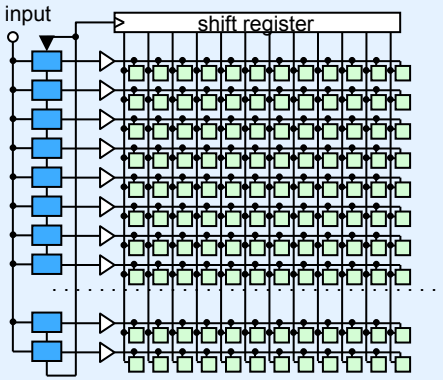


- Overview of Chips and Applications

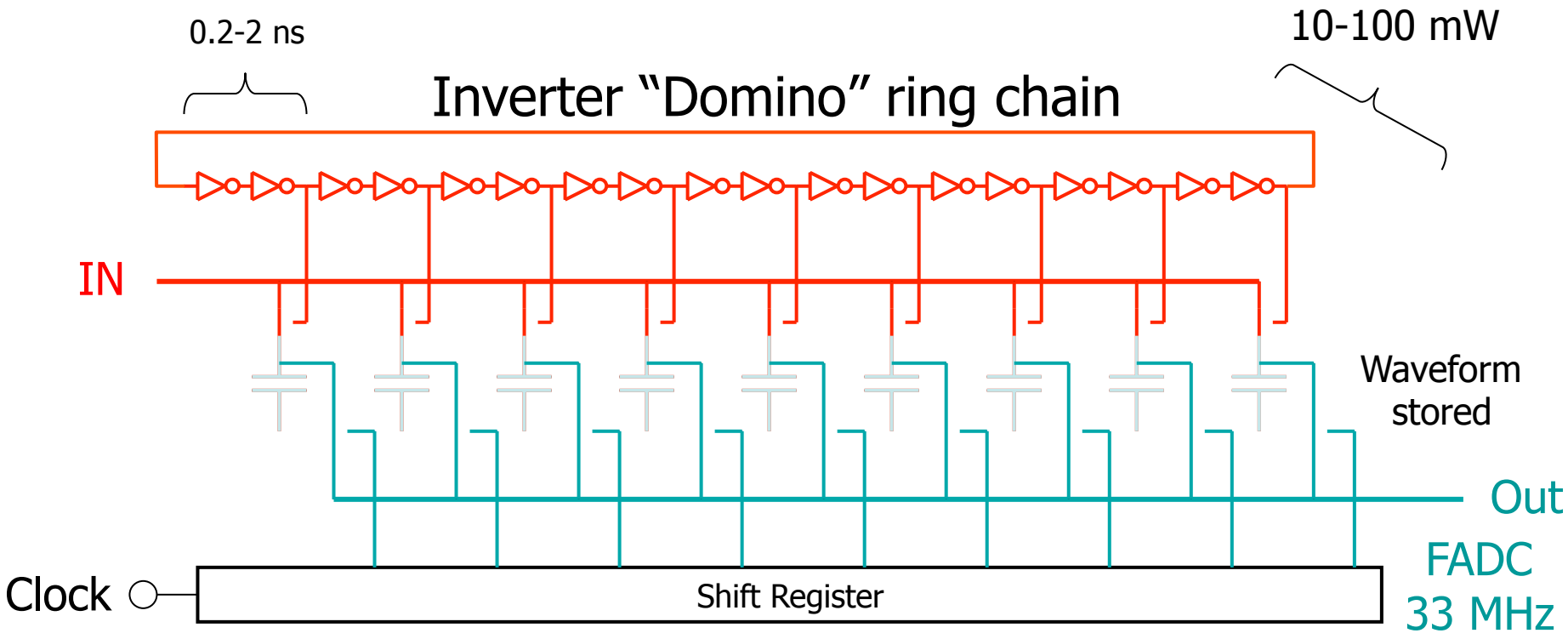




- Future Design Directions

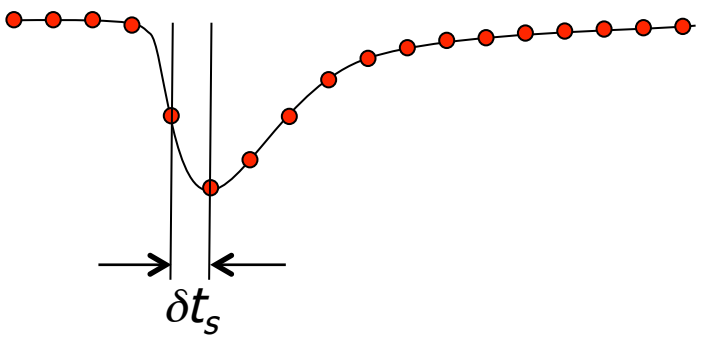


Switched Capacitor Array (Analog Memory)

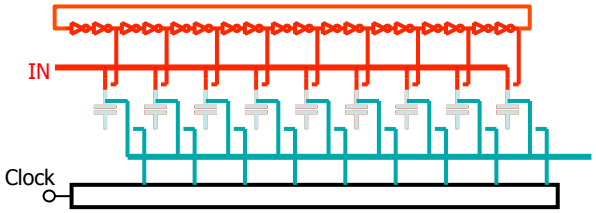


"Time stretcher" GHz → MHz

Time Stretch Ratio (TSR)



$$TSR \equiv \frac{\delta t_s}{\delta t_d}$$

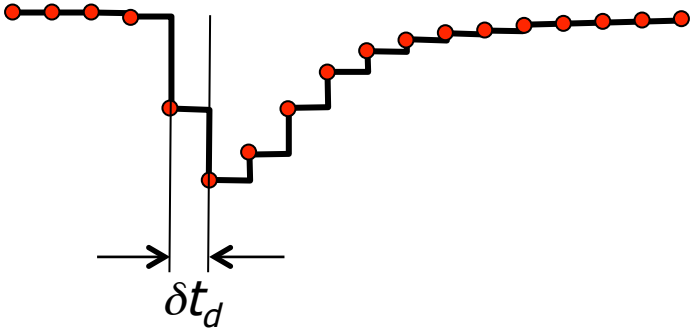


Typical values:

- δt_s = 0.5 ns (2 GSPS)
- δt_d = 30 ns (33 MHz)
  $\rightarrow TSR$ = 60

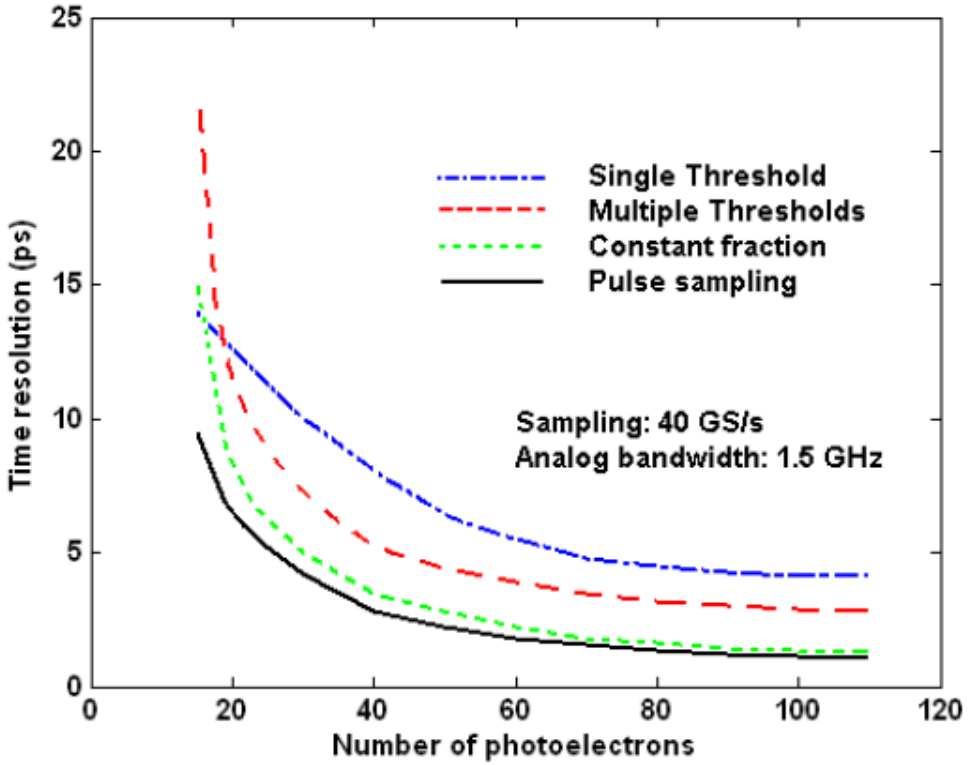
Dead time =
Sampling Window · TSR

(e.g. 100 ns · 60 = 6 μs)



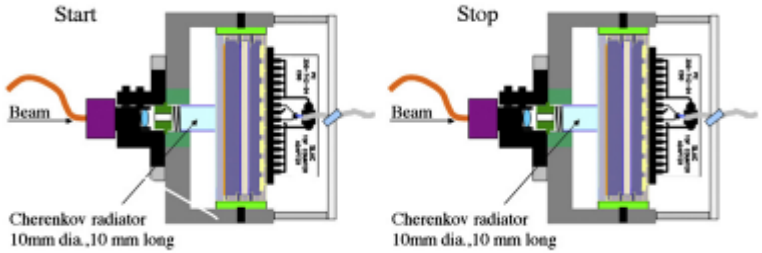
How to measure best timing?

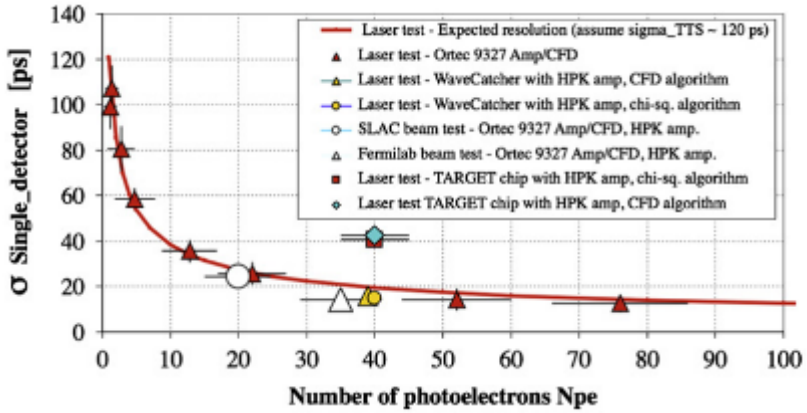
Simulation of MCP with realistic noise and different discriminators



J.-F. Genat et al., arXiv:0810.5590 (2008)

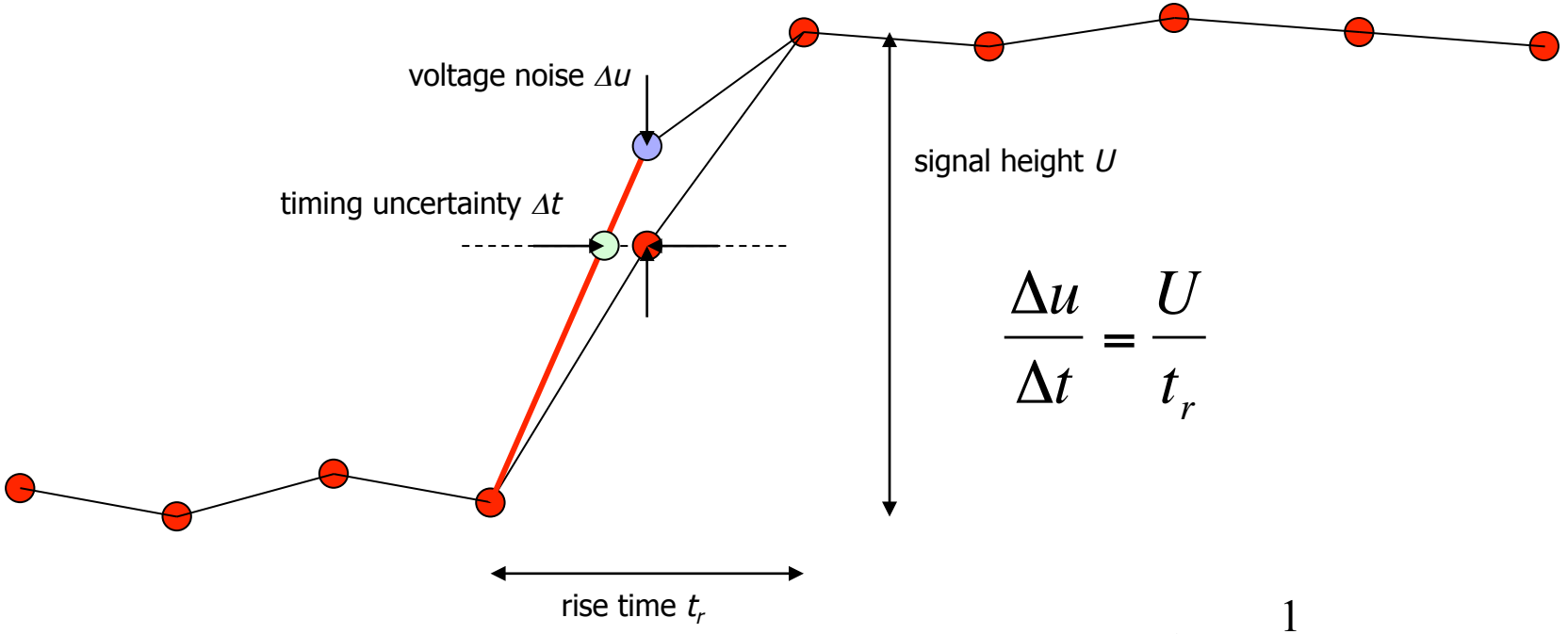
Beam measurement at SLAC & Fermilab





D. Breton et al., NIM **A629**, 123 (2011)

How is timing resolution affected?



$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

$$t_r \approx \frac{1}{3 f_{3dB}}$$

$$\Delta t = \frac{\Delta u}{U} \cdot t_r = \frac{\Delta u}{U\sqrt{n}} \cdot t_r = \frac{\Delta u}{U} \cdot \frac{t_r}{\sqrt{t_r \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

number of samples on slope

Simplified estimation!

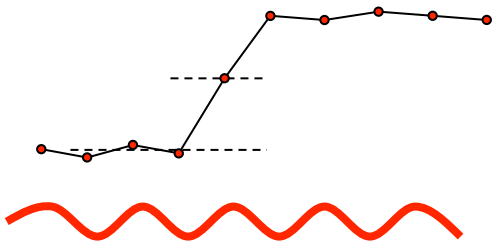
How is timing resolution affected?

$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

Assumes zero aperture jitter

	U	Δu	f_s	f_{3db}	Δt
today:	100 mV	1 mV	2 GSPS	300 MHz	~10 ps
optimized SNR:	1 V	1 mV	2 GSPS	300 MHz	1 ps
next generation:	1V	1 mV	10 GSPS	3 GHz	0.1 ps

includes detector noise
in the frequency region of the rise time
and aperture jitter



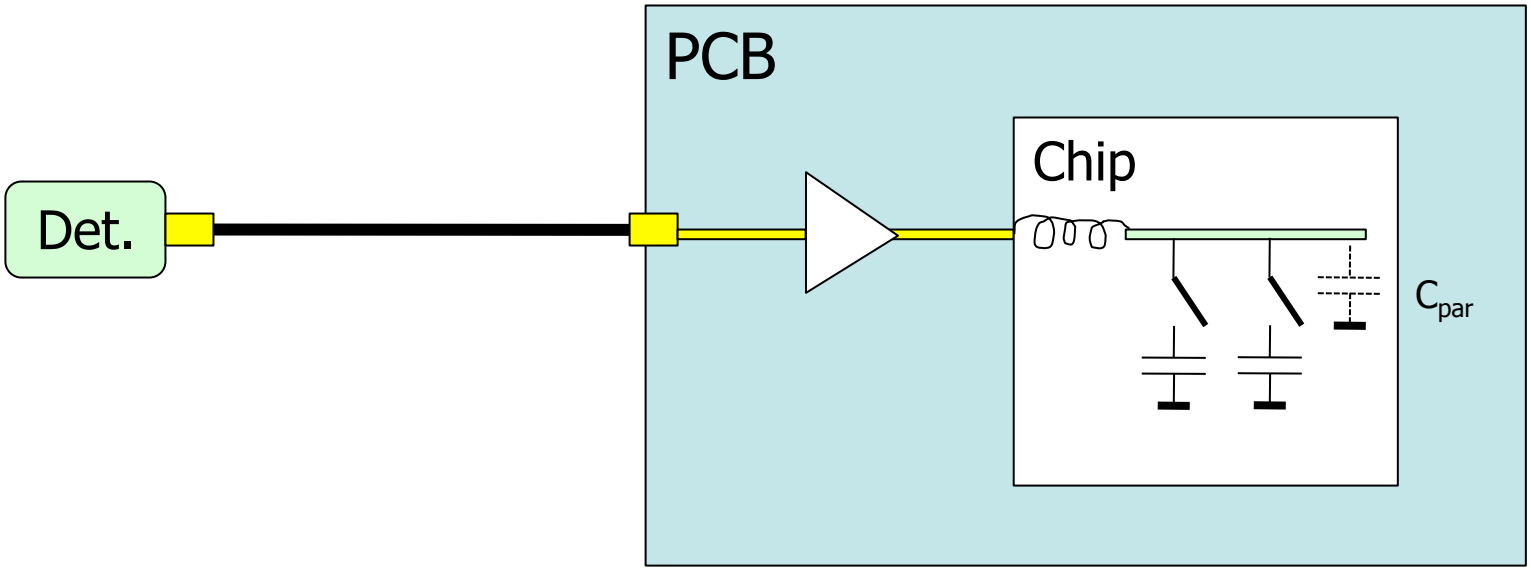
Limits on analog bandwidth

- External sources
  - Detector
  - Cable
  - Connectors
  - PCB
  - Preamplifier
- Internal sources
  - Bond wire
  - Input bus
  - Write switch
  - Storage cap

Low pass filter

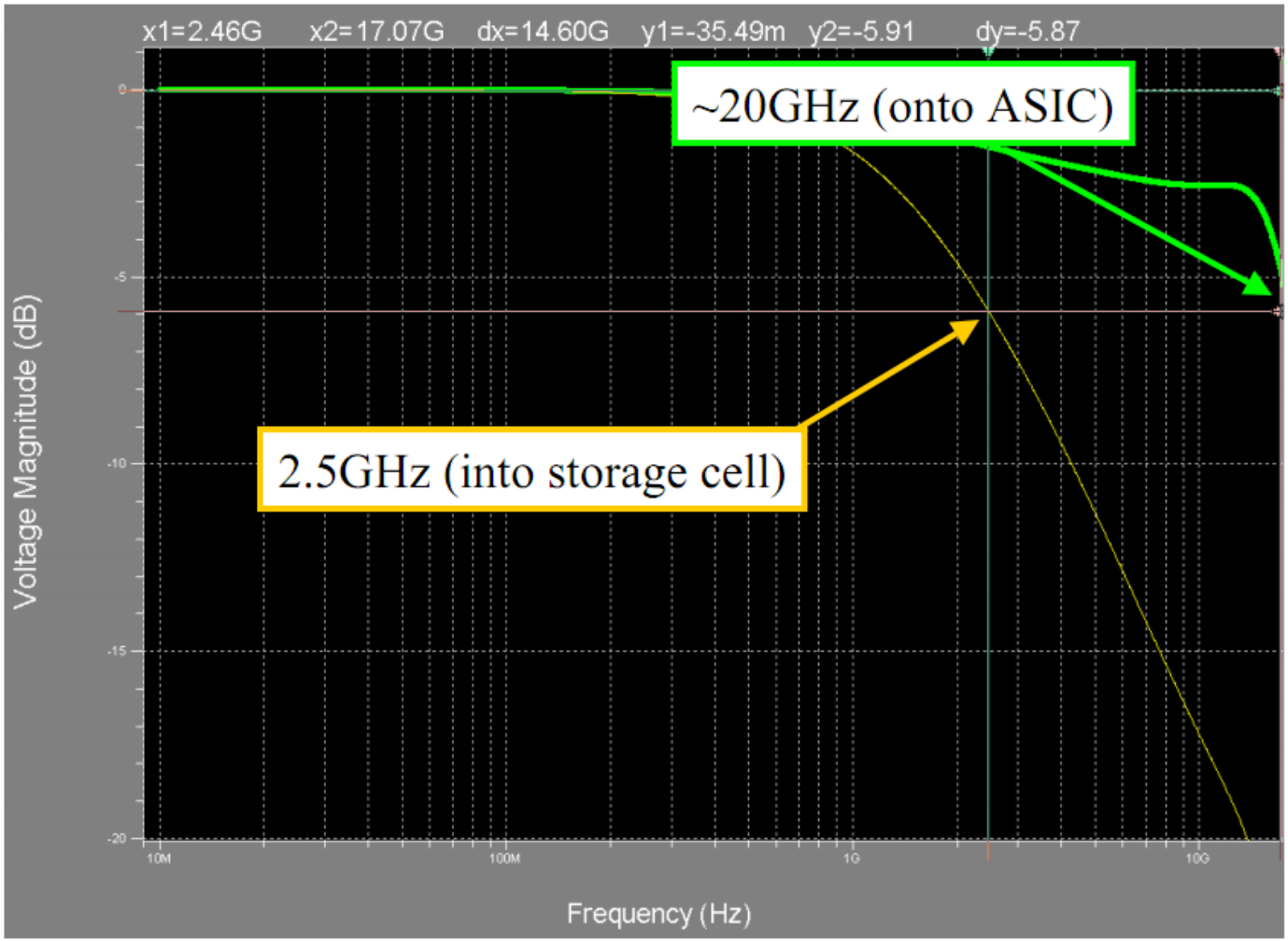
Low pass filter

$$f_{3db} = \frac{1}{2\pi RC}$$



Bandwidth STURM2 (32 sampling cells)

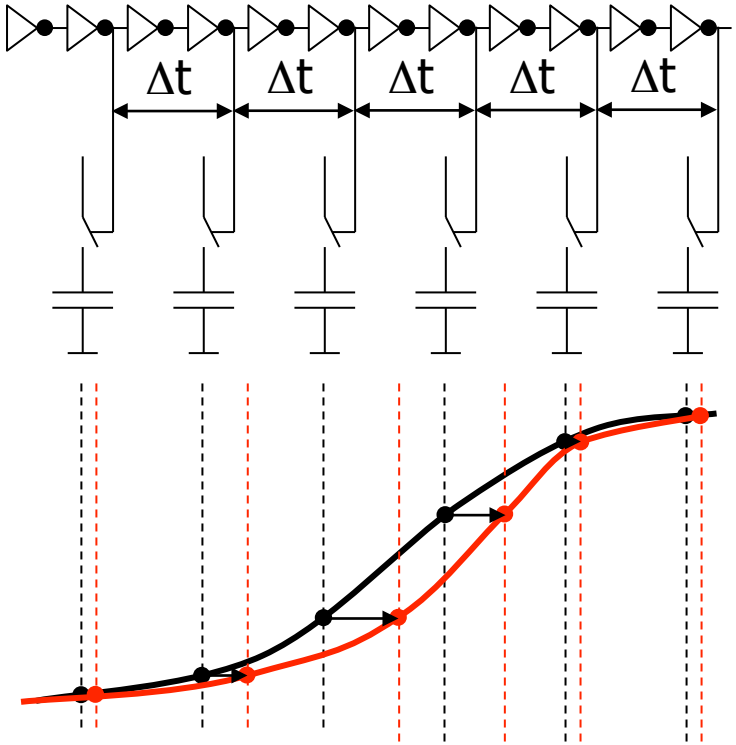
Bump-bonding (optimized) input coupling

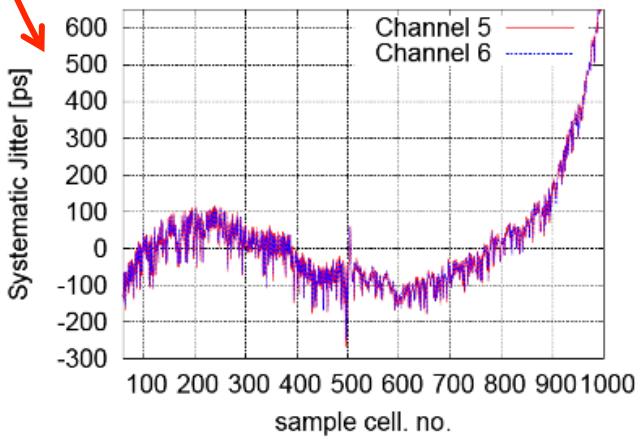


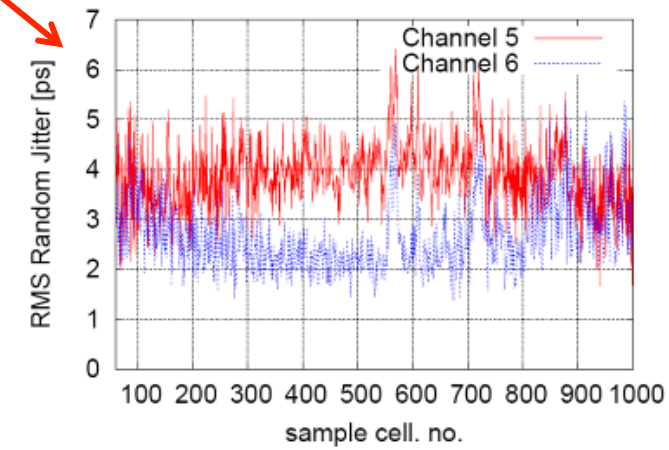
G. Varner, Dec. 2009

Timing Nonlinearity

- Bin-to-bin variation:
  "differential timing nonlinearity"
- Difference along the whole chip:
  "integral timing nonlinearity"
- Nonlinearity comes from size (doping) of inverters and is stable over time
  → can be calibrated
- Residual random jitter:
  3-4 ps RMS exceeds best TDC

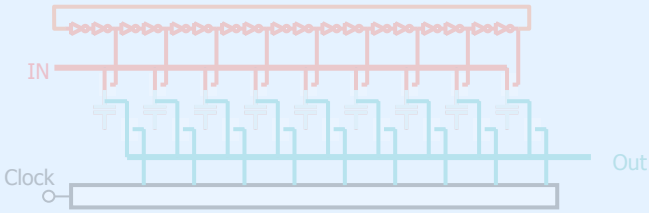




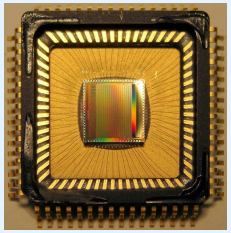


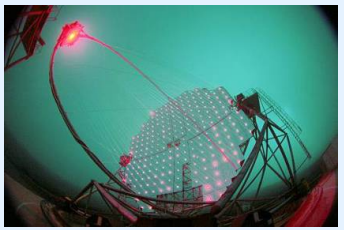
Part 2

- Design Principles and Limitations

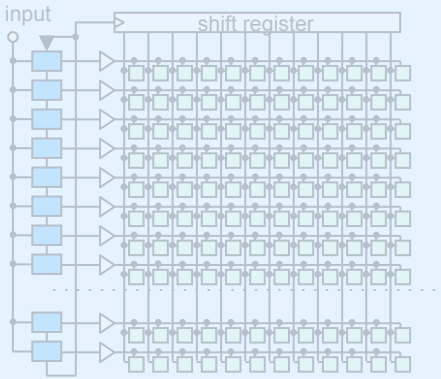


- Overview of Chips and Applications



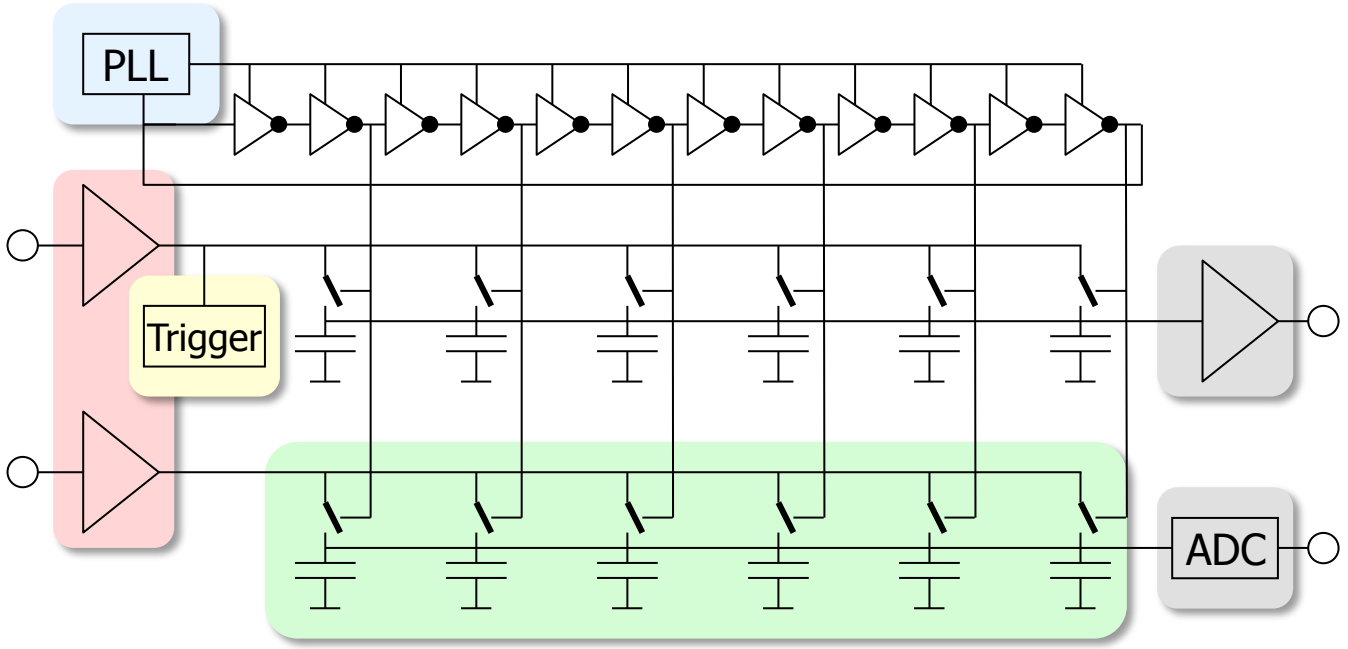


- Future Design Directions

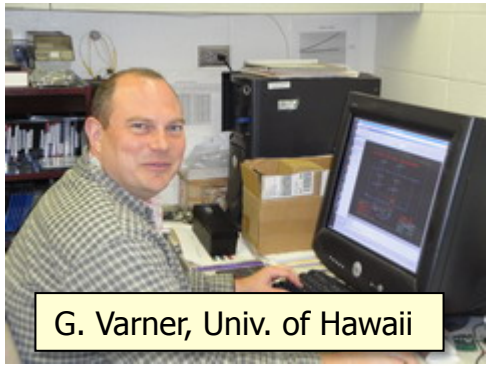


Design Options

- CMOS process (typically 0.35 … 0.13 μm) → sampling speed
- Number of channels, sampling depth, differential input
- PLL for frequency stabilization
- Input buffer or passive input
- Analog output or (Wilkinson) ADC
- Internal trigger
- Exact design of sampling cell



Switched Capacitor Arrays for Particle Physics

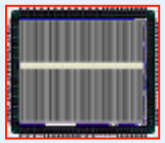
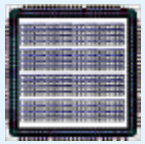


G. Varner, Univ. of Hawaii

E. Delagnes
D. Breton
CEA Saclay

H. Frisch et al., Univ. Chicago

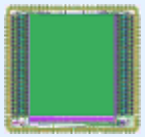
STRAW3 LABRADOR3 TARGET

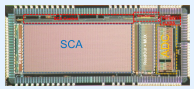




- 0.25 μm TSMC
- Many chips for different projects (Belle, Anita, IceCube …)

www.phys.hawaii.edu/~idlab/

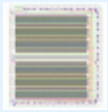
AFTER SAM NECTAR0





- 0.35 μm AMS
- T2K TPC, Antares, Hess2, CTA

matacq.free.fr



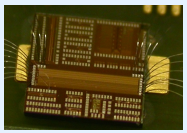
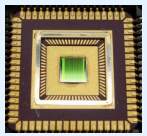
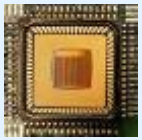
PSEC1 - PSEC4

Poster 232

- 0.13 μm IBM
- Large Area Picosecond Photo-Detectors Project (LAPPD)

psec.uchicago.edu

DRS1 DRS2 DRS3 DRS4


2002 2004 2007 2008

- 0.25 μm UMC
- Universal chip for many applications
- MEG experiment, MAGIC, Veritas, TOF-PET

Poster 15, 106

SR
R. Dinapoli
PSI, Switzerland

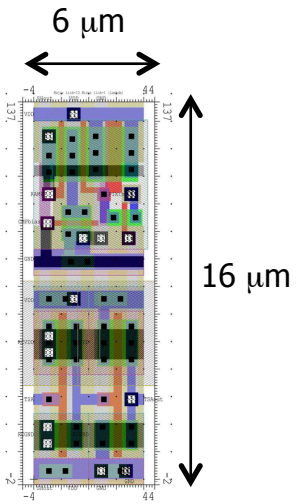
drs.web.psi.ch

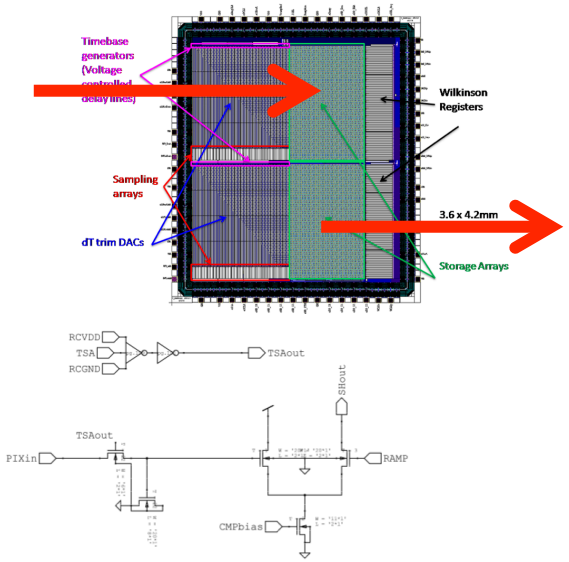
Some specialities

- LAB Chip Family (G. Varner)
  - Deep buffer (BLAB Chip: 64k)
  - Double buffer readout (LAB4)
  - Wilkinson ADC

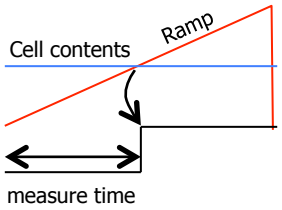
- NECTAR0 Chip (E. Delagnes)
  - Matrix layout (short inverter chain)
  - Input buffer (300-400 MHz)
  - Large storage cell (>12 bit SNR)
  - 20 MHz pipeline ADC on chip

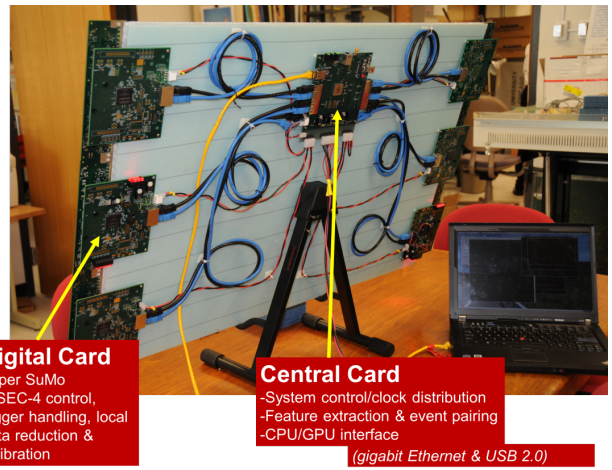
- PSEC4 Chip (E. Oberla, H. Grabas)
  - 15 GSPS
  - 1.6 GHz BW @ 256 cells
  - Wilkinson ADC

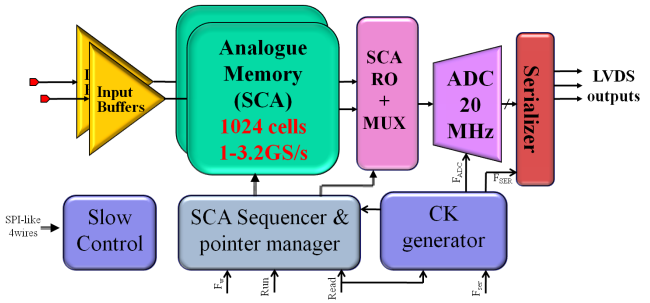




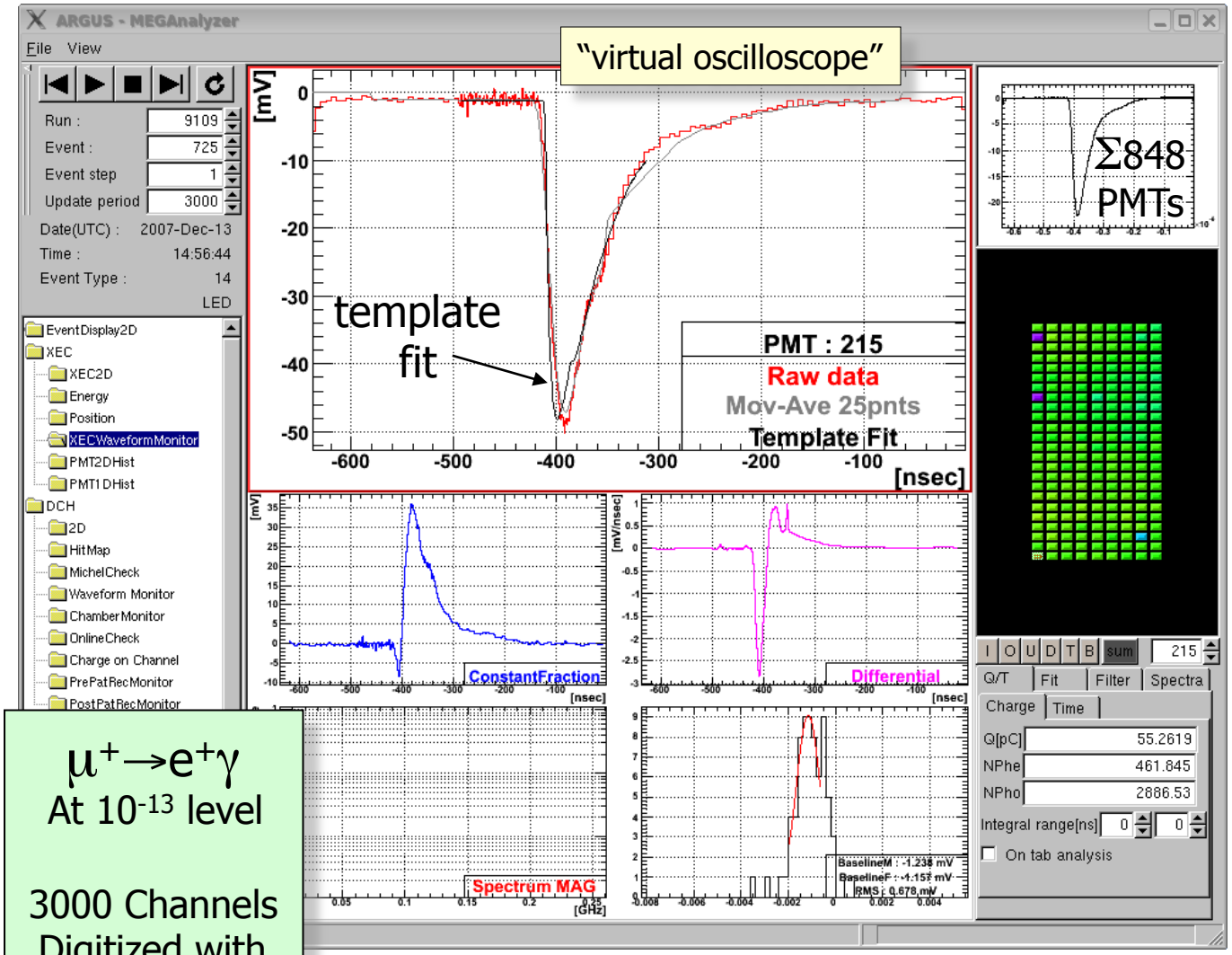
Wilkinson-ADC:

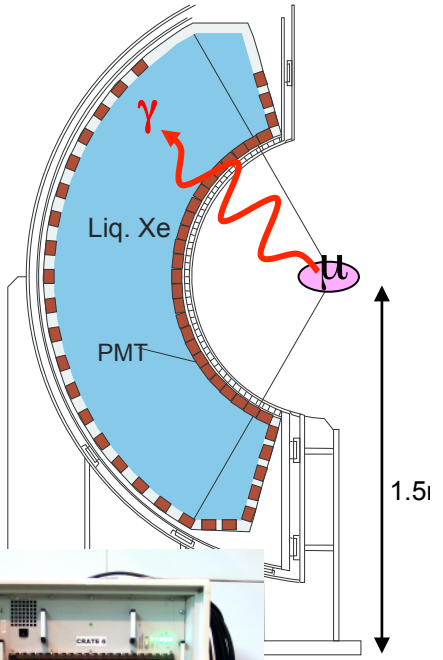


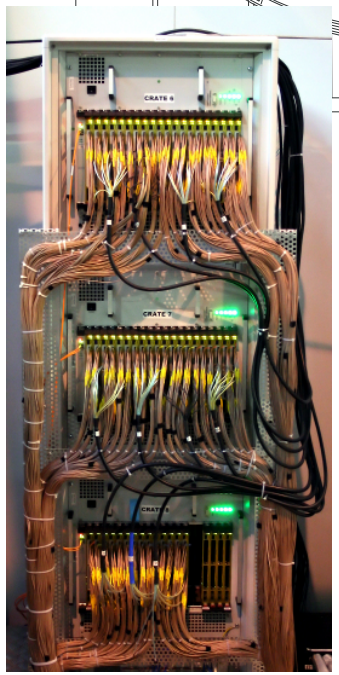




MEG On-line waveform display





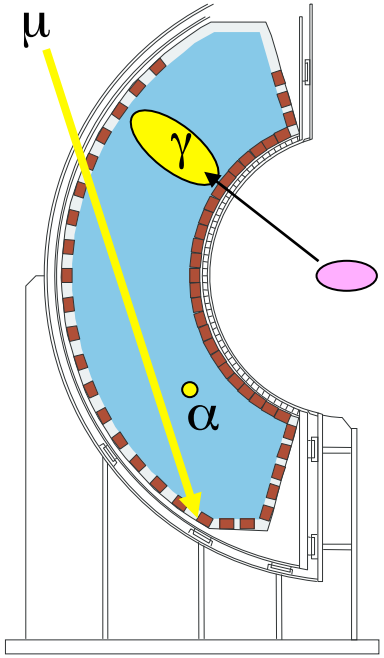


$\mu^+ \rightarrow e^+\gamma$
At 10^{-13} level

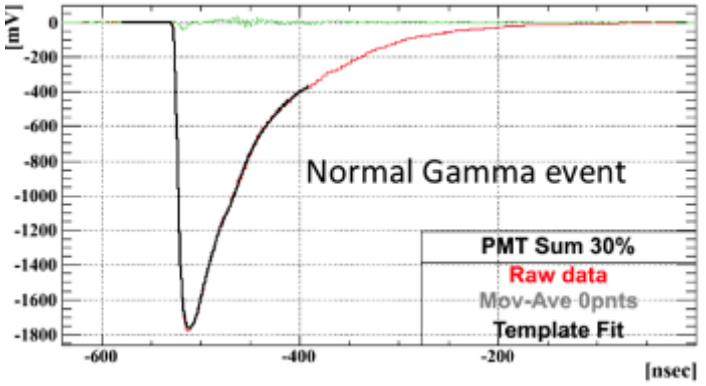
3000 Channels Digitized with **DRS4 chips** at 1.6 GSPS

Drawback: 400 TB data/year

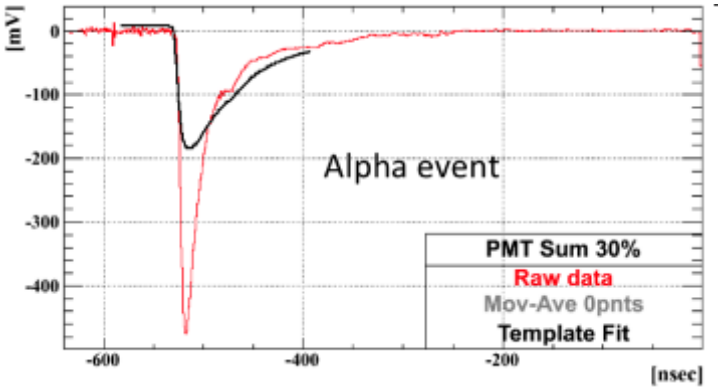
Pulse shape discrimination



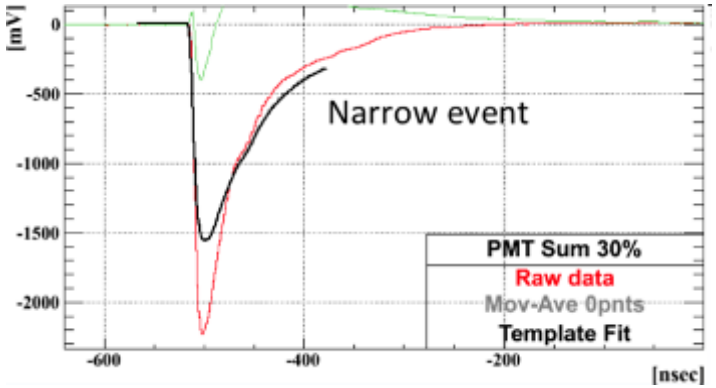
γ



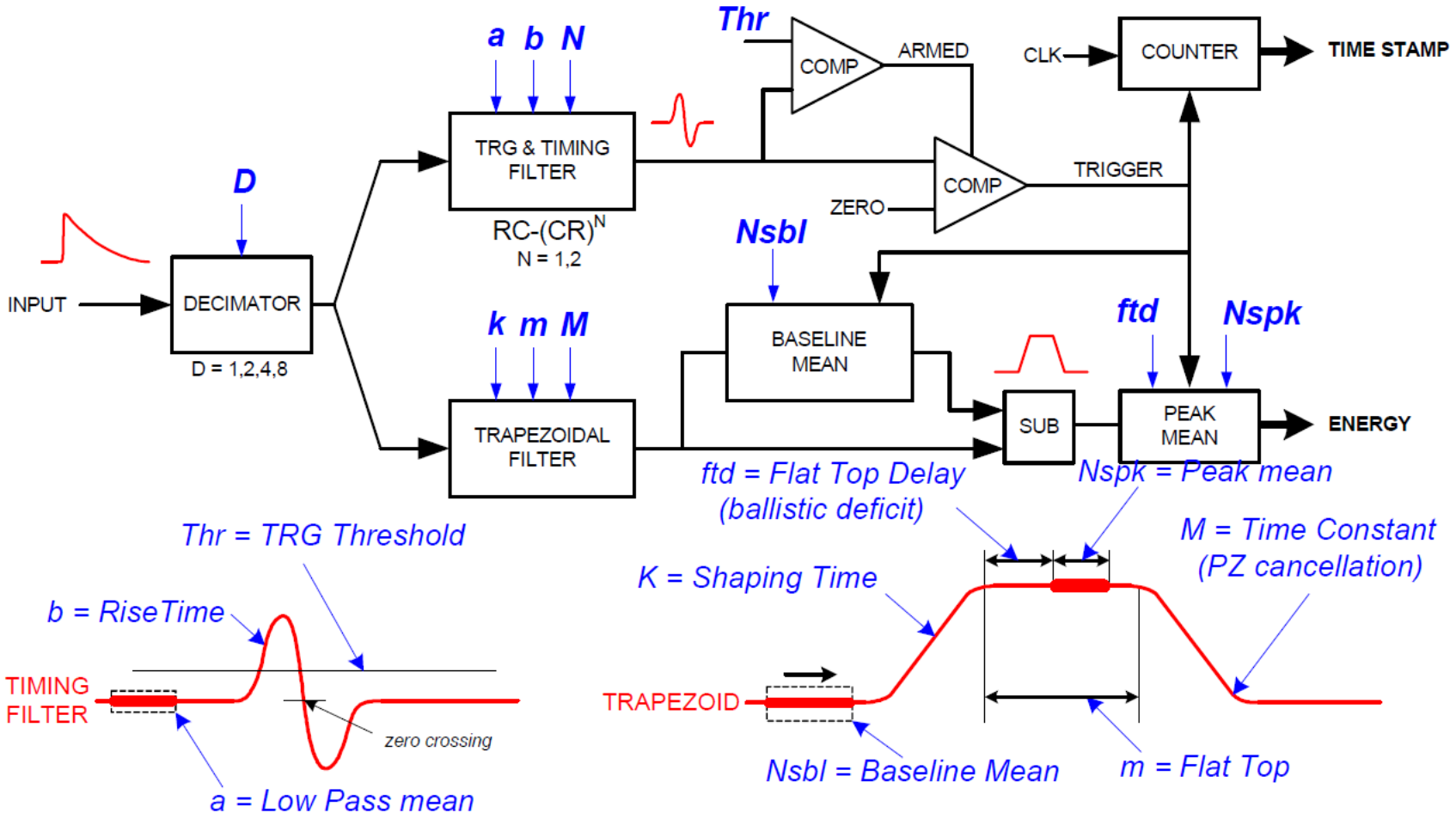
α



μ



Digital Pulse Processing (DPP)

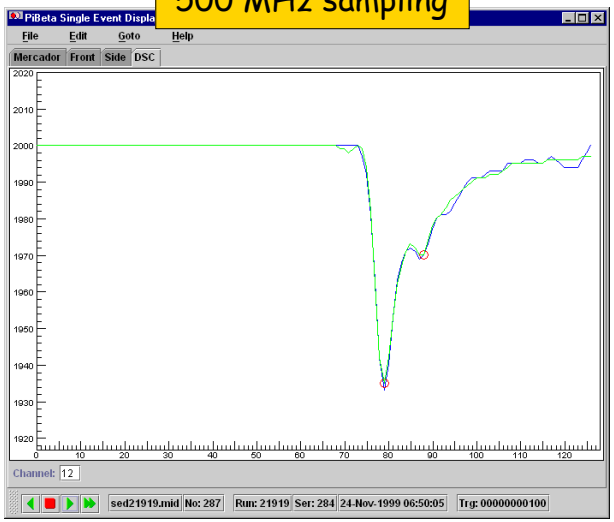


C. Tintori (CAEN)
V. Jordanov *et al.*, NIM **A353**, 261 (1994)

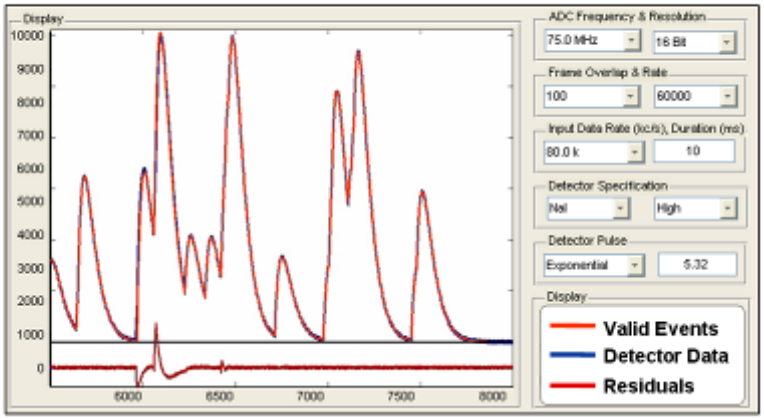
Template Fit

- Determine "standard" PMT pulse by averaging over many events → "Template"
  - Find hit in waveform
  - Shift ("TDC") and scale ("ADC") template to hit
  - Minimize χ^2
  - Compare fit with waveform
  - Repeat if above threshold
- Store ADC & TDC values

πβ Experiment
500 MHz sampling



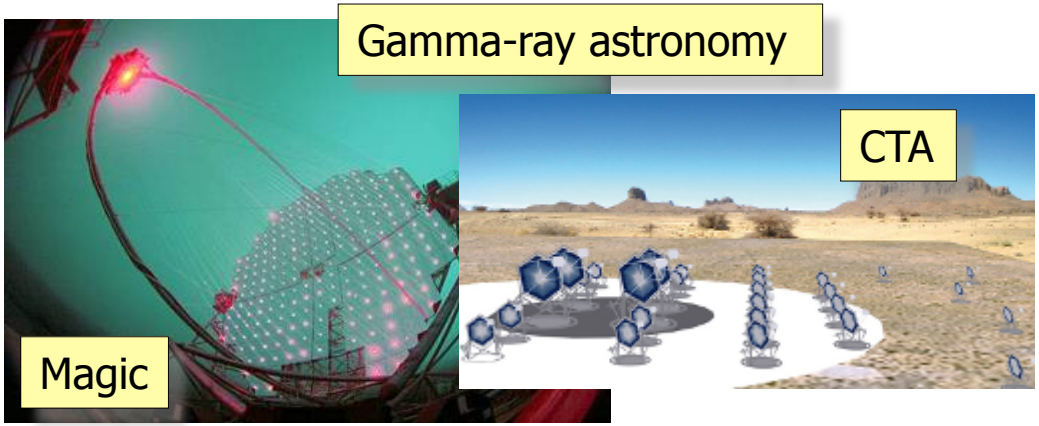
- At 1,000 kc/s less than 10% of events cannot be decoded.

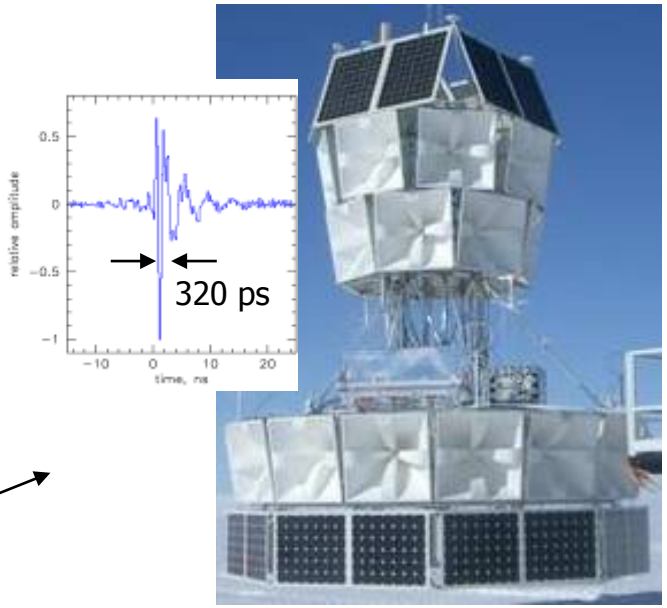


14 bit
60 MHz

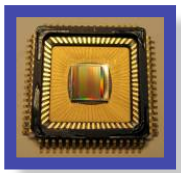
Other Applications

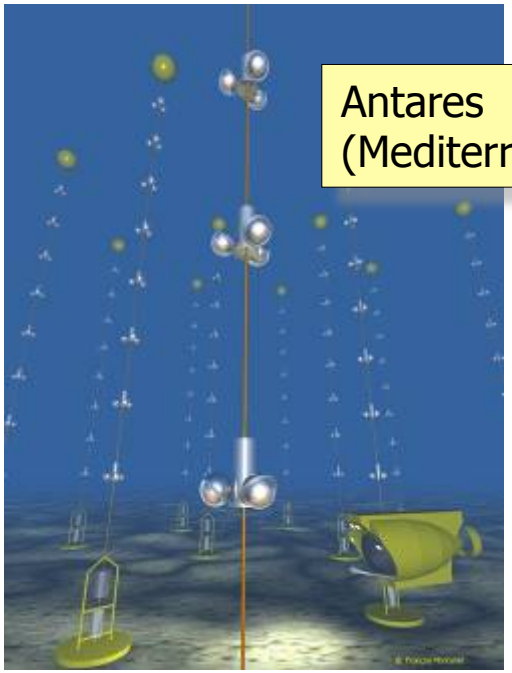
Gamma-ray astronomy





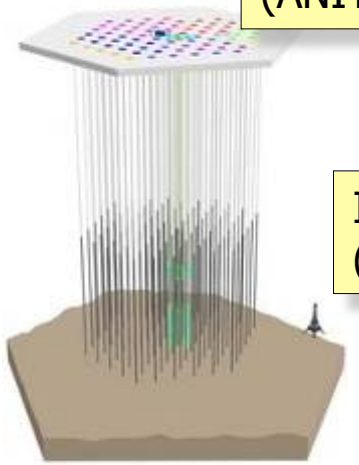
Antarctic Impulsive Transient Antenna (ANITA)





Antares (Mediterranian)

ToF PET (Siemens)

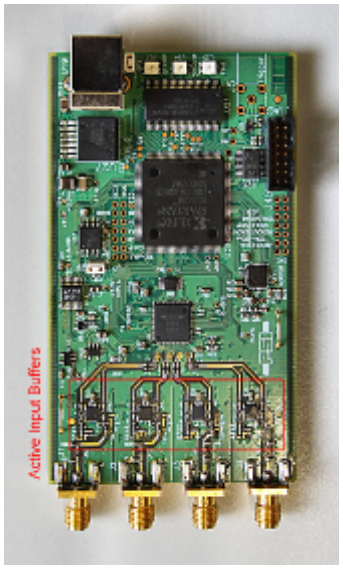


IceCube (Antarctica)

Things you can buy

- DRS4 chip (PSI)
- 32+2 channels
- 12 bit 5 GSPS
- > 500 MHz analog BW
- 1024 sample points/chn.
- 110 μs dead time

- MATACQ chip (CEA/IN2P3)
- 4 channels
- 14 bit 2 GSPS
- 300 MHz analog BW
- 2520 sample points/chn.
- 650 μs dead time

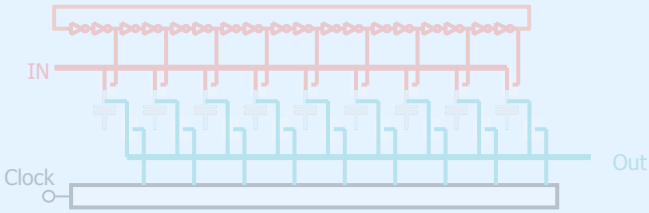


- DRS4 Evaluation Board
- 4 channels
- 12 bit 5 GSPS
- 750 MHz analog BW
- 1024 sample points/chn.
- 500 events/sec over USB 2.0

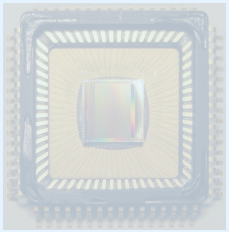
- SAM Chip (CEA/IN2PD)
- 2 channels
- 12 bit 3.2 GSPS
- 300 MHz analog BW
- 256 sample points/chn.
- On-board spectroscopy

Part 3

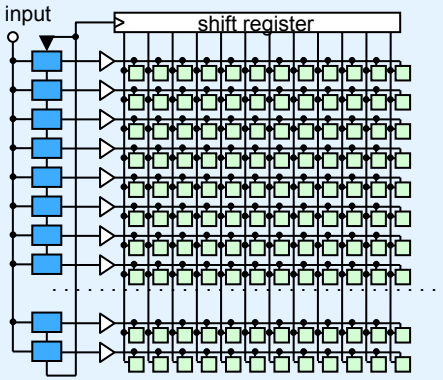
- Design Principles and Limitations



- Overview of Chips and Applications



- Future Design Directions



How to fix timing nonlinearity?

- LAB4 Chip (G. Varner) uses "Trim bits" to equalize inverter delays to < 10 ps
- Dual-buffer readout for decreased dead time
- Wilkinson ADCs on chip

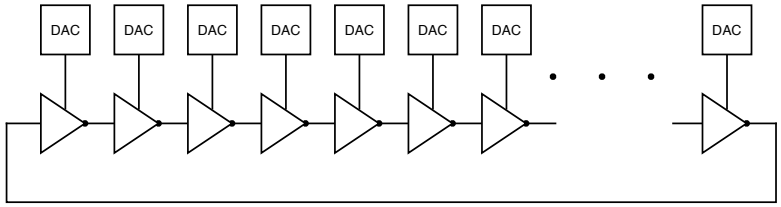
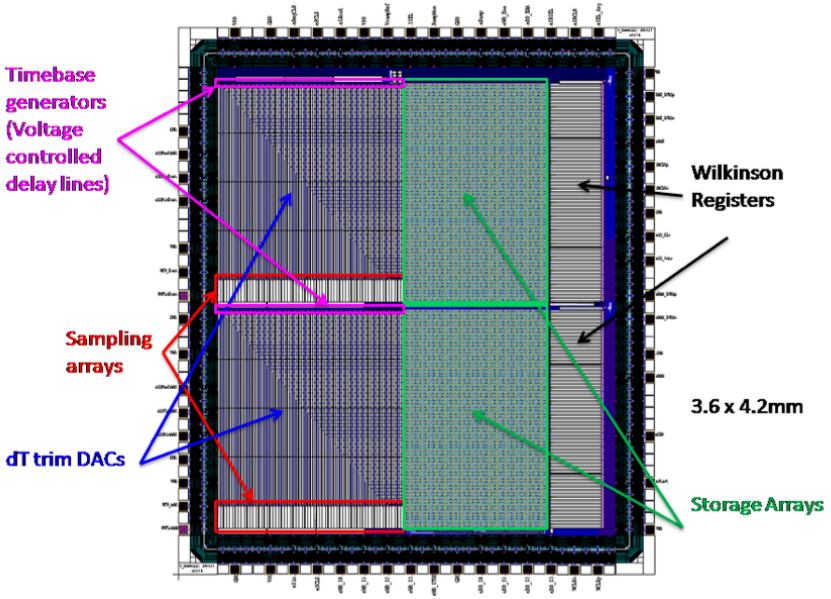


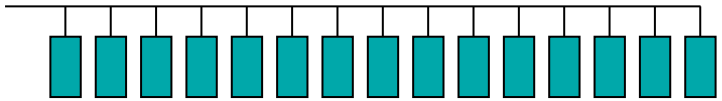
TABLE I
PERFORMANCE SPECIFICATIONS FOR THE LAB4 ASIC.

Specification	Parameter
4096	samples/channel
1	channel/ASIC
$\leq$ 10	ps residual timebase error
$\sim$ 10	bits resolution (12-bits ADC)
256	samples convert window ($\sim$64ns)
4	GSa/s sampling
$\leq$100	μs to read all samples
$\geq$1k	Hz sustained readout (multibuffer)



First tests will be reported on RT12 conference June 11-15, Berkeley, CA

Next Generation SCA



Short sampling depth ⟷ Deep sampling depth

- Low parasitic in… capacitance
- Wide input bus
- Low R_{on} write switches

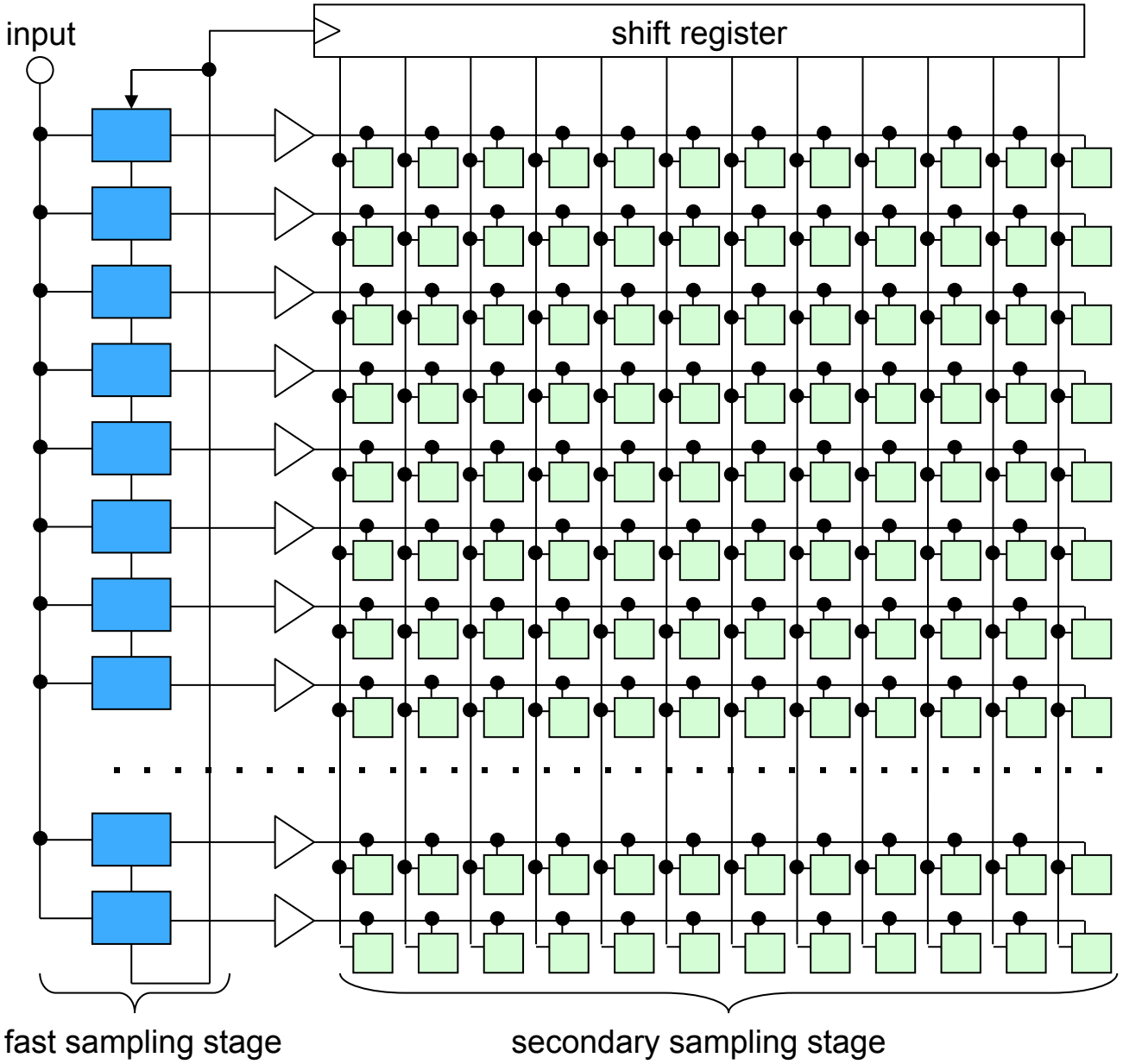
  → High bandwidth

How to combine best of both worlds?

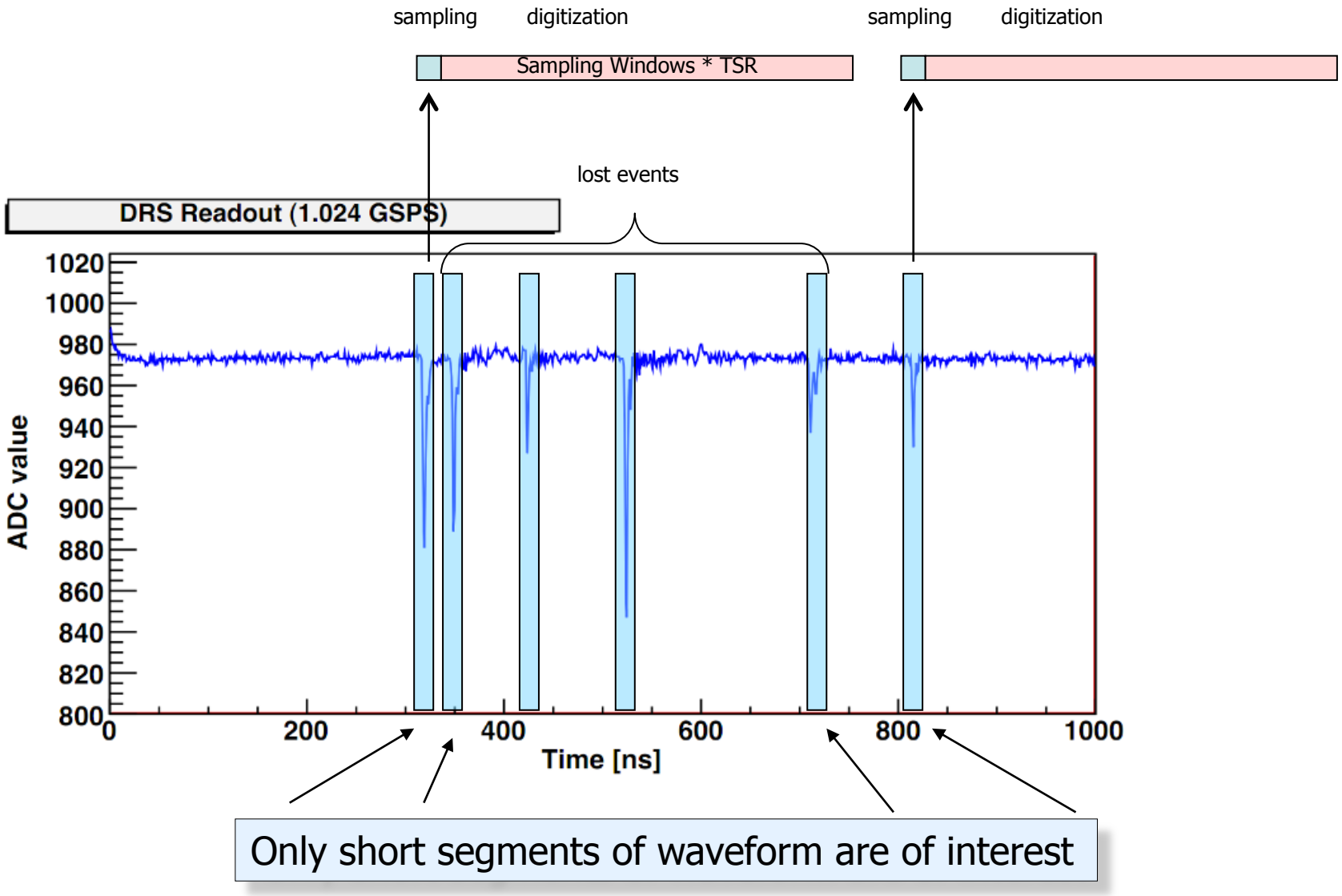
- …long waveforms
- …modate long trigger delay
- Faster sampling speed for a given trigger latency

Cascaded Switched Capacitor Arrays

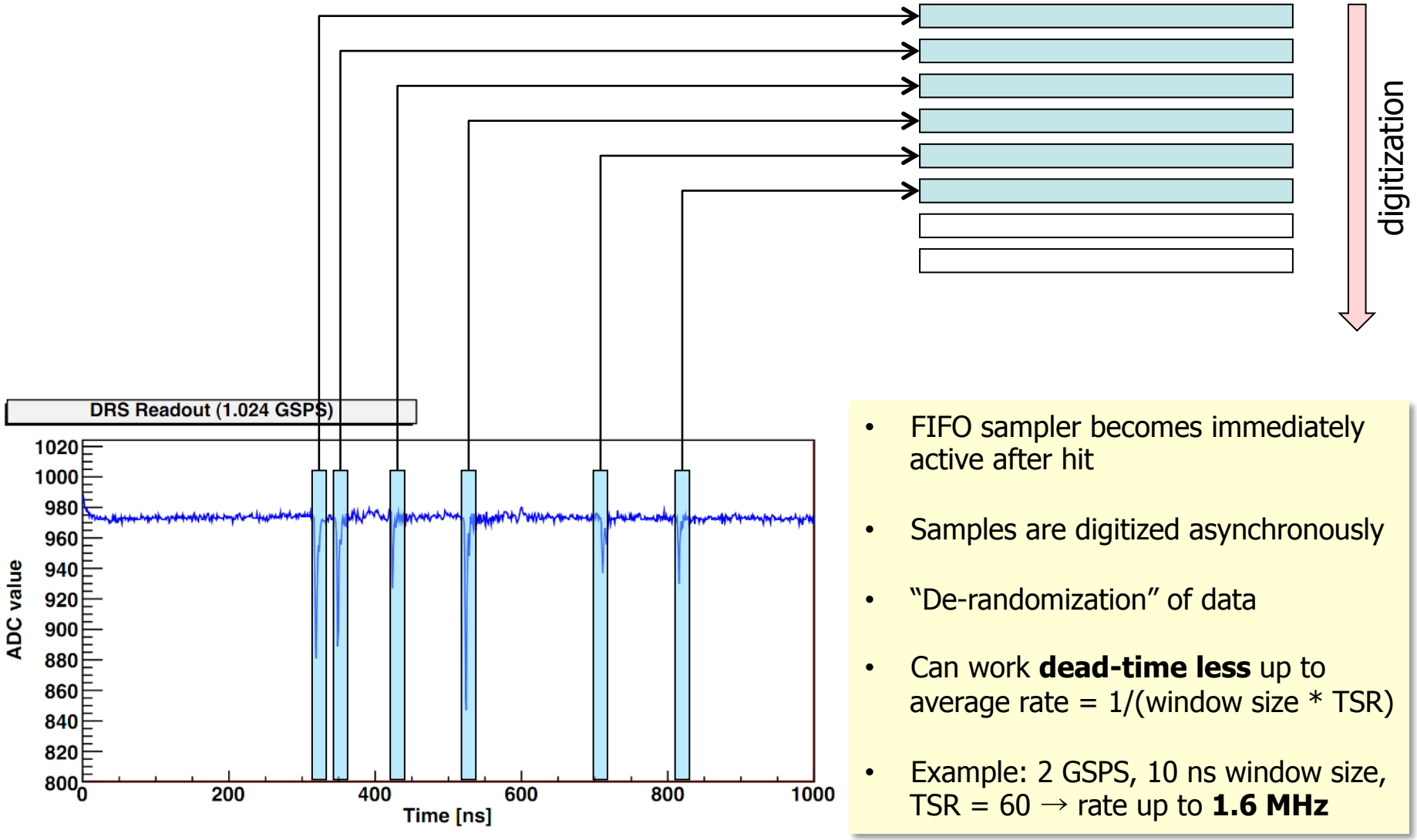
- 32 fast sampling cells (10 GSPS)
- 100 ps sample time, 3.1 ns hold time
- Hold time long enough to transfer voltage to secondary sampling stage with moderately fast buffer (300 MHz)
- Shift register gets clocked by inverter chain from fast sampling stage



The dead-time problem



FIFO-type analog sampler



- FIFO sampler becomes immediately active after hit
- Samples are digitized asynchronously
- "De-randomization" of data
- Can work **dead-time less** up to average rate = 1/(window size * TSR)
- Example: 2 GSPS, 10 ns window size, TSR = 60 → rate up to **1.6 MHz**

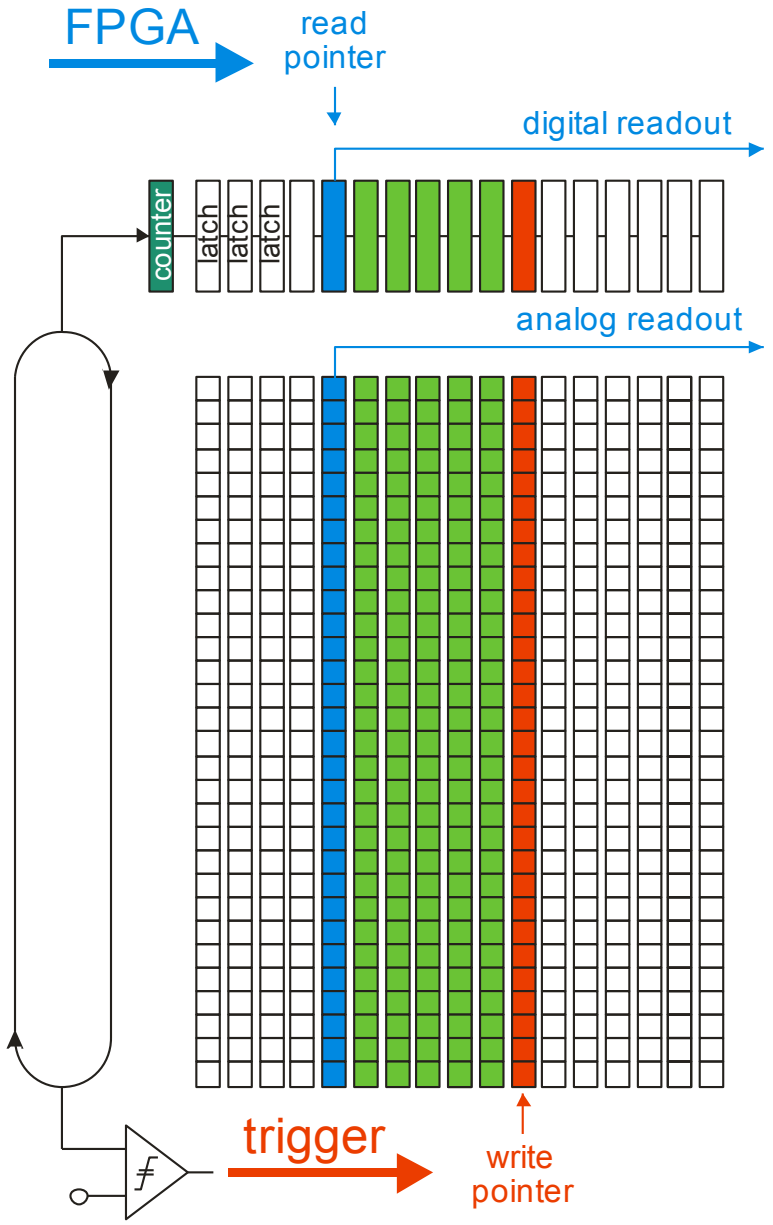
Plans

DRS5 (PSI)

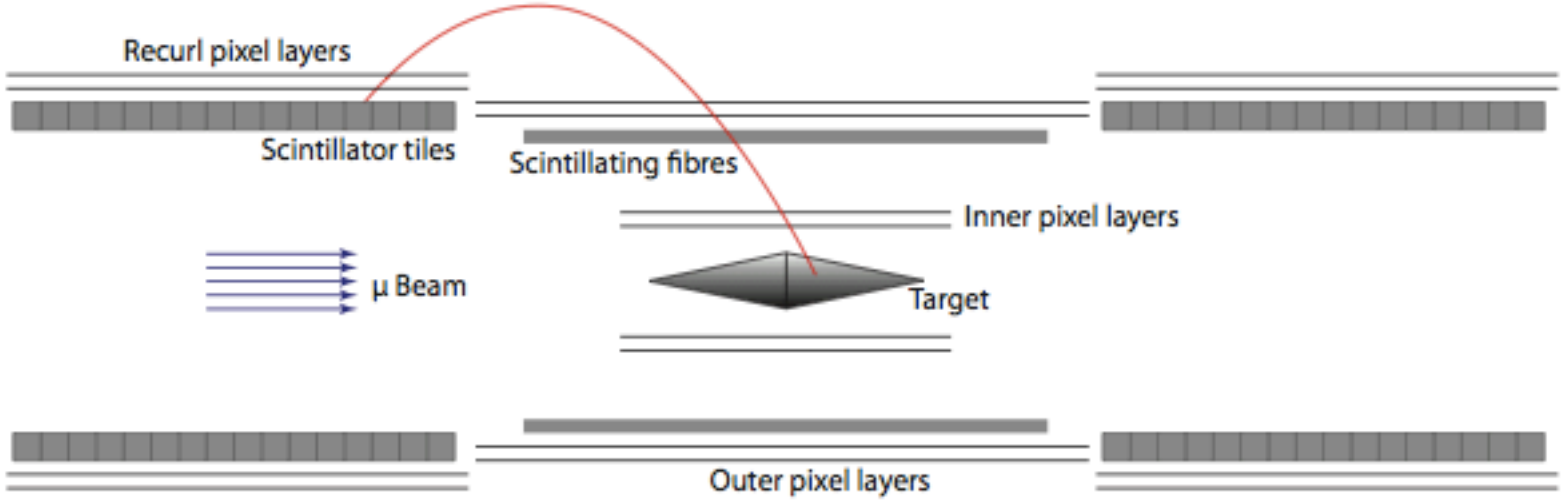
- Self-trigger writing of 128 short 32-bin segments (4096 bins total)
- Storage of 128 events
  - Accommodate long trigger latencies
  - Quasi dead time-free up to a few MHz,
  - Possibility to skip segments
    → second level trigger
- Attractive replacement for CFG+TDC
- First version planned for 2013

CEA/Saclay

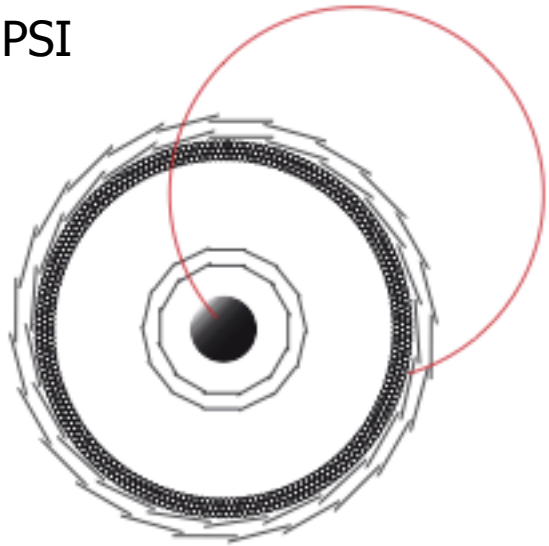
- Dual gain channels
- Dynamic power management (Read/Write parts)
- Region-of-interest readout



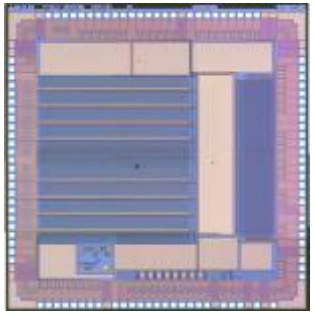
$\mu^+ \rightarrow e^+e^-e^+$



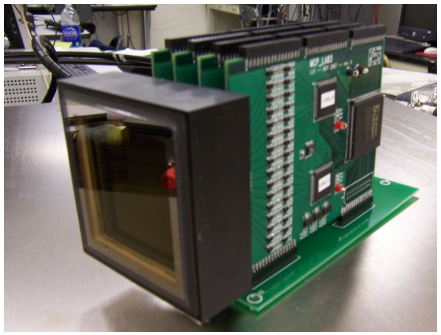
- Mu3e experiment planned at PSI with a sensitivity of 10^{-16}
- $2*10^9$ μ stops/sec
- Scintillating fibres & tiles
  - 100ps timing resolution
  - 2-3 MHz hit rate
- Can only be done with DRS5!

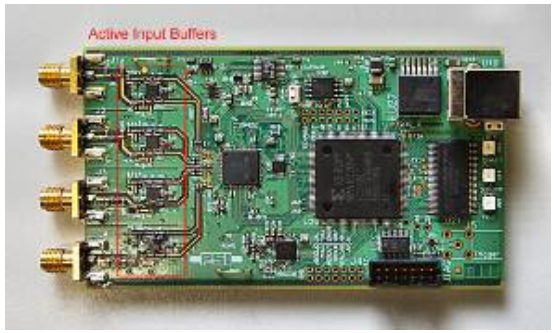


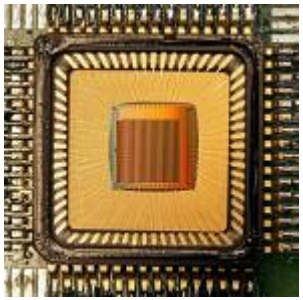
Conclusions

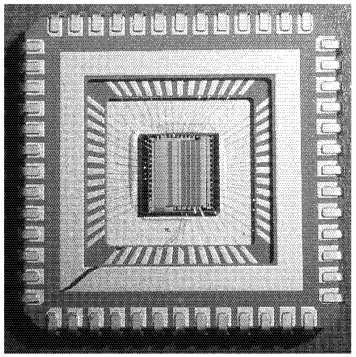


- SCA technology offers tremendous opportunities
- Several chips and boards are on the market for evaluation
- New series of chips on the horizon might change front-end electronics significantly









SCA Usage


Greenland
Iceland
Suomi
Finland
Norge
Россия
Russia
Canada
United
States
Mongolia
China
S Korea
Japan
Thailand
Indonesia
Papua New
Guinea
Australia
South
Pacific
Ocean

Profit from the true magician!