High Accuracy Injection Circuit for the Calibration of a Large Pixel Sensor Matrix

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Introduction

- Pixel sensor readout chips require a fine-tuning of readout sensitivity at pixel-level, which can be obtained simply by injecting a well-known signal into each individual readout channel.
- Such a simple procedure can be an issue in a high-granularity large pixel matrix with complex signal processors.
- This work presents the experimental results from the circuit characterization of the second version of a high accuracy injection circuit to be used for in-pixel calibration of large pixel sensor matrices.
- Compared to the first version of the circuit[1][2], the one presented in this work shows, in particular, a reduced in pixel area occupation.
- In a large sensor matrix the circuit provides a useful means for precise calibration of the readout electronics of the pixel cell unit for both monolithic active pixel sensors and hybrid pixel detectors.
- In the latter case the injection circuit is particularly useful to test the functionality of the readout electronics already at the chip level, when no sensor is connected to the chip.

Injection Circuit Architecture

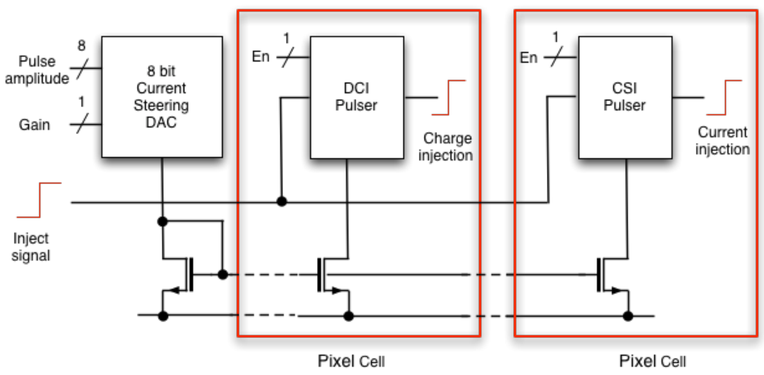
The injection circuit, belonging to a CMOS commercial process by **IBM** with **130 nm** minimum feature size and maximum supply voltage V_{DD}=1.2 V, allows for two injection:

- **in the Direct Charge Injection (DCI)** mode, the circuit feeds a charge at the input of the preamplifier for charge-sensitive amplification;
- **in the Current Steering Injection (CSI)** mode, the input of the readout electronics is fed with a known current provided by the injection circuit. This solution can be used both for transresistance readout and for charge amplifier calibration by steering the current into the preamplifier input during a fixed time interval.

Injection Circuit main properties:

- Since the proposed circuit will be part of an ASIC known as DSSC chip under development for the European XFEL facility, it has been designed with the following features
- It is required to **inject either a charge or a current** at the input of the front-end electronics.
- It must be able to cover the full dynamic range of the signals delivered by the sensor (100 fC in DCI mode and 25 uA in DCR mode), with at least 1 point into the lowest energy level (<0.36 fC in SFR mode and <0.1 uA in CSI mode).
- The proposed architecture is based on a DAC designed for an Integral Non Linearity (INL) error smaller than 0.5 LSB, then the Differential Non Linearity (DNL) is always smaller than 1 LSB which ensures that the converter is monotonic.

The proposed circuit consists of two main parts: one hosted by the pixel cell itself and one shared by all pixels and located in the chip periphery.



Conceptual block diagram of the injection circuits

- The pulse amplitude can be selected with an 8-bit current steering DAC, in the periphery of the chip. In order to meet the requirements concerning the range and resolution of the injected signal without increasing the DAC complexity and area, an additional bit for selectable gain has been introduced.
- The current provided by the DAC is mirrored into each pixel where a pulser circuit generates a signal corresponding to the one delivered by the DEPFET:
  - **DCI pulser** injects a charge directly into the input of the amplifier by applying a voltage step to a small injection capacitor;
  - **CSI pulser** injects a current at the drain of the input cascode.
- Signal injection into each pixel can be enabled with a local control bit set by means of the kill mask which consists of 64x64 bits pushed into the matrix by means of a shift register connecting all the pixels in a row-by-row fashion.
- A complete test structure was submitted to the foundry, and a complete characterization in term of linearity and noise has done.

References

1 E. Quartieri; M. Manghisoni: "Performance of a High Accuracy Injection Circuit for in-Pixel Calibration of a Large Sensor Matrix "; Nuclear Science Symposium Conference Record (NSS/MIC), 2011 IEEE.

2 E. Quartieri; M. Manghisoni: "High precision injection circuit for in-pixel calibration of a large sensor matrix"; Ph.D. Research in Microelectronics and Electronics (PRIME), 2011 7th Conference on; 2011 , Pages: 73 – 76.

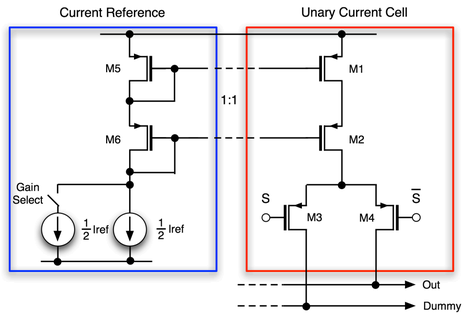
8-bit Current Steering DAC

The 8-bit Current Steering DAC switches k out of 2^8-1 unity current generators toward the output node or to a dummy load under the control of the 8-bit digital input. A **current-steering topologies** based on **binary weighted architecture** has been used.

Unit current cell

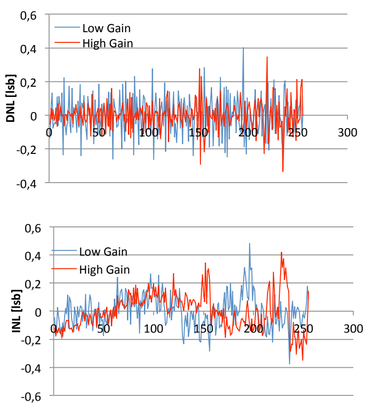
The unit current cell consists of a cascoded current source (M1, M2) and current-steering switches (M3, M4).

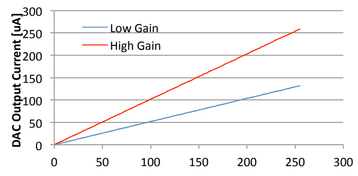
- The current generated by the reference (I_{ref}=0.5 uA in low gain and I_{ref}=1 uA in high gain) is mirrored into each unary current cell by means of a 1:1 cascode current mirror.
- The current-steering switches send the current to the output when phase S is low, and to the dummy load when S is high.



Switching scheme for the unary current source

Measurement Results



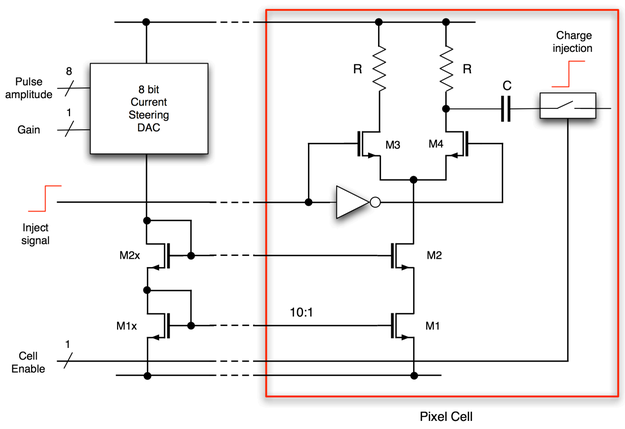


	Low Gain	High Gain
I_{MIN} [µA]	0.495±0.048	1.026±0.071
I_{MAX} [µA]	131.08±6.3	258.20±10.40
I_{LSB} [µA]	0.51±0.025	1.01±0.041
$\sigma I_{LSB}/I_{LSB}$ [%]	4,81	4,02
DNL_{max} [LSB]	0.45±0.10	0.44±0.09
INL_{max} [LSB]	0.42±0.06	0.44±0.05

In the right column: Output current as a function of the input DAC code both in the low and high gain setting; in the left column: DNL and INL as a function of input DAC code.

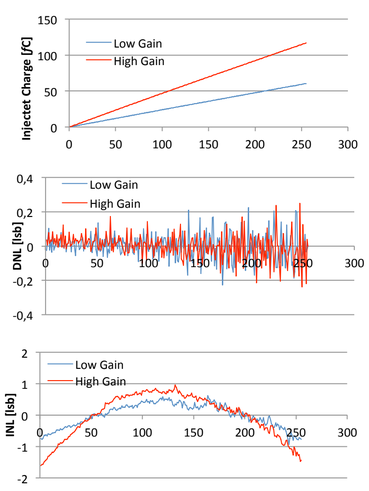
DCI Mode

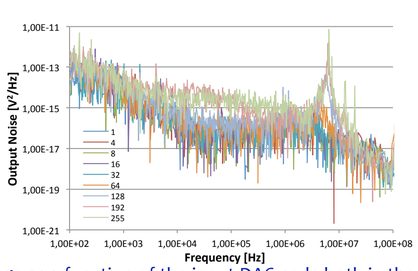
The pulser injects a charge into the input of the amplifier by applying a voltage step to a small injection capacitor. The current from the 8-bit DAC is mirrored into each pixel by means of a 10:1 mirror, then it is switched from the left branch of the differential stage to the right one to produce the negative voltage step.



Simplified block diagram of the DCI pulser architecture

Measurement Results



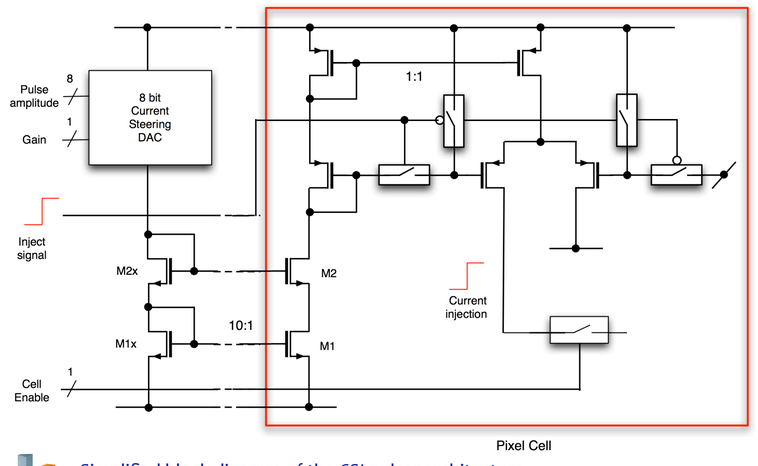


	Low Gain	High Gain
Q_{MIN} [fC]	0.207±0.041	0.418±0.026
Q_{MAX} [fC]	57.6±4.8	112.59±8.2
Q_{LSB} [fC]	0.226±0.019	0.442±0.032
$\sigma Q_{LSB}/Q_{LSB}$ [%]	8,3	7,3
DNL_{max} [LSB]	0.46±0.12	0.49±0.15
INL_{max} [LSB]	0.94±0.33	1.18±0.36

In the left column: Output Charge as a function of the input DAC code both in the low and high gain setting, together with the corresponding DNL and INL; in the right column: output noise spectrum.

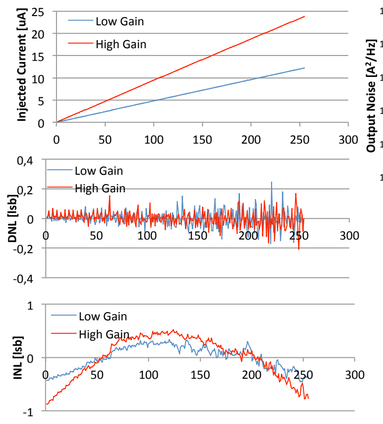
CSI Mode

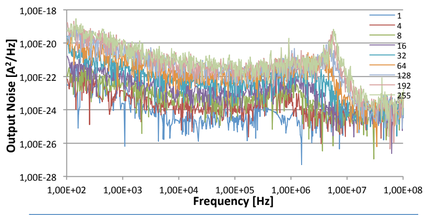
The pulser injects a current step into the drain of the input cascode which is a low impedance virtual ground. The current from the 8-bit DAC is mirrored into each pixel by means of a 10:1 cascode current mirror, then it is mirrored once again by means of a 1:1 mirror to obtain the right polarity of the signal to be injected. Mirrored current is switched from the right branch of the differential stage to the left one to produce a current step applied to the drain of the input cascode. Due to the low voltage budget a solution in which the cascode current mirror and the differential switch share a transistor has been adopted.



Simplified block diagram of the CSI pulser architecture

Measurement Results





	Low Gain	High Gain
I_{MIN} [nA]	43.50±4.25	88.74±6.73
I_{MAX} [µA]	12.23±0.61	23.78±0.87
I_{LSB} [nA]	47.98±2.37	93.27±3.39
$\sigma I_{LSB}/I_{LSB}$ [%]	4,94	3,63
DNL_{max} [LSB]	0.43±0.13	0.40±0.09
INL_{max} [LSB]	1.03±0.57	1.08±0.43

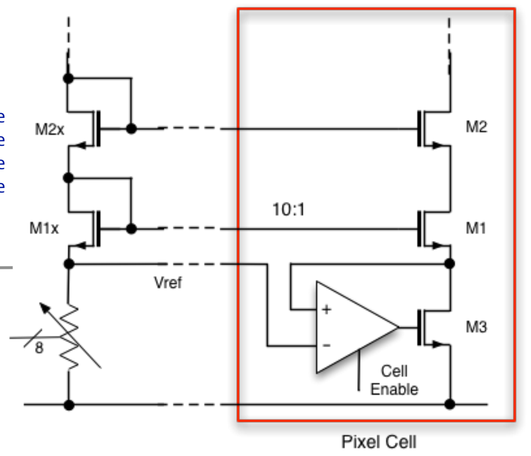
In the left column: Output current as a function of the input DAC code both in the low and high gain setting, together with the corresponding DNL and INL; in the right column: output noise spectrum.

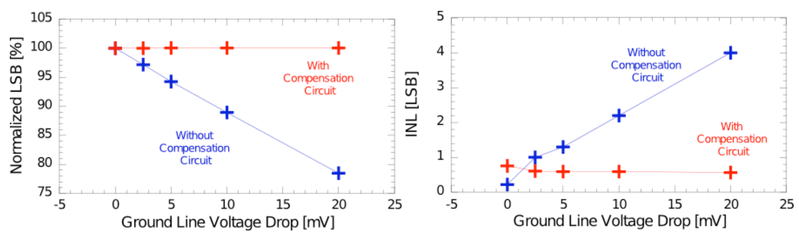
Voltage Drop Compensation

The current provided by the 8-bit DAC in the chip periphery is mirrored inside each pixel by means of a current mirror. A voltage drop of few mV along the ground line causes that the first and last pixels in column obtain different reference current. This aspect has a detrimental effect in terms of INL and DNL performance in particular for the cells far away from the chip periphery.

This problem has been overcome by transferring a reference voltage in each pixel.

Schematic of the circuit used for the compensation of the voltage drop on the reference ground line





Measurement of the Voltage Drop Compensation Circuit: in the left graph the normalized value of the LSB as a function of the voltage drop on the ground line both with and without compensation circuit; in the right graph the value of the INL of the output current of the CSI Pulser in the same condition.