Development of thin pixel detectors on epitaxial silicon for HEP experiments

FONDAZIONE BRUNO KESSLER

INFN Istituto Nazionale di Fisica Nucleare

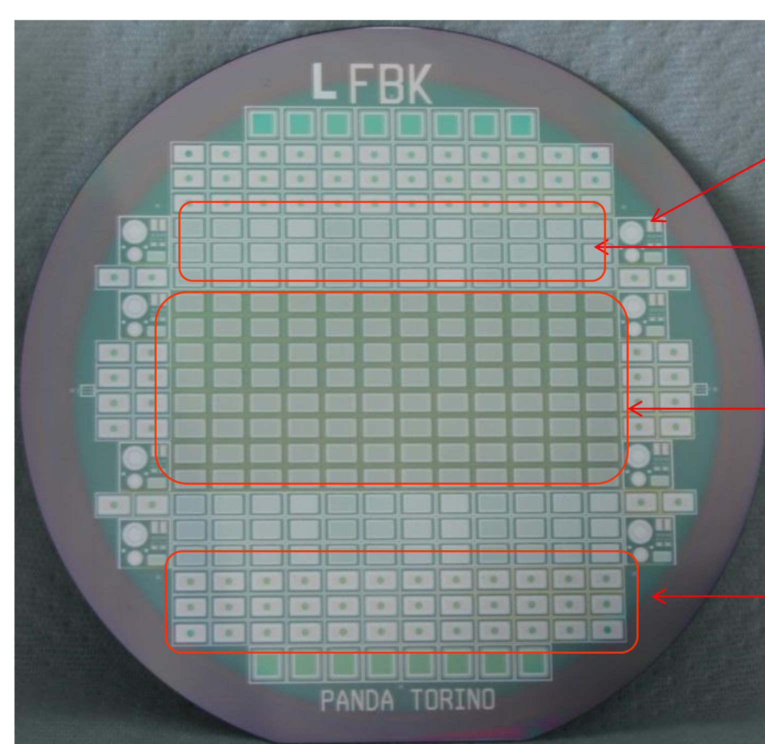
Maurizio Boscardin[a], Daniela Calvo[b], Gabriele Giacomini[a], Sabina Ronchin[a], Richard Wheadon[b], Nicola Zorzi[a]
[a] FBK, Trento - Italy , [b] INFN sez. Torino, Italy

Introduction

The foreseen luminosity of the new experiments in High Energy Physics will require that the next generation of vertex detectors will be able to sustain fluencies up to $1x10^{16}$ cm^{-2} and also to minimize the material budget of the detectors.

Thin pixel devices on epitaxial material are a natural choice to fulfill these requirements due to their rad-hard performances and low active volume. We present an R&D activity aimed at developing a new thin hybrid pixel device in the framework of PANDA experiment. The detector is a p-on-n pixel sensor realized starting from epitaxial silicon wafers, in which the sensitive area is the epi-layer itself, while the low-resistivity substrate acts as a mechanical support. After completion of the fabrication, the substrate is back thinned down to a value slightly larger than the epitaxial layer thickness, which can be in the order of 50-150 µm.

Process & Layout



Test structures

Pixel-like Test Structures

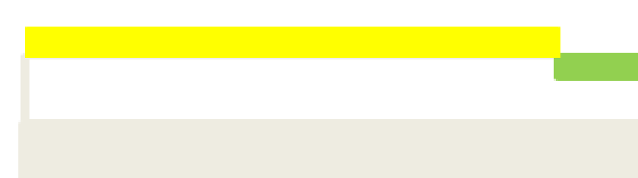
Pixel Sensors

MultiGuard Diodes

The layout is based on pixel detectors for the first single chip assembly prototypes targeted to PANDA experiment.

The realization of the device consists in:

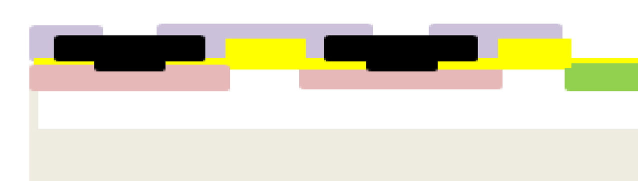
- ✓ Standard planar pixel detector fabrication
- ✓ bump-bonding and subsequent thinning of the sensor, leaving about 20µm of heavily doped silicon which is used as an ohmic contact.



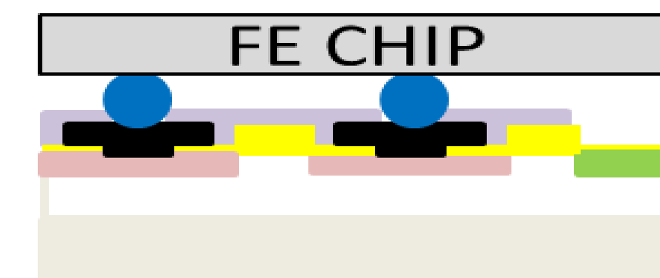
1. *Oxidation 800nm*
   Define scribe line
   N^+ implant

2. *Define diode*
   P^+ implant
   Oxidation 20nm

3. *Define contact*
   Deposit & Define metal



4. *Deposit Oxide 500nm*
   Define passivation
   Sintering

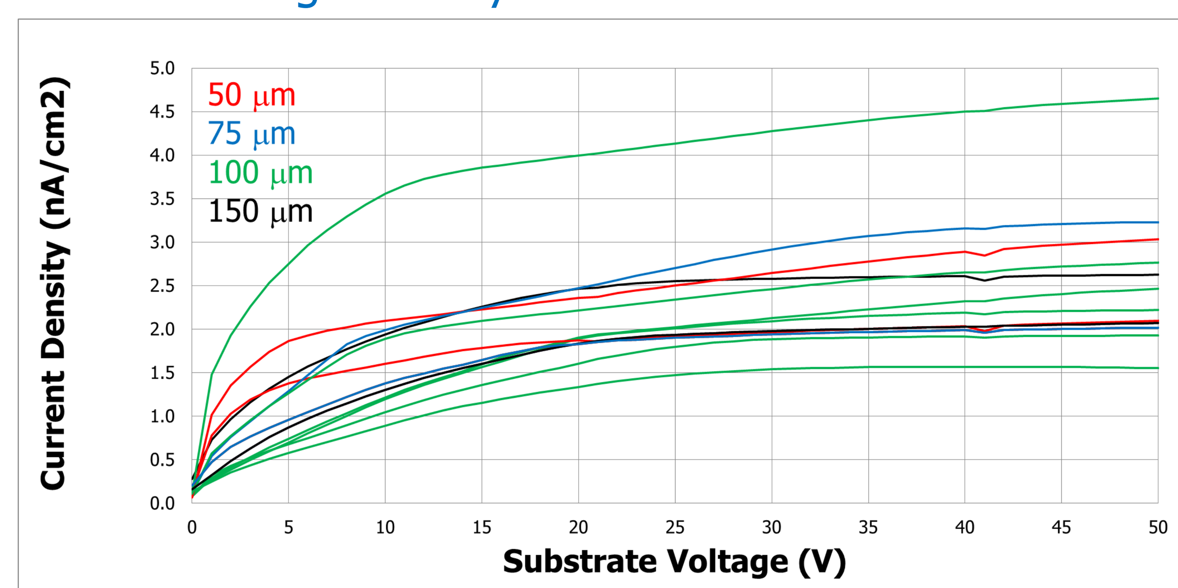


5. *Bump bonding*

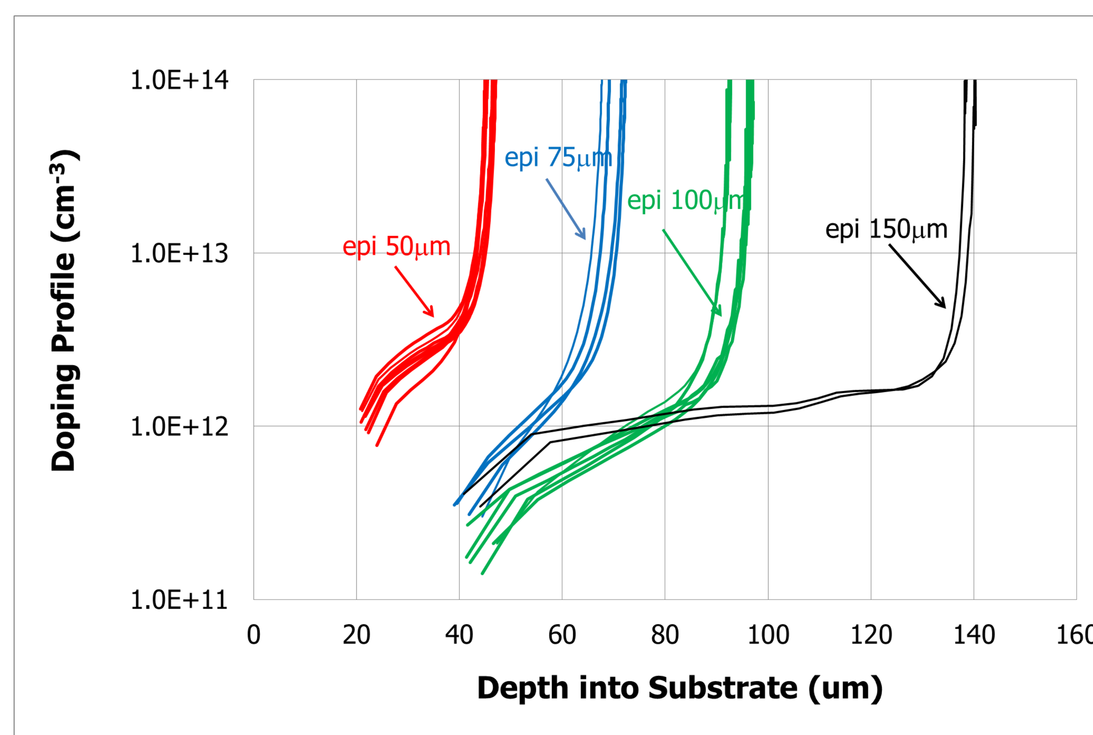
6. *Wafer thinning*

Electrical characterization BEFORE thinning

- Tau (generation time): 3 – 10 *ms*
- Surface generation velocity: 2 – 4 *cm/s*
- Oxide charge density: 0.6 – 3 10^{11} cm^{-2}

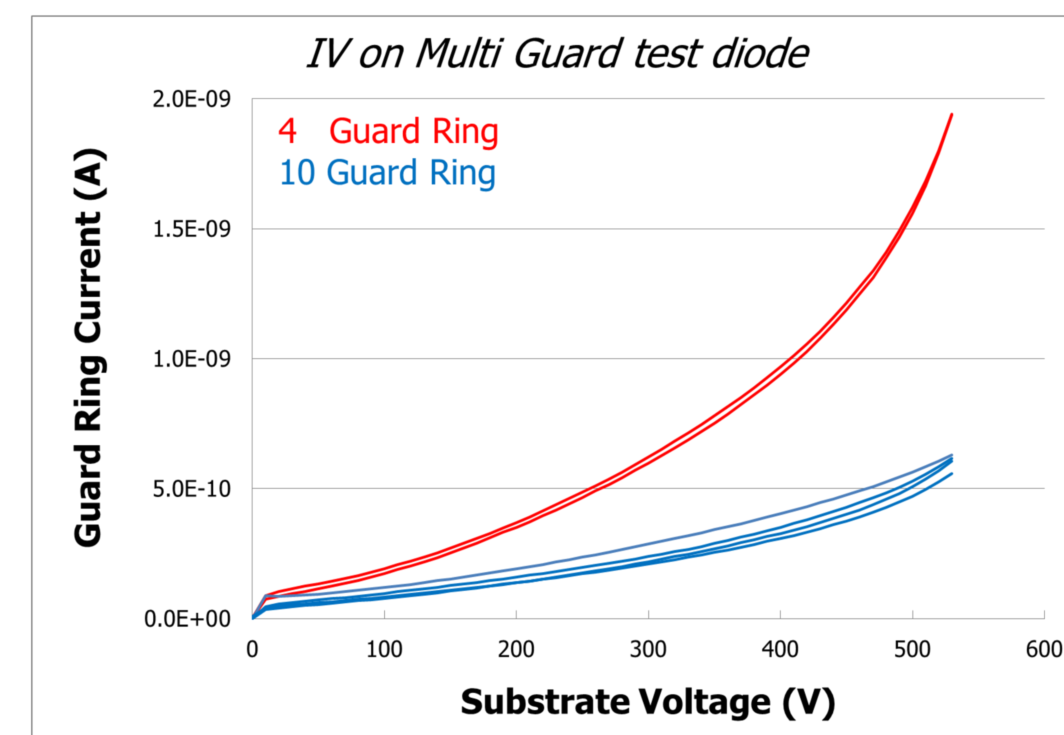


- ✓ I-V of 4mm² test diodes on 50, 75, 100 and 150 µm epi silicon wafers
- ✓ The leakage currents show a spread in the range from 1 to 4 nA/cm² and seem to be not dependent on the epi thickness



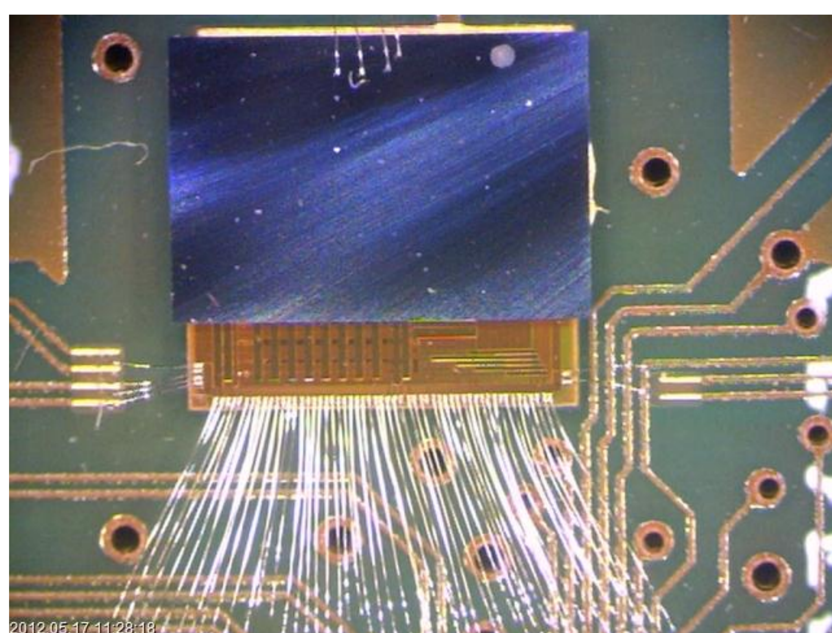
- ✓ epitaxial depth extracted from C-V on test diodes
- ✓ At FBK have been processed wafers with different thicknesses of the epi-layers on the Cz substrate
- ✓ The epitaxial wafers have been provided by ITME (Warsaw)

Electrical characterization AFTER thinning



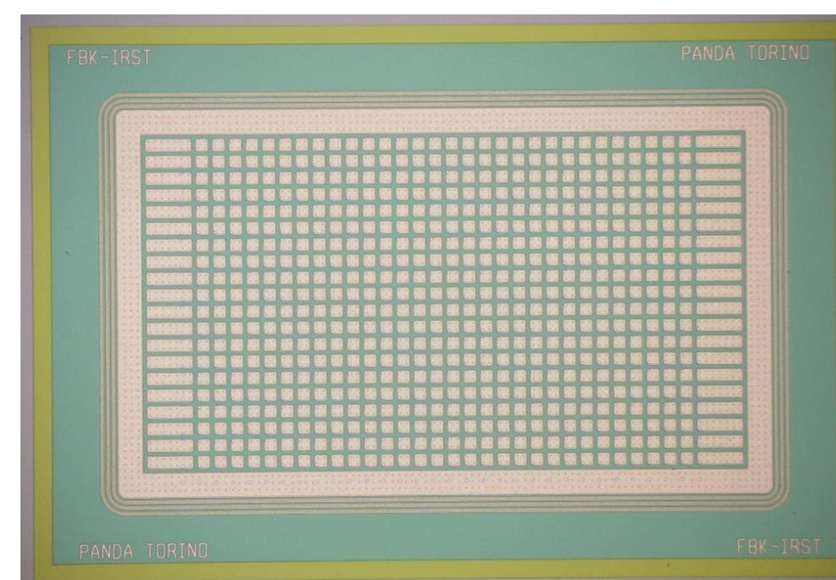
- ✓ Multi Guard Ring Diodes on thinned wafers (epi thickness: 50µm)
- ✓ High Breakdown Voltage equal before and after thinning
- ✓ No degradation of the electrical parameters

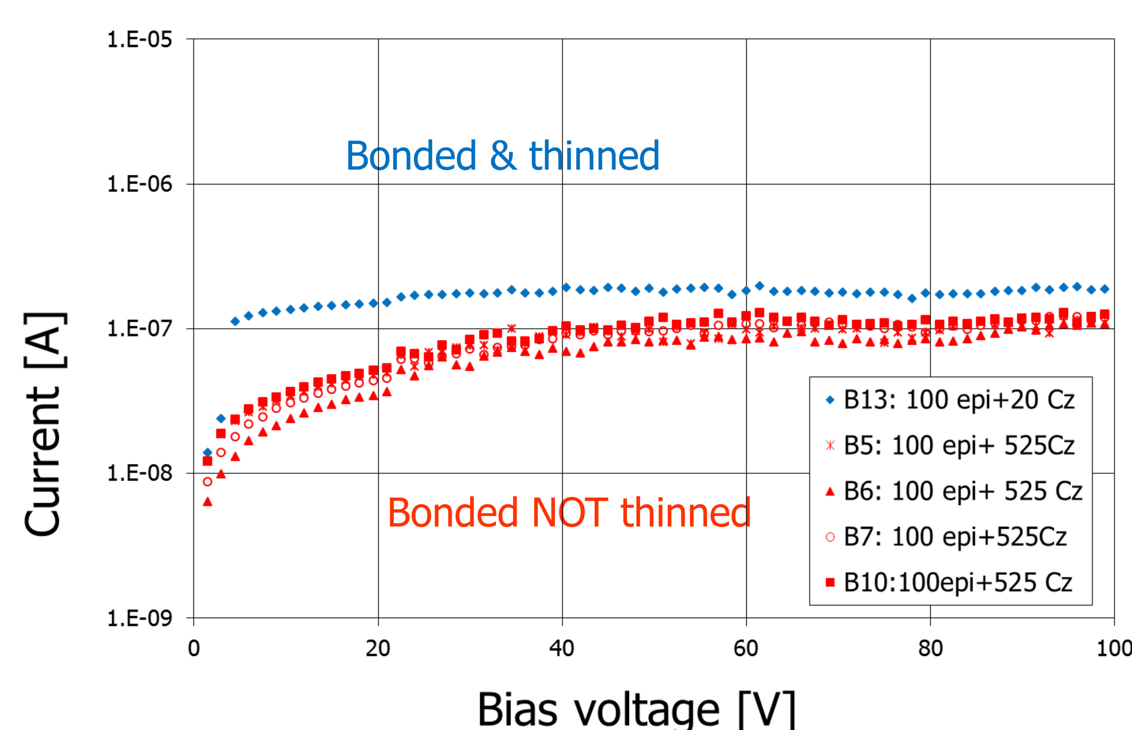
Characterization after bumping and thinning



- wafer thinning and bump-bonding by IZM
- The readout chip is ToPix_v3 (developed @INFN-Torino)

The sensor is composed by 32X20 pixels (pitch 100 µm x 100 µm)





- ✓ IV measurements of bump bonded sensors as obtained with (blue) or without (red) thinning process. Each prototype includes 640 pixels.
- ✓ The mesurement does not show a breakdown up to 100 V (typical V_{depl}~few volts).
- ✓ The observed difference of the two measured leakage currents is in the range of typical spread evaluated by test structures.
- ✓ New thinned detectors will be delivered in June and additional measurements are planned.
- ✓ More statistics will help to understand the bumping and thinning processes reliability.

Conclusions and Perspectives

- Capability to get thinned detectors starting from epitaxial silicon wafers
- The final thickness includes the epitaxial layer plus 10-20µm of the heavily doped substrate.
- The device doesn't show a worsening of the electrical parameters after bumping and thinning processes.

Further developments:

- ✓ Optimize thinning procedure
- ✓ Use of oxygen-enriched epi material
- ✓ Radiation test