Analog Front-end electronics for the outer layers of the SuperB SVT: design and expected performances

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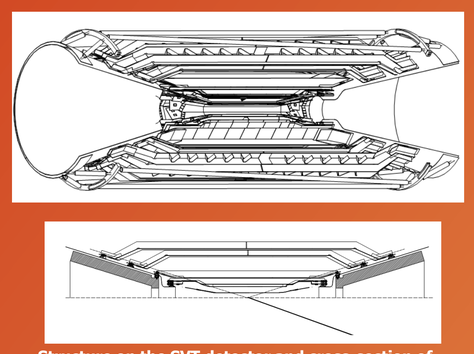
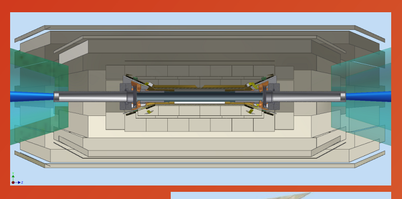
The SuperB Silicon Vertex Tracker (SVT) Detector

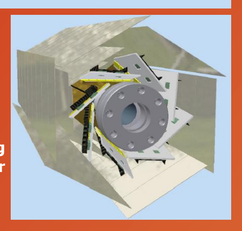
The Silicon Vertex Tracker (SVT) of the new SuperB collider will be composed of 6 different detector layers. The innermost layer (L0) will be composed by striplets or pixels; the other 5 detector layers will be double-sided long-strip detectors. The strip geometries and the foreseen hit-rates will change according to the different layers. As a consequence, different optimization of the analog read-out electronics are needed in order to provide high detection-efficiency and low noise level in the different layers. Two readout ASICs are currently developed, one for layers 0-3, another for layers 4 and 5; they differ mainly in the analog front-end.



Structure on the SVT detector and cross-section of the 6 detector layer arrangement



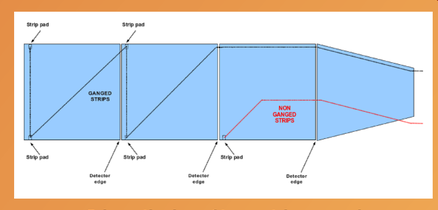
Preliminary Drawing of the SVT detector



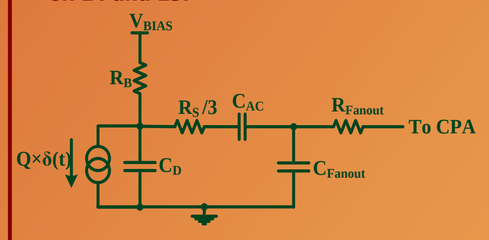
In this work, we present the design and the expected performances of the analog front-end for layers 4 and 5. For these layers, the microstrip detectors show a very high stray capacitance and high series resistance. In this condition, the noise optimization is our primary concern. A necessary compromise on the best peaking time to achieve an acceptable noise level together with efficiency and time accuracy has been found. We will present the design of preamplifier and shaper and the results of simulation of noise performance and efficiency (with the expected background rates). In addition, the design of the Time-over-threshold (TOT) and its use to correct the time-walk of the event trigger is discussed as well as the achievable timing accuracy of the circuit.

The foreseen strip detector for the SVT outer layer

In order to reduce the number of channels to be readout, more strips in the outer layers (L4, L5) will be connecter to the same electronic channel. This solution (referred as ganging in the following) becomes mandatory in particular for the Z-side of L4 and L5, where the number of strips becomes increasingly high due to the much higher barrel length. Ganging the strip is necessary, not only to reduce the number of electronic channels, but mainly to limit the number of connections between the detector and the processing electronics. An example of the connection between 2 strips is shown in the figure. It is foreseen that up to 3 strip will be ganged on L4 and L5.



Schematic view of two z strips ganged through the fanout circuit.



The detector will be implemented with 300um silicon thickness, and the strip will be AC biased on both sides.
In order to simulate the strip behavior with the electronic channel, a simplified model of the strip has been developed. Such model foresees the total strip capacitance (C_D), the biasing resistor (R_B) the strip series resistance (R_S), the strip coupling capacitance (C_{AC}). The fanout board is also included with its stray capacitance (C_{fanout}) and series resistance (R_{fanout}). The table below reports all the relevant strip parameters used for the electronics design and for the noise evaluations.

Strip side	Layer	Type	Total Strip length (cm)	C_D (pF)	R_B (MΩ)	R_S (Ω)	I_{leak} (nA)	I_{leak} (x 5 safety factor) (nA)	C_{AC} (pF)	C_{fanout} (pF)	R_{fanout} (Ω)
Phi	4	p	30.34	51.6	2.7	121	102	484	1213.6	1.5	3.2
Phi	5	p	38.04	64.7	2.5	152	44	187	1521.6	1.5	3.2
Z	4	n	15.42	26.2	2.7	46	105	513	925.2	21	53
Z	5	n	15.42	26.2	3.3	46	34	156	925.2	26	66

The Analog Channel architecture

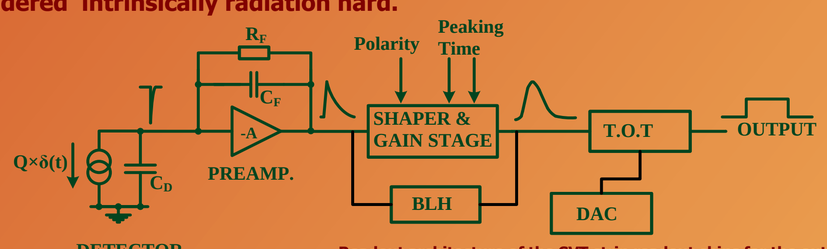
The analog section of the chip is composed by the classical processing scheme. The chosen shaping function is the third-order semi-Gaussian function implemented with complex poles.

A preamplifier provides an amplification of the signal up to the full dynamic range of the circuit (which is limited only the ASIC power supply). The preamplifier also introduces the first real-pole of the shaping function. After the preamplifier, a second stage provides a couple of conjugate complex-pole.

The circuit foresees the possibility to select the peaking time of the shaper output (between 375, 500, 750, and 1000 ns). In this way, the noise performances and the signal occupancy can be optimized according to the real background during the experiment. An inverter stage can also be included in the analog chain in order to operate with signals delivered from both n and p strips. An a-symmetric baseline holder (BLH) is also included to suppress any baseline shift and to reduce the offset at the shaper outputs due to mismatch between channels.

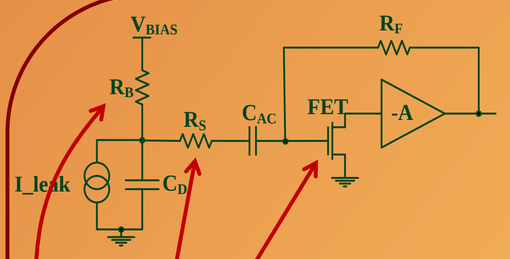
Time-Over-Threshold (TOT) detects the hit and it performs a 4-bit or 6-bit analog-to-digital conversion. The TOT is based on a simple hit discriminator with adjustable threshold.

The chosen technology for the implementation is the 130 nm CMOS process which is considered intrinsically radiation hard.



Readout architecture of the SVT strip readout chips for the outer layer.

The expected noise performance



Contribution to the ENC of the different noise sources for different peaking-time (layer 5, Phi side)

Tp(ns)	375	500	750	1000
ENC_FET	591	525	452	405
ENC_Rs	546	478	401	351
ENC_RB	262	301	360	415
ENC_Rf	648	651	653	655
ENC_Leakage	786	900	1078	1242
ENC_others	647	596	507	472
ENC_Total	**1474**	**1478**	**1530**	**1629**

Simulated total noise for: different layers, detector sides, and relevant peaking times.

Strip side	Layer	Peaking time (ns)	Total ENC nominal case (el)	Total ENC (x 5 safety factor) (el)
Phi	4	375	**1271**	**1696**
		500	**1263**	**1804**
Z	4	375	**1124**	**1607**
		500	**1113**	**1716**
Phi	5	500	**1251**	**1478**
		750	**1204**	**1530**
		1000	**1214**	**1629**
Z	5	500	**1018**	**1243**
		750	**963**	**1281**
		1000	**970**	**1378**

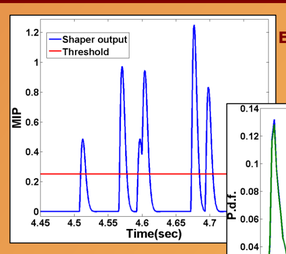
Including the increase of the leakage current due to nominal background-rate for the 7.5 year of data taking. The worst-case foresees a radiation damage due to 5 times higher background rate.

In the foreseen combinations of layers, detector sides, peaking times and leakage current , the signal-to-noise (S/N) ratio is between 13 and 24.

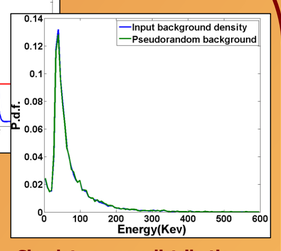
Efficiency simulation

In the analog section of the readout ASIC, the cause of inefficiency is the pile-up of the individual pulses at the output of the shaper. The different hits are identified and time stamped by the ASIC when the shaper output exceeds a pre-determined threshold. So in some pile-up cases (when the shaper does not cross the threshold multiple times), the event after the first are not identified.

The efficiency are calculated by simulating a random time distribution of hits at the input. The energy distribution, also random, follows the expected background spectrum in the different layers.



Examples of pile up.



Simulate energy distribution according background sources.

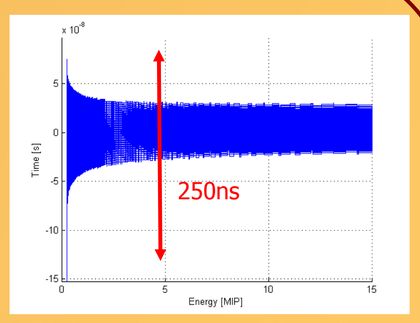
Strip side	Layer	Peaking time (ns)	Background Rate (kHz)	Efficiency	Efficiency (x 5 safety factor)
Phi	4	375	25	**98.4%**	**91.8%**
		500		**97.8%**	**89.1%**
Z	4	375	13.4	**98.9%**	**94.4%**
		500		**98.5%**	**92.6%**
Phi	5	500	16.2	**98.5%**	**92.8%**
		750		**97.8%**	**89.4%**
		1000		**97.1%**	**86.1%**
Z	5	500	8.8	**99.0%**	**95.3%**
		750		**98.6%**	**93.0%**
		1000		**98.1%**	**90.6%**

The table shows the simulation results, the efficiency drops almost linearly as the peaking-time increases. Thus, clearly a tradeoff exists between efficiency and S/N ratio.

Expected Timing accuracy

The timing information is also an important requirement because it impacts on the off-line time-windows used during the data analysis to reconstruct the tracks onto the various layers. Larger time-windows lead to higher occupancy and difficulties to discriminate between different tracks. The time accuracy is very critical in the outer layers (respect to the inner ones) where longer peaking-times suffer from severe time-walk and higher jitter (even with the same S/N as the inner layer).

The simulated time-resolution due to the Time Stamp (TS) of the event, the residual of the Time-walk correction and the jitter due to noise are indicated in the table below.



Residual error of time-stamp and time-walk correction simulated for different energy deposition (4 TOT bits).

Peaking time (ns)	TOT bit	TOT clock (Mhz)	TS and Time walk error rms (ns)	Jitter for 0.3 MIP (ns)	Time resolution (ns)
375	4	11.3	33	35	**48**
	6	47.5	15		**38**
500	4	8.5	41	43	**59**
	6	35.7	17		**46**
750	4	5.66	56	60	**82**
	6	23.8	21		**64**
1000	4	4.25	72	78	**106**
	6	17.8	25		**82**

The calculation are performed for the 4 available peaking-times and assuming a S/N equals to 20. Moreover two cases are considered which differ for the TOT number of bits.

Better amplitude measurements enable to better estimate and correct for the time-walk. Thus, higher TOT accuracy (up to 6-bits) enables to increase the time resolution of the considered outer layers.

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