A Fast Readout Algorithm for Cluster Counting/Timing Drift Chambers on a FPGA Board

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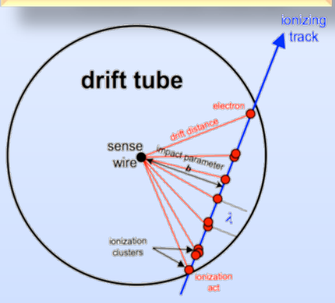
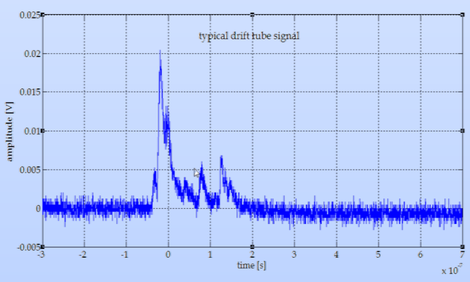
ABSTRACT

A fast readout algorithm for Cluster Counting and Timing purposes has been implemented and tested on a Virtex 6 core FPGA board. The algorithm analyzes and stores data coming from a Helium based drift tube instrumented by 1 GSPS fADC and represents the outcome of balancing between efficiency and high speed performance. The algorithm can be implemented in electronics boards serving multiple fADC channels and used as an on-line preprocessing stage for signals coming from drift chambers.

CLUTIM AIM



A charged particle passing through a drift chamber creates ion-electron pairs along its path. Depending on the released charge, for each ionization act, the particle releases one or more ion-electron couples referred to as Cluster.
The distance between two successive clusters follows an exponential distribution with average λ which represents the mean free path of the particle. λ value depends on the gas nature, pressure and temperature.



- 1.6 GHz bandwidth preamplifier
- 4 GHz bandwith, 8 bit, digital oscilloscope, 6 GSPS samp. freq.
- Gas mixture: 90% He - 10% iC_4H_{10}
- Tube diameter: 8 mm
- Sense wire: 20 µm
- Gas Gain: $4x10^5$

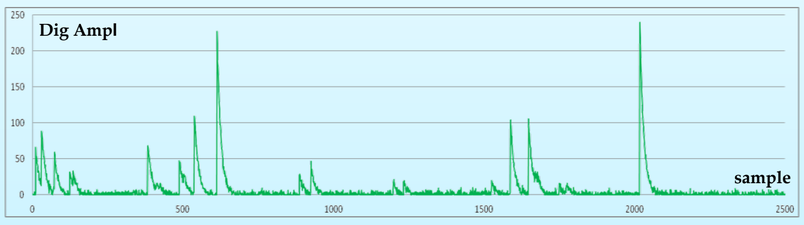
Typical time separation between consecutive ionization acts, in helium-based gas mixture, goes from a few ns to a few tens of ns.
Read-out interface has to be able to process such a high-speed signal.

- Acquire and sample the high speed signal.
- Detect all significant peaks on digitized signal.
- Store amplitude, timing and peak sequential number.

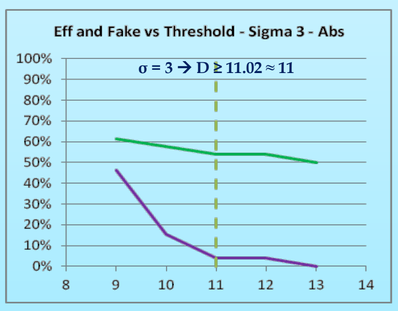
SIMULATIONS AND RESULTS

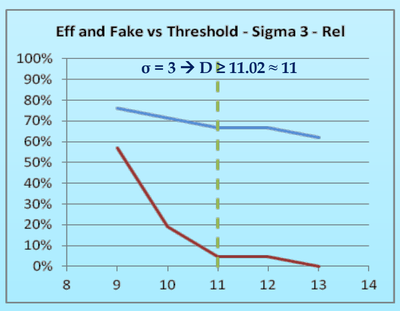
ALGORITHM PERFORMANCES: ➡ Efficiency Measurements

SIMULATED EVENTS: Montecarlo Sim (ideal signal + Gaussian white noise).



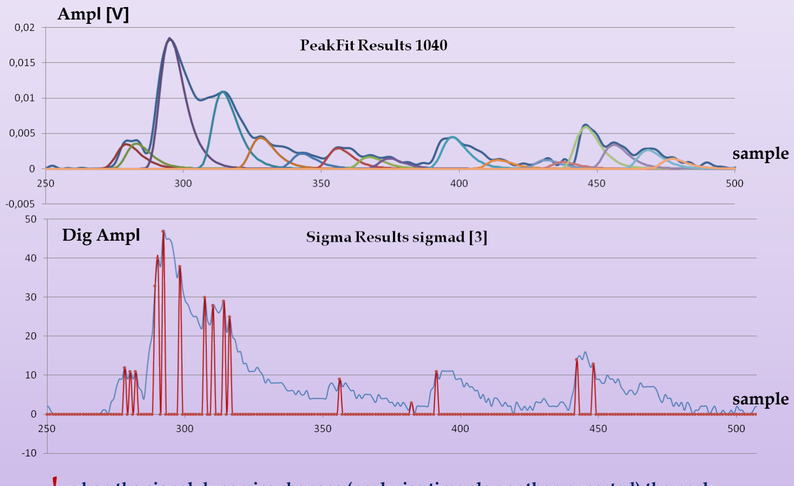
- The number of peaks found must be at the correct time.
- The peak amplitude value is corrupted by the noise.
- The peaks hidden by the noise are not taken into account for efficiency calculation.





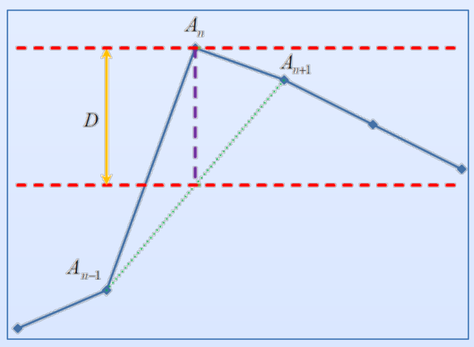
$$\varepsilon_{abs} = \frac{Algorithm\ Identified\ Peaks}{n^{\circ}\ of\ Ideal\ Peaks} \qquad \varepsilon_{rel} = \frac{Algorithm\ Identified\ Peaks}{n^{\circ}\ of\ Potentially\ Identifiable\ Peaks}$$

REALISTIC SIGNALS coming out from drift tube. Preliminary evaluation comparing the peaks found by the algorithm with those recognized by peak separation and analysis software (PeakFit).



! when the signal dynamics changes (peak rise time slower than expected) the peak finding condition maybe not satisfied. The possibility of taking into account more than 3 consecutive samples will be pursued as a further evolution of the algorithm.

HARDWARE SETUP AND SOFTWARE

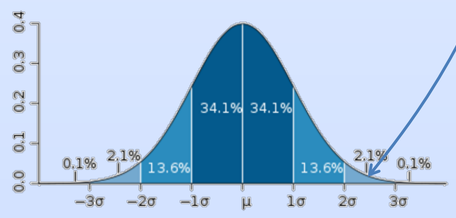


Algorithm approach

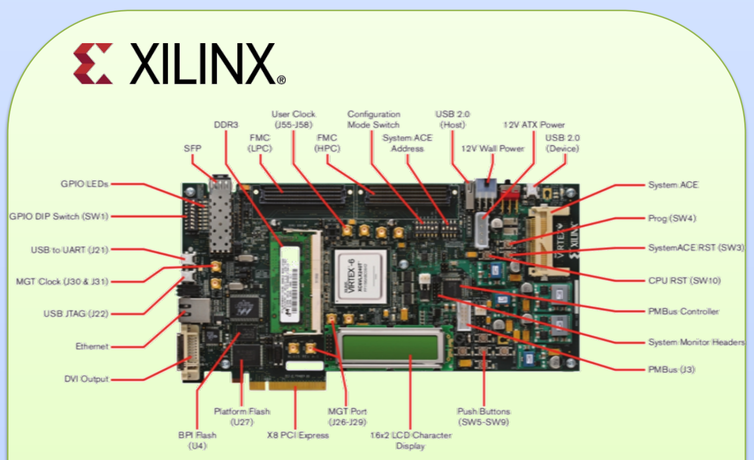
$$D = A_n - \left(\frac{A_{n-1} + A_{n+1}}{2}\right) \geq 3\sigma_d$$ Peak found condition

$$\sigma_d^2 = \sigma_{A_n}^2 + \frac{1}{4}\sigma_{A_{n-1}}^2 + \frac{1}{4}\sigma_{A_{n+1}}^2 = \frac{3}{2}\sigma^2$$ Set the threshold

Advantages:
- Simple
- Resource-saving
- No smoothing or baseline (implicitly set into the threshold)

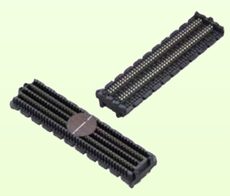


$3\sigma_d$ = cutting 99.7% of noise

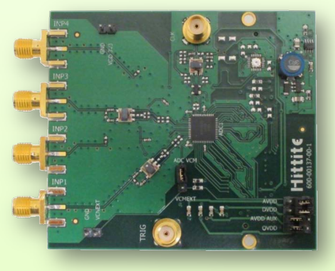


FPGA (Field Programmable Gate Array) Virtex6

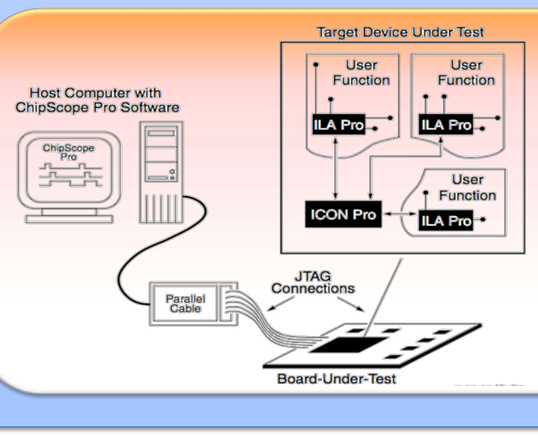
- ML 605 base board with FPGA: XC6VLX240T-1FFG1156
- Input/Output Clock Max Switching Freq.: 710 MHz
- Speed Grade: -1
- SMA connectors for external clock (differential)
- 66 MHz Socketed Oscillator (single-ended)
- FMC connectors: HPC (High Pin Count) and LPC (Low Pin Count)
- USB to Uart Bridge
- PCI Express x8 Edge Connector
- System ACE CF with 2GB Compact FLASH (CF) card
- 10/100/1000 tri-speed Ethernet (GMII, RGMII, SGMII, MII)



VITA 57 FMC (FPGA Meazzine Connector) : limits parasitic effects of pin coupling



HITTITE HMCAD1511 Analog to Digital Converter	
Resolution (bit)	8
Sample Rate (MBPS)	1000 (single channel) 500 (dual channel) 250 (quad channel)
Power Dissipation (mW)	710
SNR (dBFS)	49.8
Output	LVDS /RSDS
ENOB	> 7.5 up to 16X gain



ChipScope™ Pro tool inserts logic analyzer, system analyzer, and virtual I/O low-profile software cores directly into HDL design, allowing to view any internal signal or node.
Signals are captured in the system at the speed of operation and brought out through the programming interface.
Captured signals are then displayed and analyzed using the ChipScope Pro Analyzer tool.

CONCLUSIONS

A cluster timing algorithm has been developed on a Virtex 6 FPGA to implement peak detection of signals coming from a drift chamber. A VHDL code and a hardware setup, which includes a fast 1 GSPS fADC and a ML605 board, is proposed to acquire pre-amplified signals. The proposed algorithm shows good results both on simulated signals and on the realistic ones. Code optimizations to maximize peak counting efficiency are currently under development. Once the entire chain is fully tested and the VHDL code optimized, we plan the design of a VME board able to read at least four fADC channels.

REFERENCES

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