Trigger-less Readout System with Pulse Pile-up Recovery for the PANDA Electromagnetic Calorimeter

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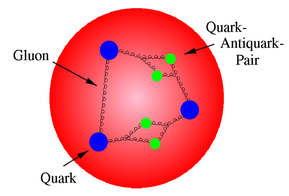
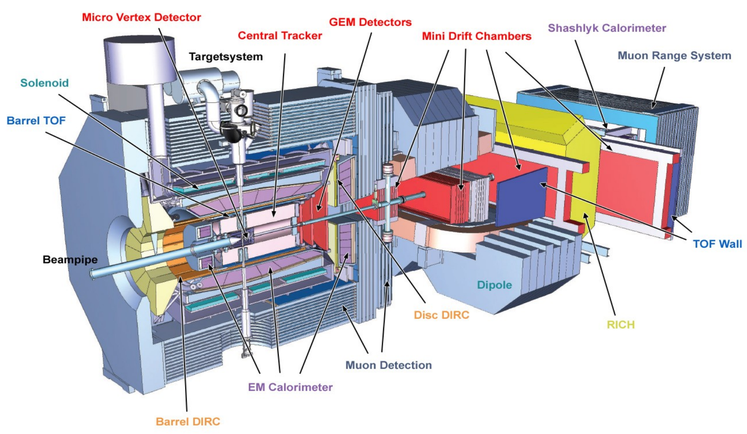
on behalf of the PANDA Collaboration

PANDA, the detector for antiProton ANnihilations at DArmstadt at the Facility for Antiproton and Ion Research (FAIR) in Germany:
will enable crucial tests of QCD, the theory of strong interaction, in the regime of strong coupling:
precision studies of charm-quark mesons, discovery of glue-balls and hybrid-mesons.



strong coupling in the proton



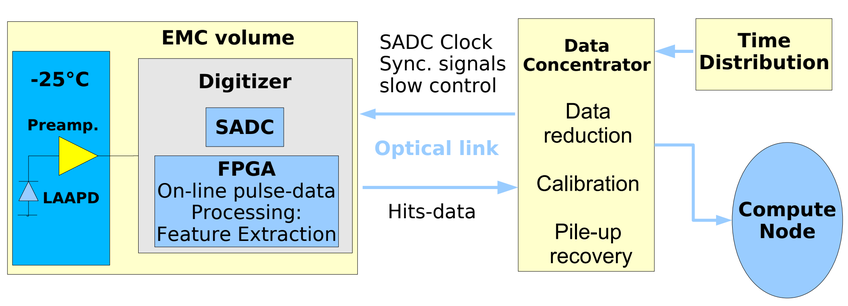
PANDA spectrometer in 2T solenoid magnet:
vertex detection, tracking, particle identification, calorimetry.

High-resolution ElectroMagnetic Calorimeter (EMC):
enables spectroscopy of charm-quark mesons (multi-photon final states).
Crystals: $PbWO_4$ (PWO-II) crystals, light yield of 500 photons/MeV at T=-25°C, which is about a factor 4 better than employed in CMS.
Light sensors: newly developed rectangular 7x14 mm^2 HAMAMATSU APDs

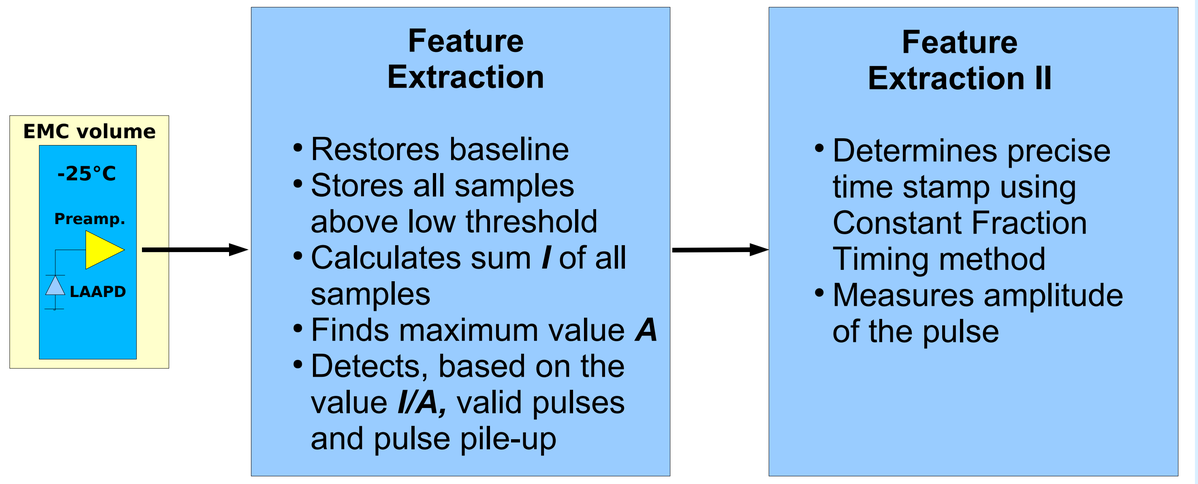
Trigger-less Data Acquisition

Goal: Flexible event-selection on basis of high-level data;
Operation at 20 MHz annihilation rate → 500 kHz hit rate
Implementation: Self-triggered intelligent front end, autonomous hit detection;
Precise time distribution: single clock source
Time-sorting, online processing in FPGA

Example: EMC readout



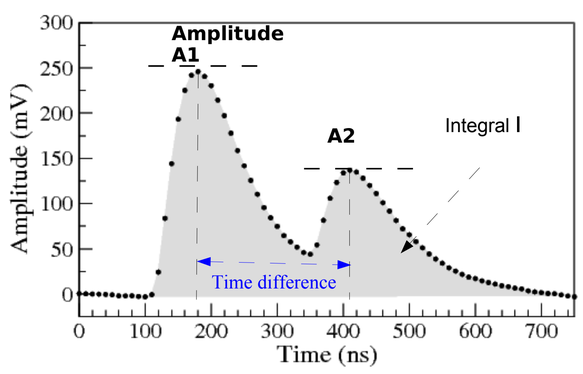
FPGA online processing: for shaped and unshaped pulses

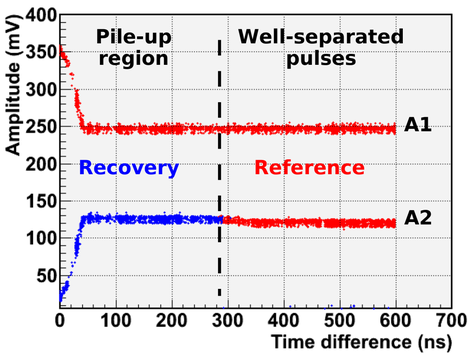


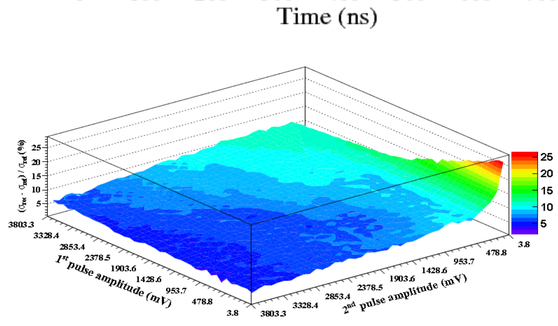
Details of the implementation, performance with EMC prototype:
E. Guliyev et al., Nucl. Instrum. Meth. Phys. Res. A 664 (2012) 22
M. Kavatsyuk et al., Nucl. Instrum. Meth. Phys. Res. A 648 (2011) 77

Online Pile-up Recovery

Pulse-shape stability verified in wide dynamic range: Integral I = k A
⇒ I = k (A1 + A2) ⇒ A2 = I / k - A1

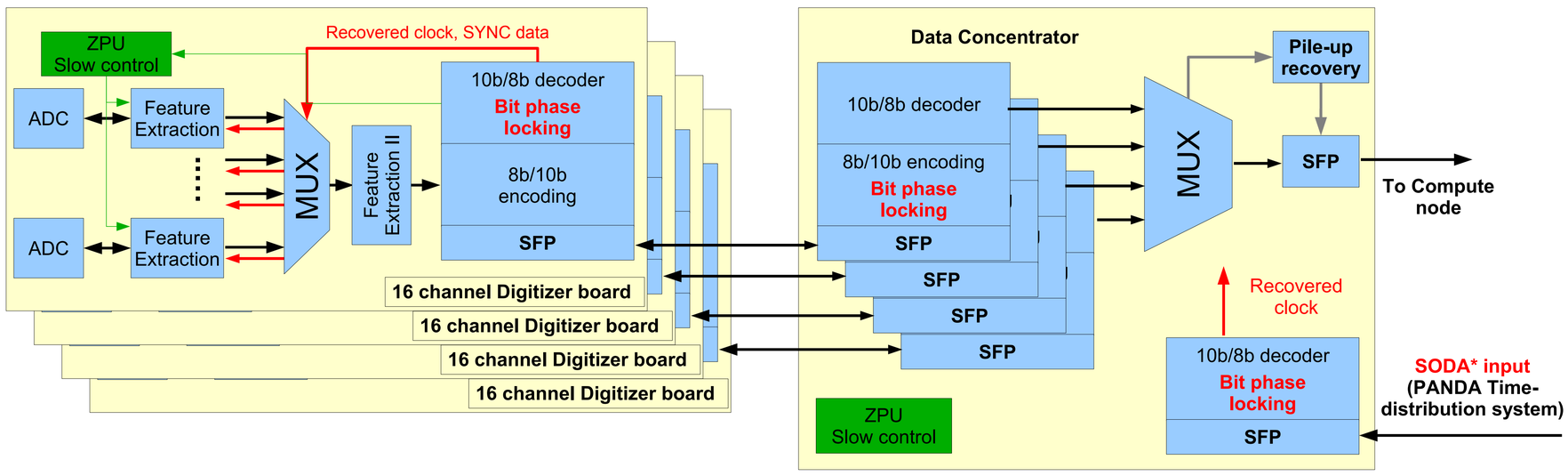






- Maximum hit-rate capability improves from 130 to 600 kHz
- Worst-case deterioration of cluster energy resolution : 20%

Prototype of Complete Readout Chain



Hardware components

16 channel SADC
(P. Marciniewski, Uppsala University):

- 14 bit ADC
- 125 MHz sampling rate
- Xilinx Virtex-5

Functional tests

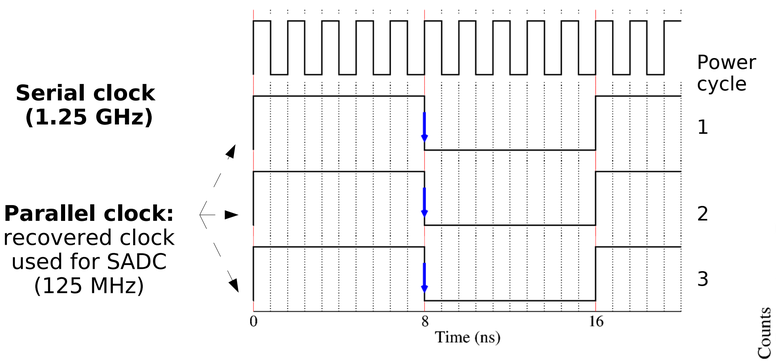
- single SADC unit with complete functionality
- synchronous optical link (stability of the recovered clock-phase)
- time-ordering multiplexer unit

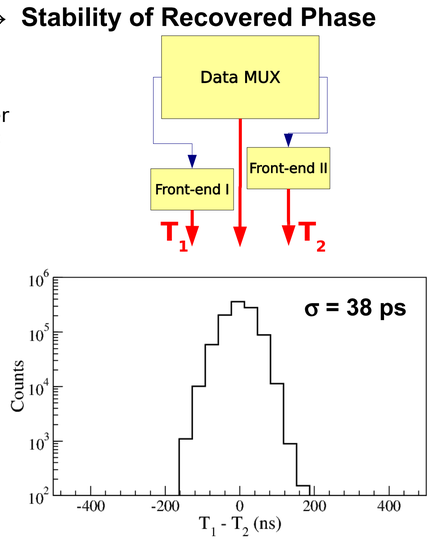
Measurements

- Time resolution < 1ns for signals > 80x noise level

Synchronous Optical Link Connection

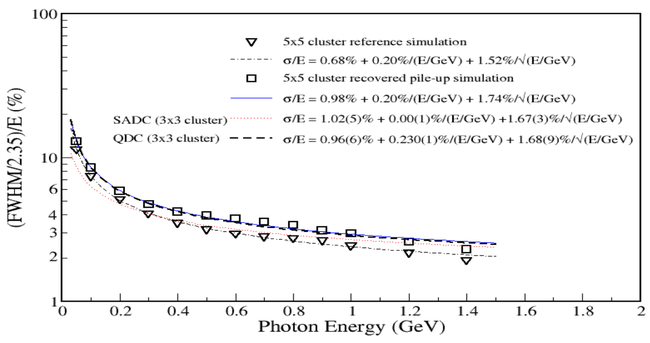
Standard implementation **does not guarantee stable phase** of the recovered clock
(phase changes at power/reset cycle) → **Bit Phase Locking** → **Stability of Recovered Phase**

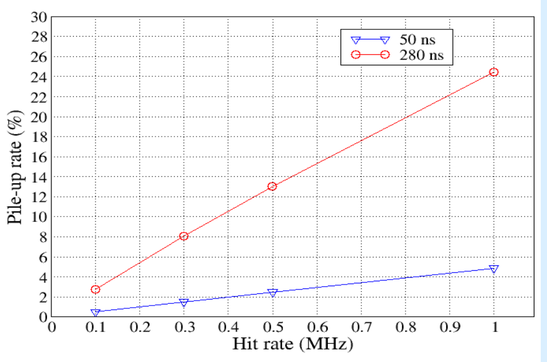




Jitter induced by **TDC >** 19 ps
→ **Jitter of single channel < 23 ps!**

Results and Conclusions





- Low-noise SADC readout, good resolution, efficient pileup recovery
  - Complete trigger-less readout chain developed and tested:
  - VHDL code **released as an open-source project**
  - **Efficient on-line pile-up recovery method developed**