The MU-RAY experiment. An application of SiPM technology to the understanding of volcanic phenomena.

12th Pisa Meeting on Advanced Detectors
Frontier Detectors for Frontier Physics
La Biodola, Isola d'Elba - 2012

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Introduction – MuRay Collaboration & Goals

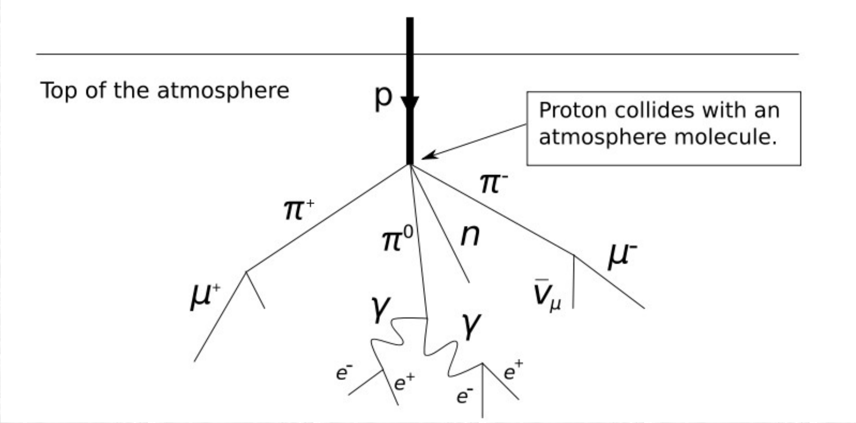
- INFN e Università Federico II, Napoli
- INFN e Università di Firenze
- INGV-Osservatorio Vesuviano, Napoli
- CNR-IFAC, Firenze
- LAL, Orsay, France
- Fermilab, USA
- Earthquake Research Institute, University of Tokyo
- Department of Physics, University of Tokyo
- Vulcano Laboratory, Hokkaido University

- Muon radiography is an imaging technique to measure density variations within a volcanic cone down to a depth of hundreds of metres.
- In optimal conditions with sufficient statistics one can expect to obtain resolutions of the order of ten metres. These compare very favorably with what can be obtained by traditional gravimetric techniques.
- If these goals can be achieved, this type of measurement can provide significant complementary information on eventual anomalies in the rock density (i.e. like those given by the presence of lava conduits).

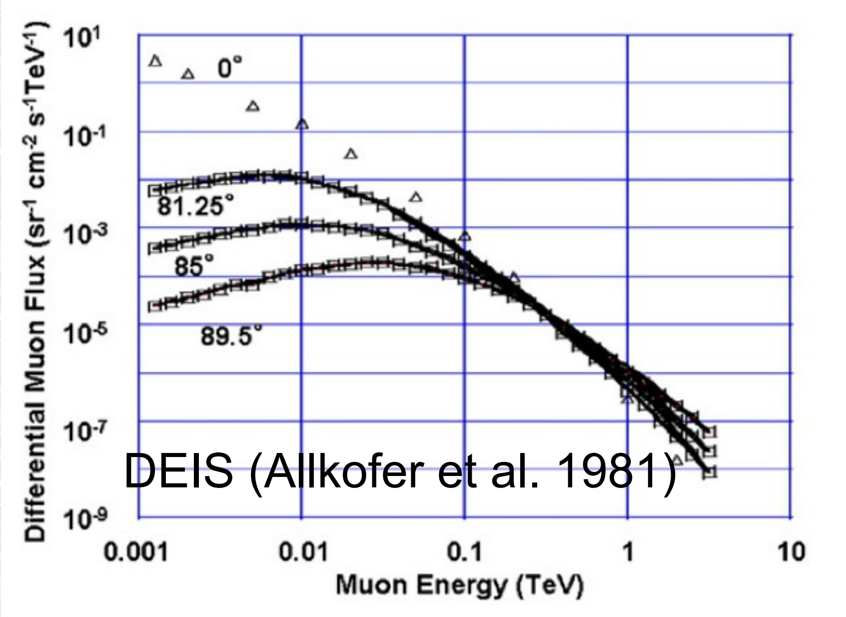
Basics

- Atmospheric Muons:

Particle showers are created from the interaction of primary cosmic rays with the nuclei of the earth's atmosphere.



- Practically only muons arrive at ground level (together with a small fraction of electrons which are not relevant to this application)
- 70 $s^{-1}m^{-2}sr^{-1}$ (vertical, 1 cm^{-2} min^{-1})



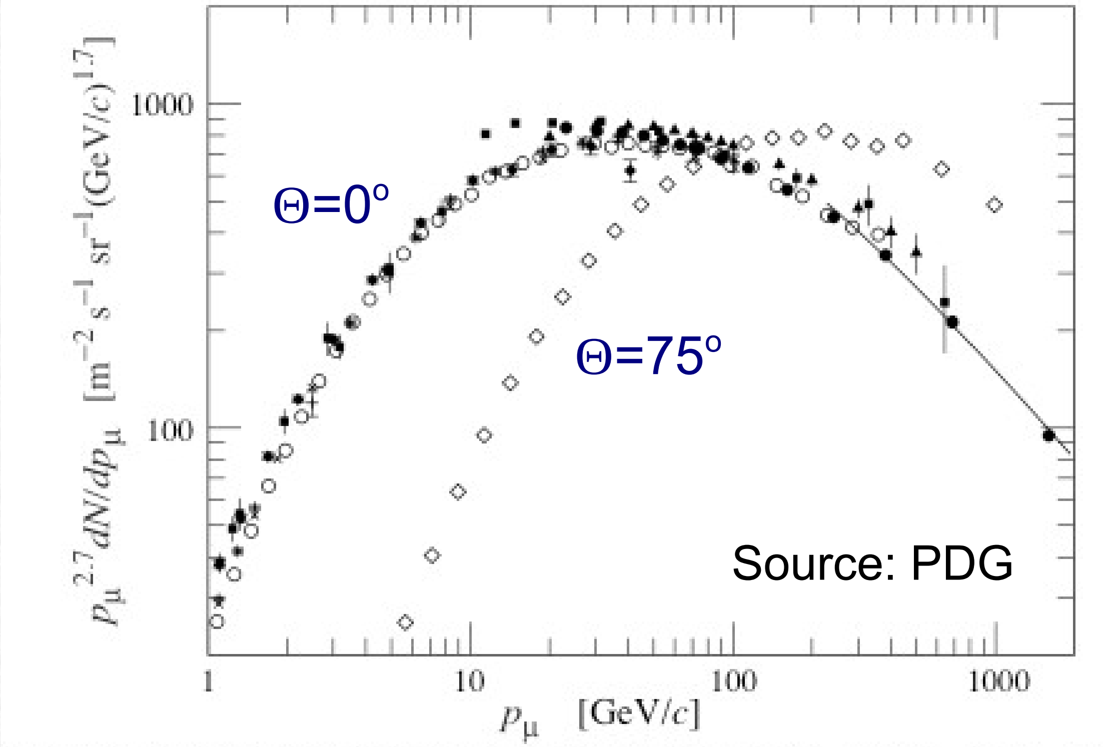
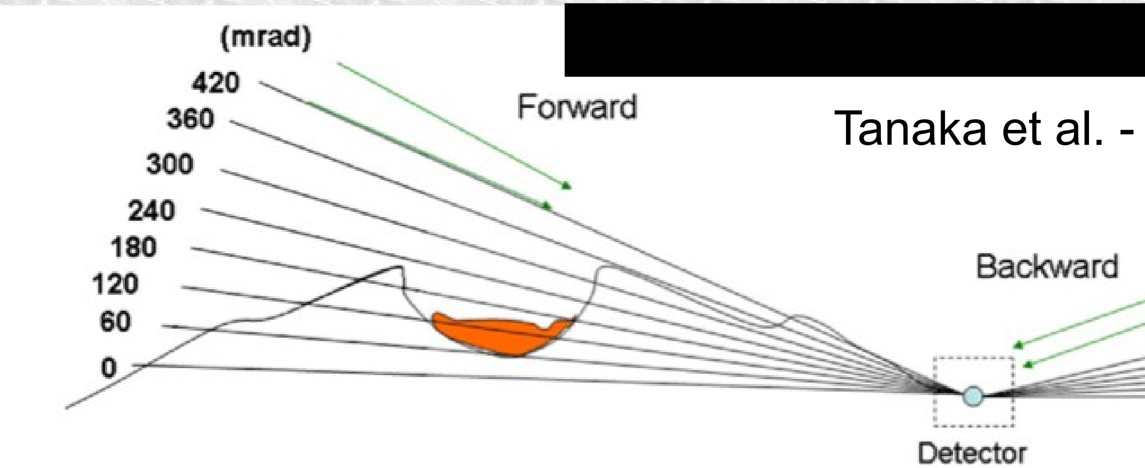


Figure 24.4: Spectrum of muons at $\theta = 0°$ (♦ [38], ■ [43], ▾ [44], ▲ [45], ×, + [40], ○ [41], and • [42] and $\theta = 75°$ ◊ [46]) . The line plots the result from Eq. (24.4) for vertical showers.

Basics

[redacted]

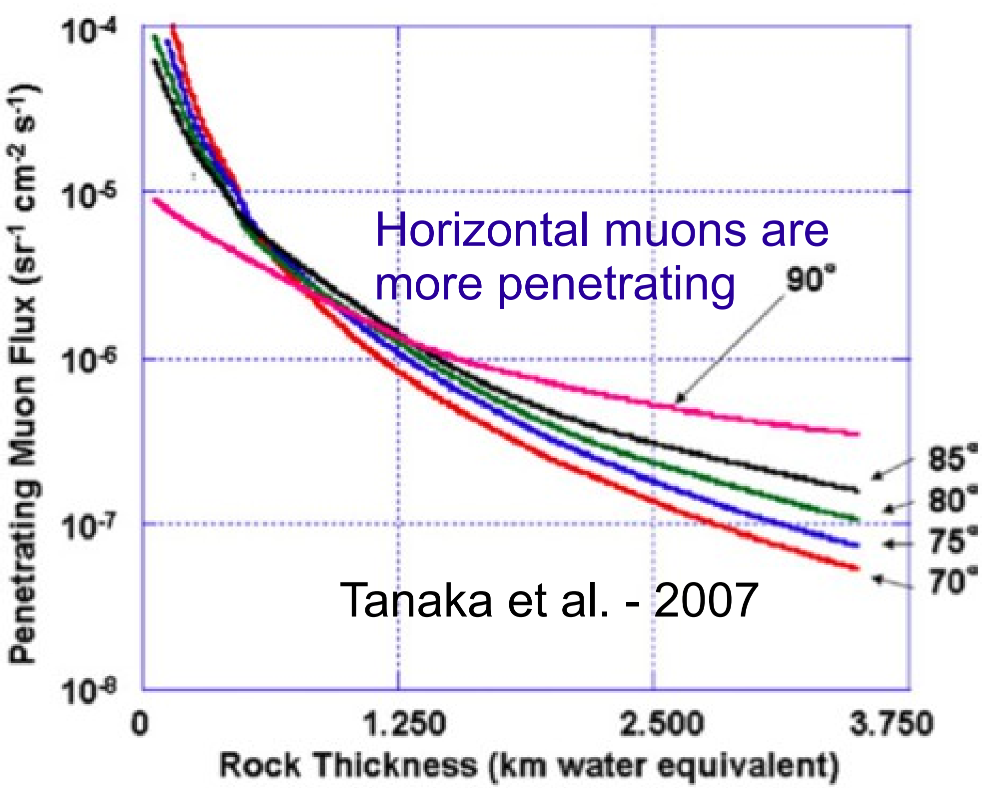


Muon range *R* and energy loss parameters calculated for standard rock

E_μ (GeV)	*R* (km.w.e)	*a* (MeV g^{-1} cm^2)	*b* (MeV g^{-1} cm^2)
10	0.05	2.15	1.91
100	0.41	2.40	3.12
1000	2.42	2.58	4.01
10,000	6.30	2.76	4.40

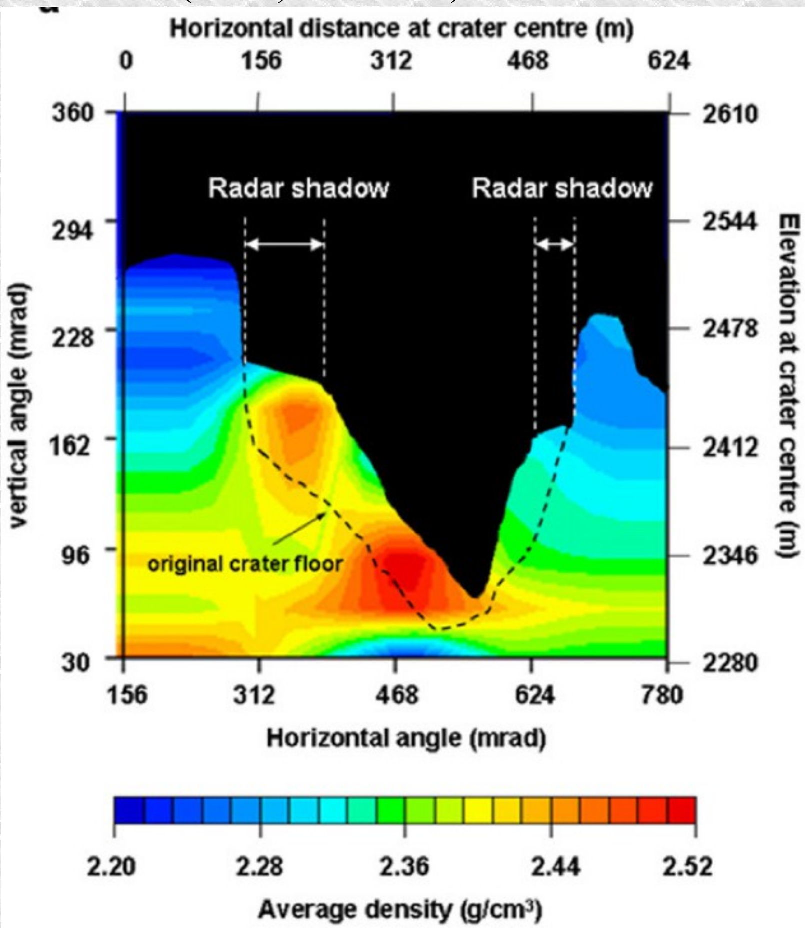
Range is given in km-water-equivalent.

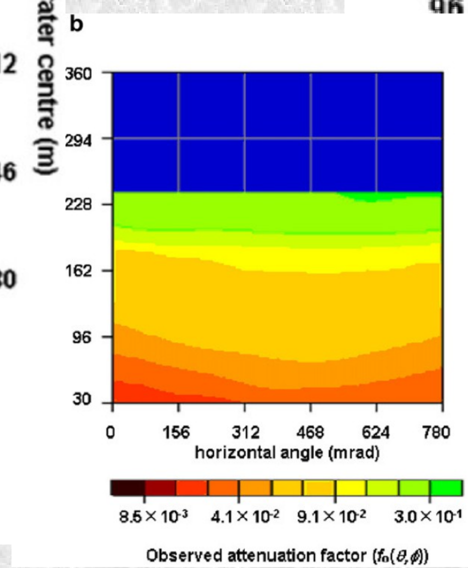
- Horizontal muons, very low rates need relatively large detectors.
- Rock = Threshold on the muon energy
- Energy loss: **dE/dX = a + bE**
- Need to know the morphology of the terrain under investigation.

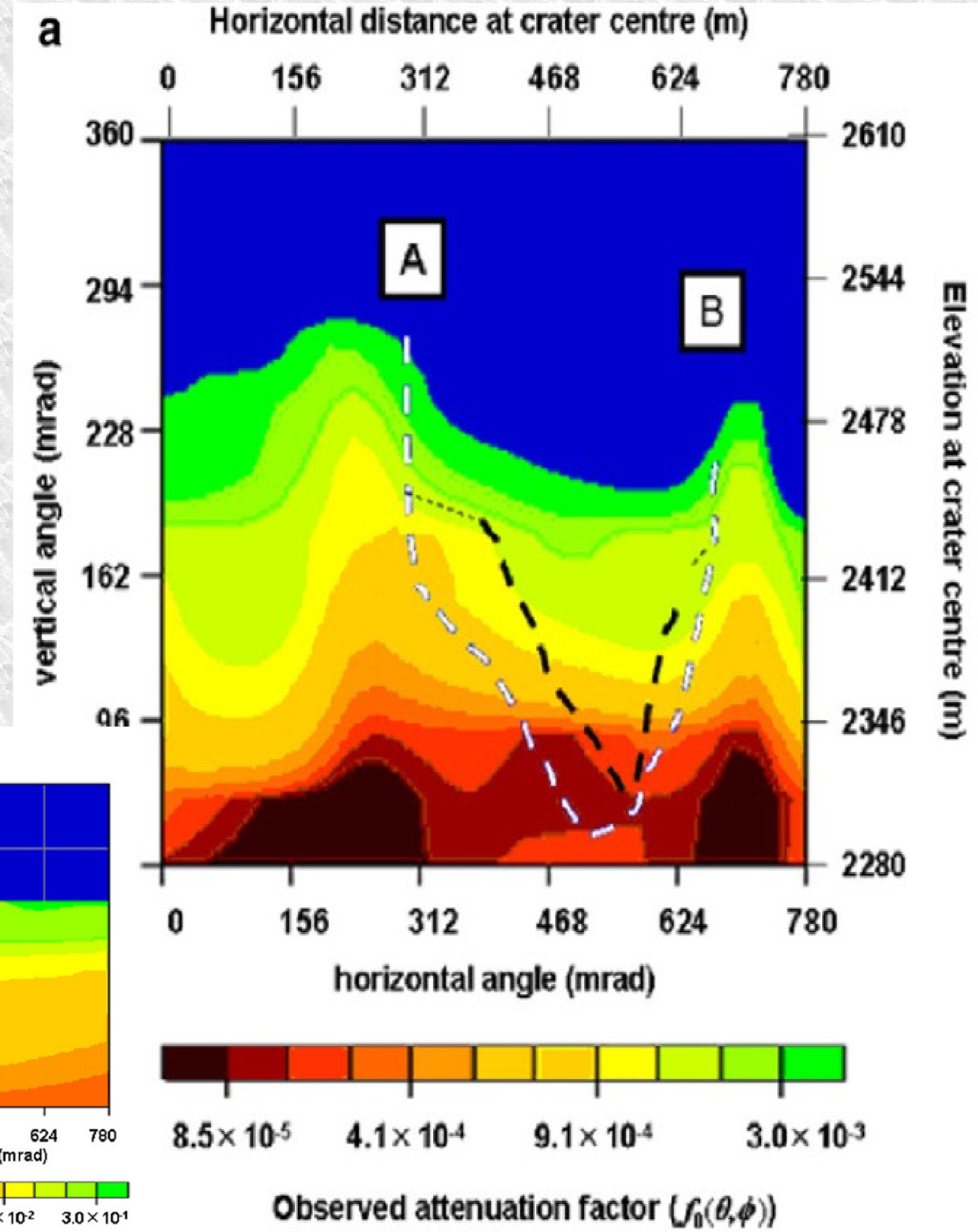


What has been achieved

- Very young field of research.
- Pioneering results by H. Tanaka et al. - Tokyo University.
- Example: Mt. Asama
(Earth and Planetary Science Letters 263 (2007) 104–113)





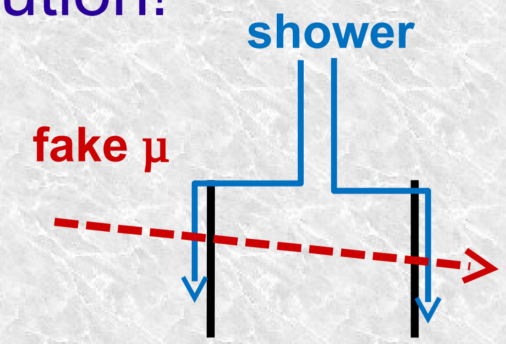


Muon telescope requirements

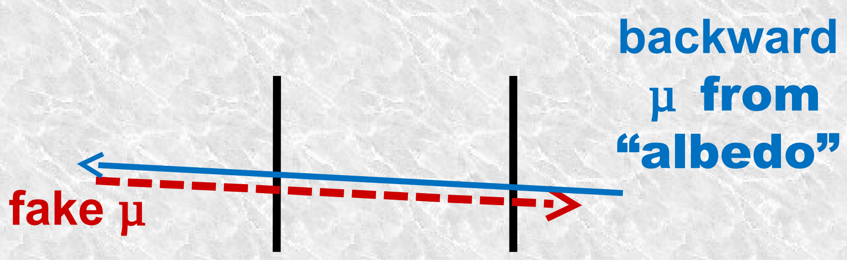
- Tracking capability: direction of muons with relatively high spatial/angular resolution (few millirads)
- Uniformity of response
- Redundant background suppression capability
- Low cost/channel: larger telescope area and/or higher resolution
- Resistant and modular structure: usage in volcanic area
- Low energy consumption : usage in volcanic area
- Electronics and sensors must perform from below zero to 50-60 ^{o}C

Background from other sources

- Showers of charged particles created in the atmosphere can mimic a straight track -> use at least 3 planes, increase resolution!



- At low angle re-scattered «albedo» muons coming from the opposite direction (where there is no volcano….) can mimic the muon-> measure Time Of Flight (TOF)



MuRay Prototype Design

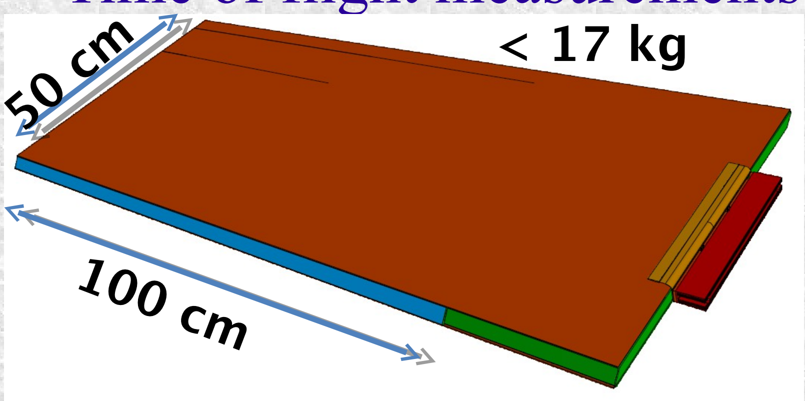
Several solutions originally proposed by Mu-Ray are nowadays «standard» design practice for proposed detectors in the muon tomography field:

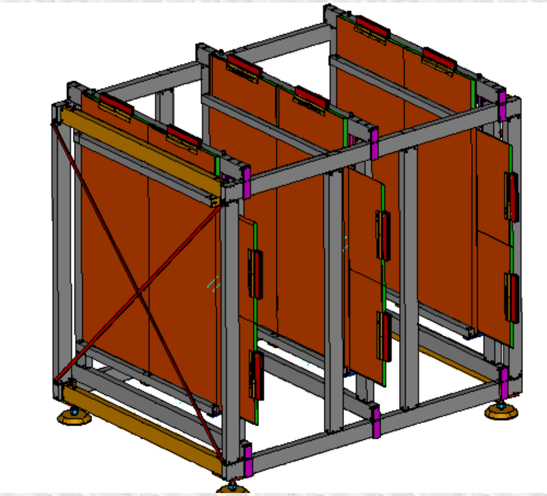
- At least three planes, each with both X and Y measurement
- Azimuthal rotation for flux calibration

Time of flight is still unique to Mu-Ray, due to its unique time resolution which allows to distinguish the direction of the traveling muons.

Space/time resolution, background rejection, large active area, low cost.

- **Three X-Y stations of 1x1 m^2 sensitive area**
- **12 modules easy to transport and to assemble**
- Time of flight measurements

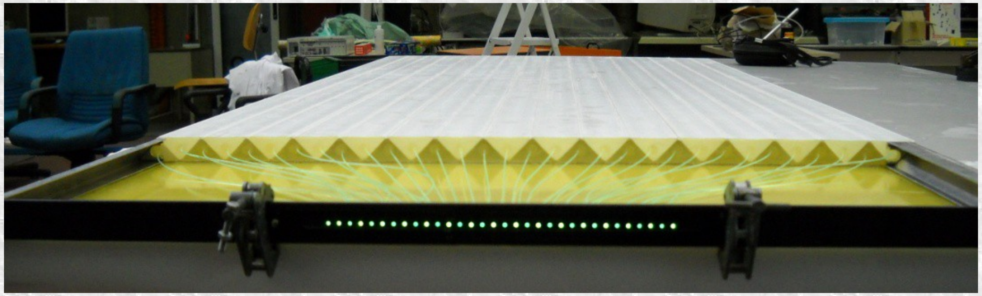


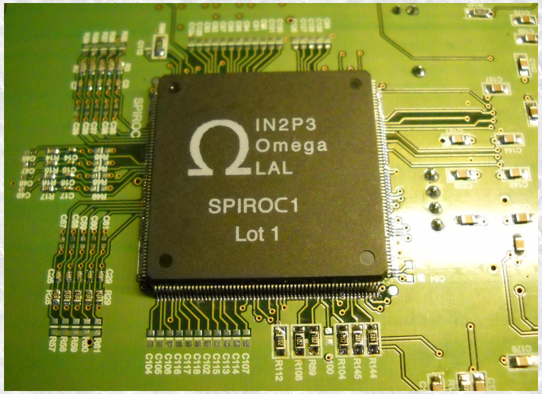


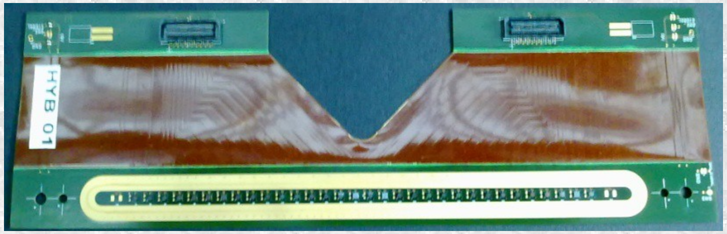
< 280 kg

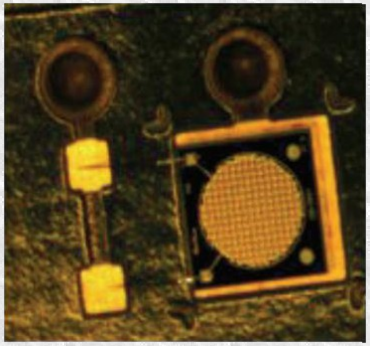
MuRay Detector Choices

- Triangular plastic scintillator bars: robust, fast, chip, spatial resolution.
- Fast WLS fibres photon collection
- SiPM light read-out: low power, robust , fast, chip
- One single 32-SiPMs connector/hybrid per module
- SPIROC FE electronics: SiPM dedicated, low power consumption
- Dedicated low power consumption FE and DAQ electronics
- Peltier cooling



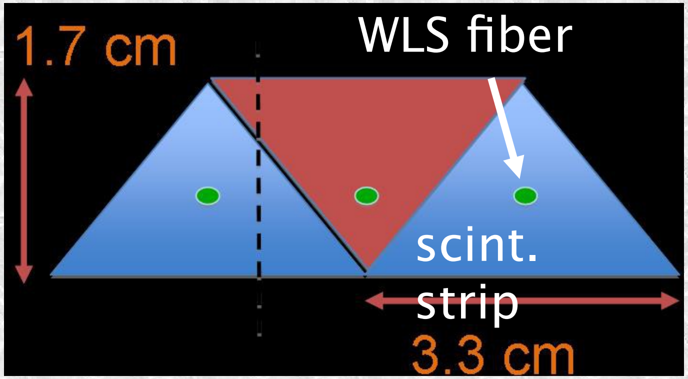


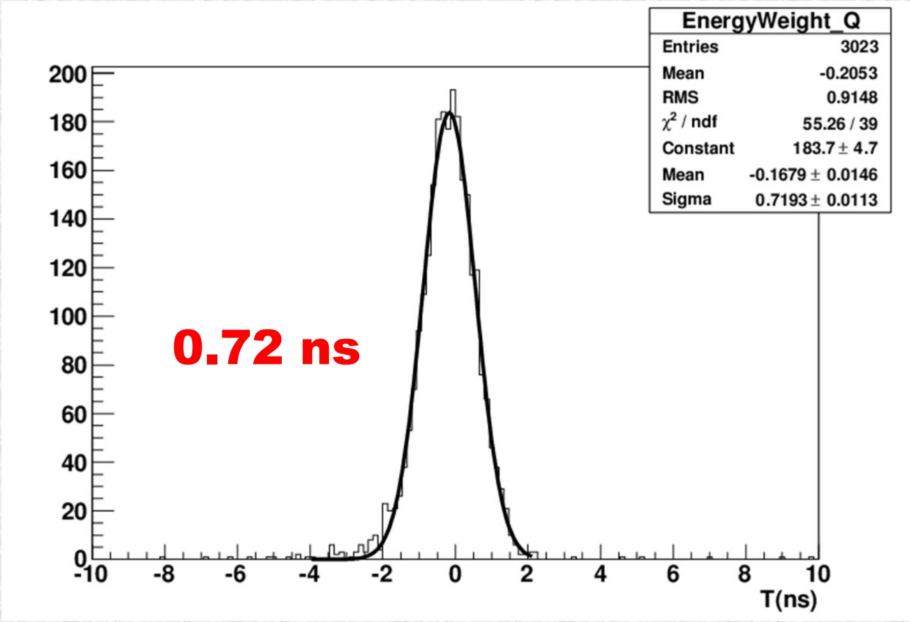




Fast scintillators and WLS fibers: excellent time resolution

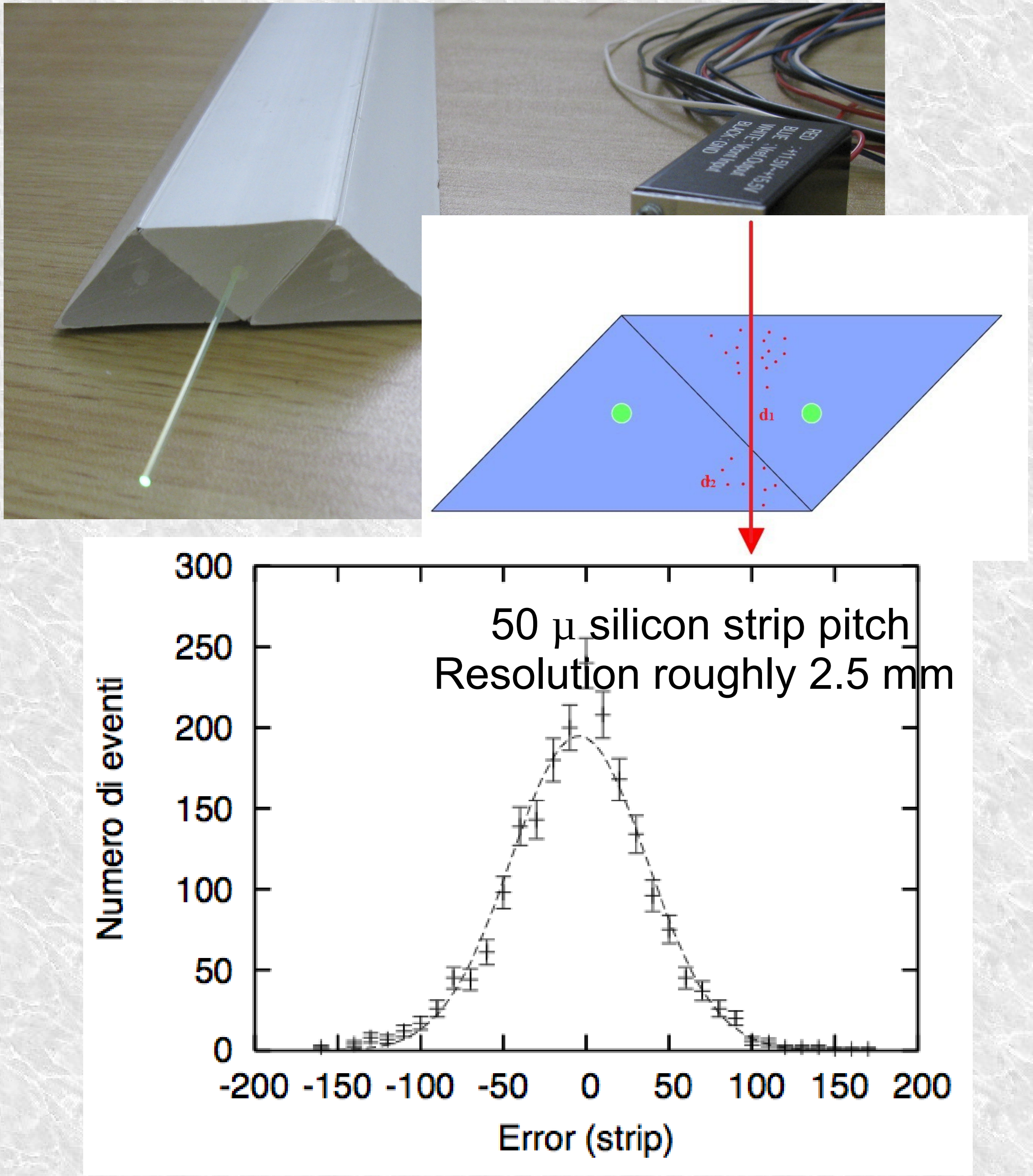
- Scintillator: fast emission time (≈3 ns) polystyrene produced NICADD_FNAL by extrusion with 0.25 mm TiO_2 coating and ~1.8 mm hole
- WLS fiber: BCF92 multi-clad: fast emission time (≈ 2.7 ns) mirrored at one side.
- Sub-nanosecond resolution achievable
- NA62 experiment at CERN (Hamamatsu MPPC S10362 13-50C)





Obtainable spatial resolution

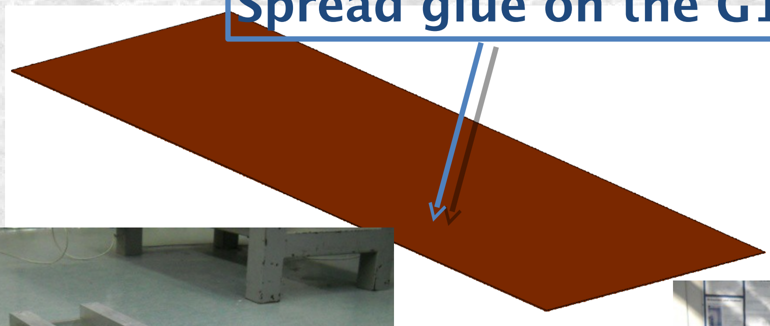
- Tested the concept with an external trigger a silicon telescope and high quality photo multipliers
- Coupling between WLS and scintillator was not optimal
- Expected “Digital Resolution” of the order of 6mm.



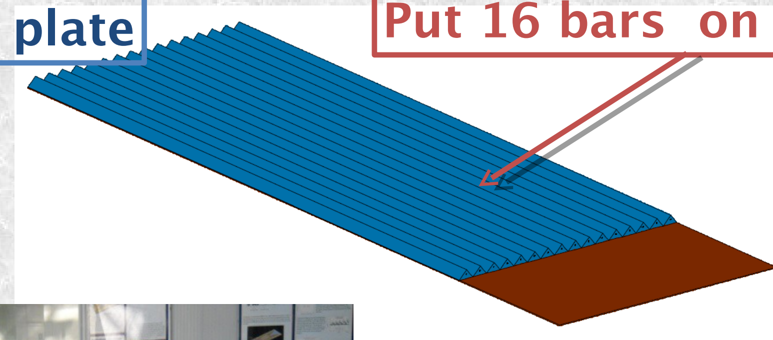
Scintillator Module Construction (1)

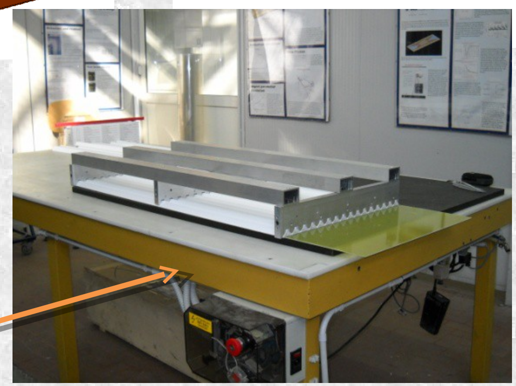
- 12 modules have been constructed in spring 2011

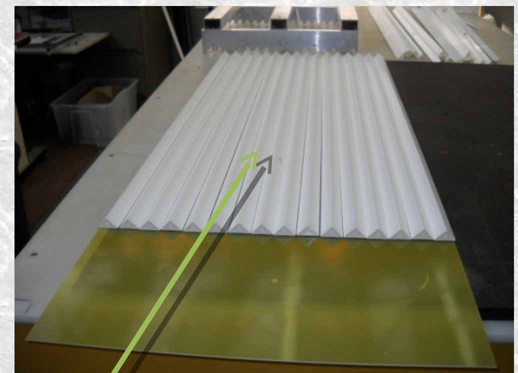
Spread glue on the G11 plate



Put 16 bars on the plate

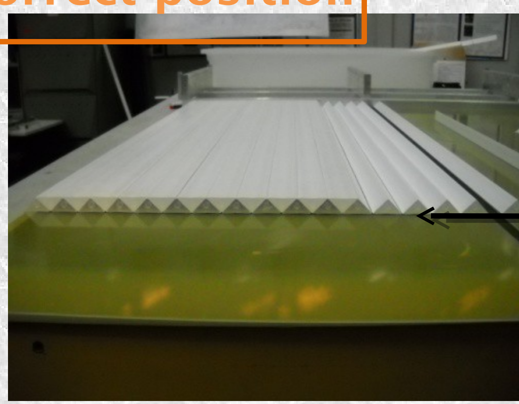






Jig holding the scintillator bars in the correct position

After the glue sets the jig is removed

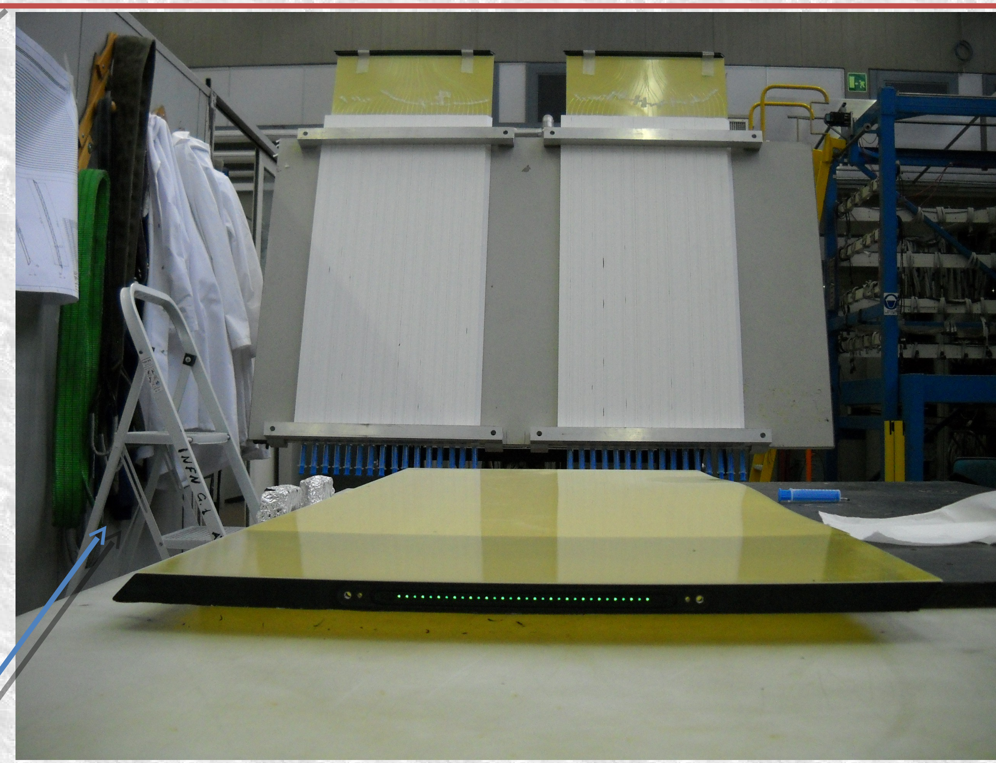


Now it's possible to glue the second scintillators layer

Scintillator Module Construction (2)

- When the scintillator bars have set, the fibres are glued inside the through holes

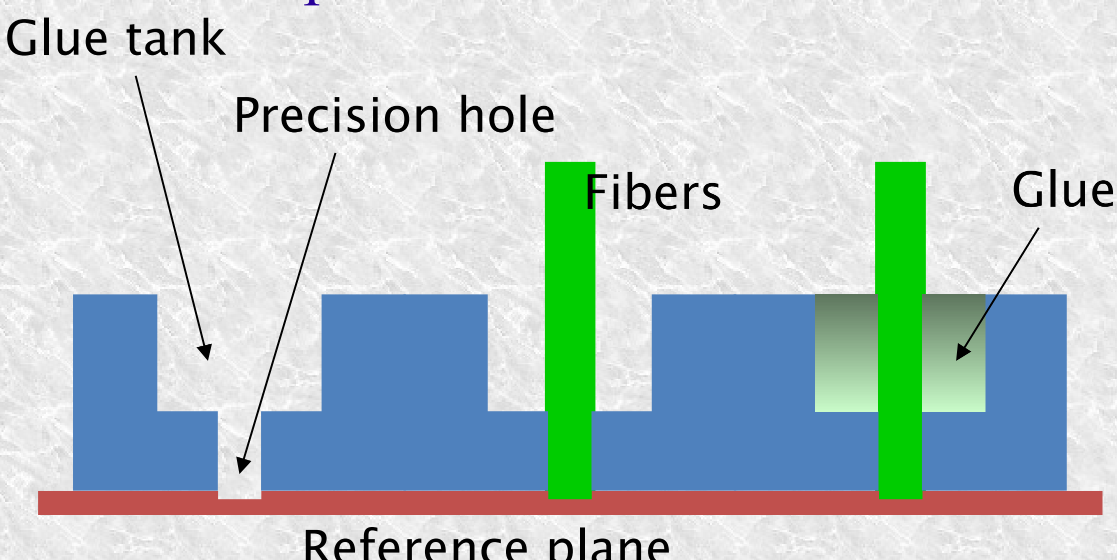
Fibres, already glued in the fibre-connector, are inserted in the scintillators holes

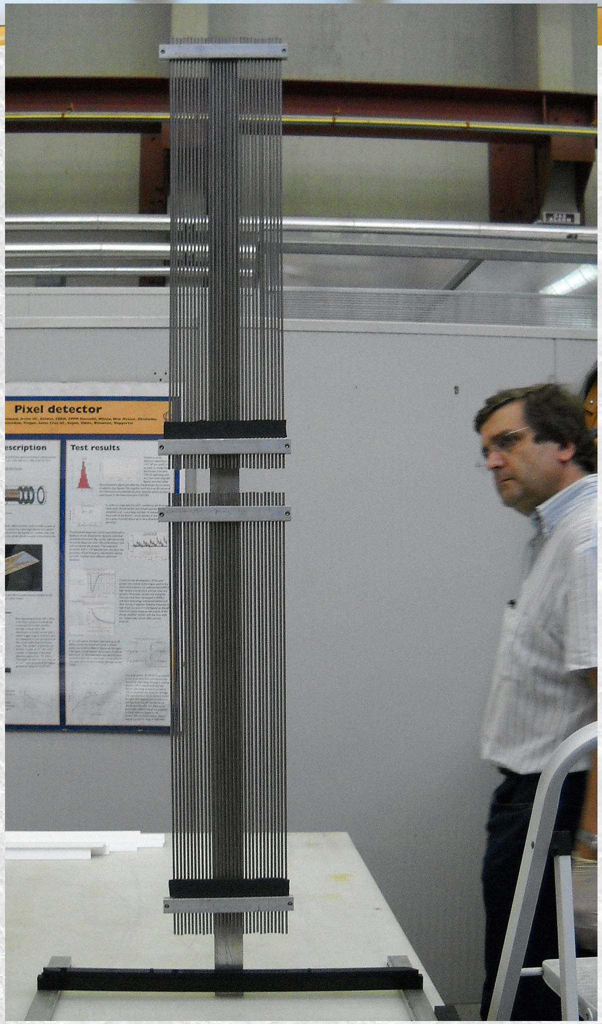


The optical glue is injected with a syringe from the bottom

Fibre connector

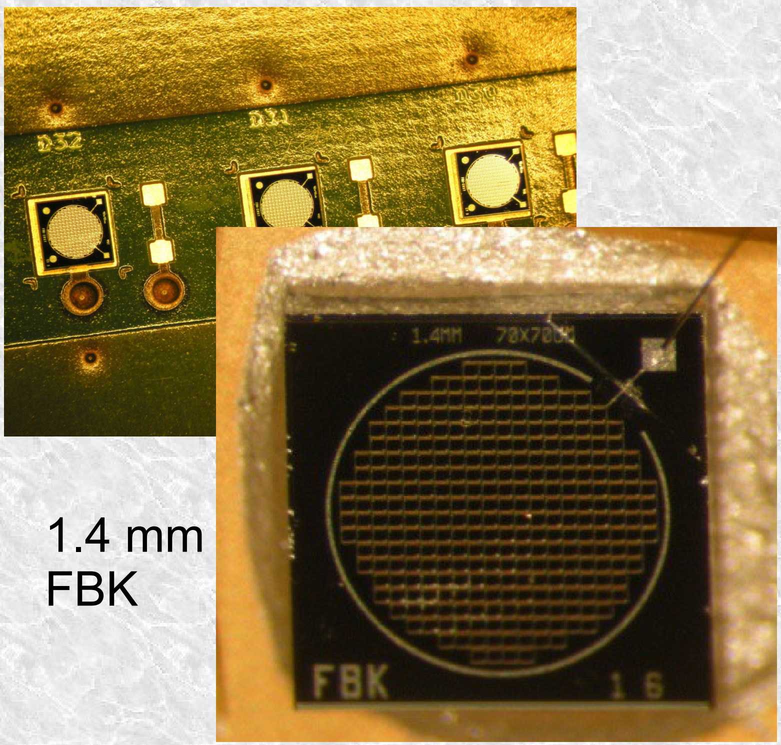
- Fibres are precut to required length
- One of the ends has a reflective coating
- Fibres are bundled in 32s and glued at the other end to a precision moulded connector cap
- This connector will then be plugged to the hybrid carrying the SiPMs
- Alignment is better than 50µm as well as depth



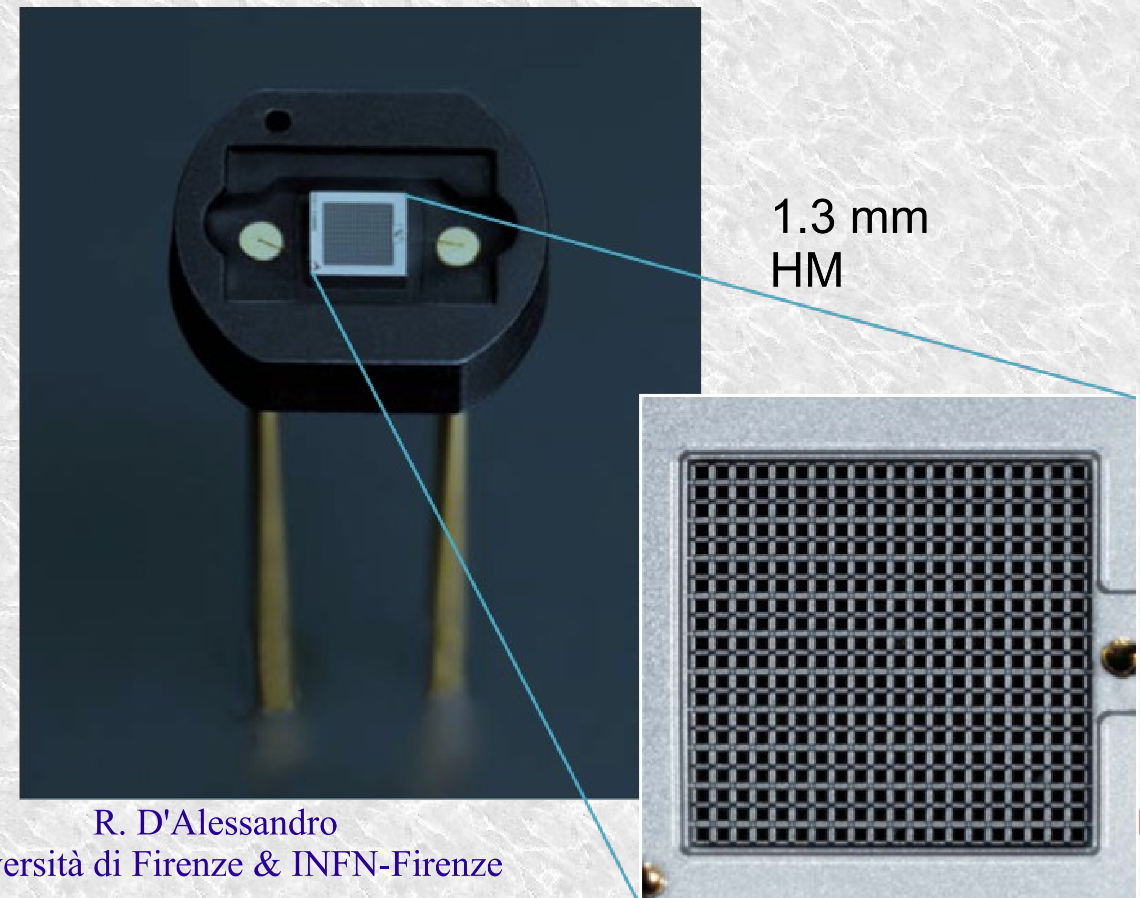


SiPM

- New concept in light detection
- Array of APD cells working in self-quenching Geiger mode
- High level of miniaturization and integration
- Light detection efficiency higher, and gain comparable to traditional PMTs
- “Digital” linear response (each APD cell works in on/off mode)



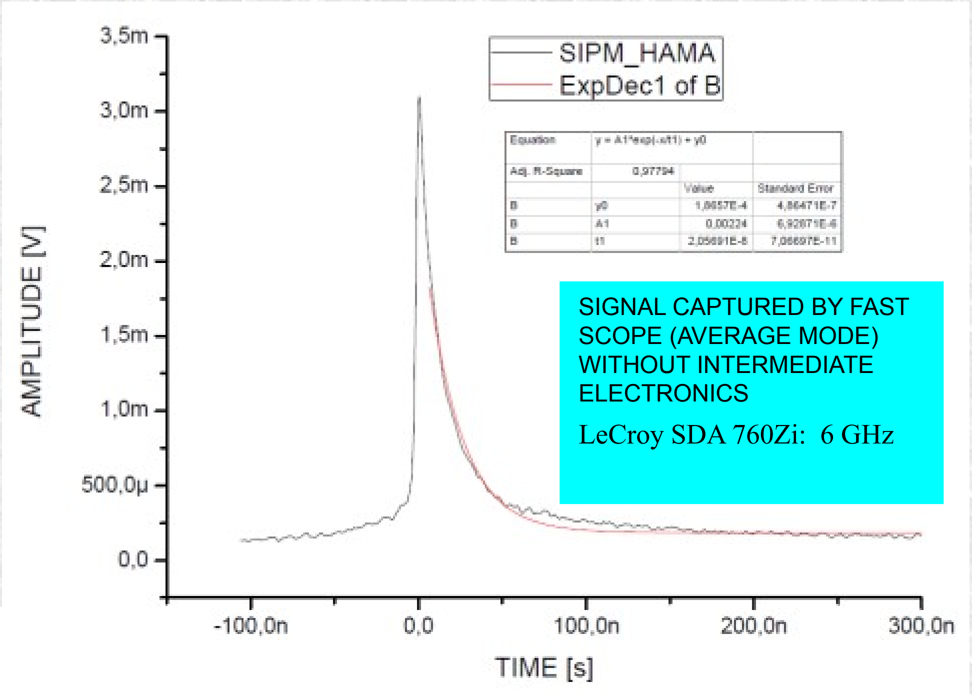
1.4 mm
FBK

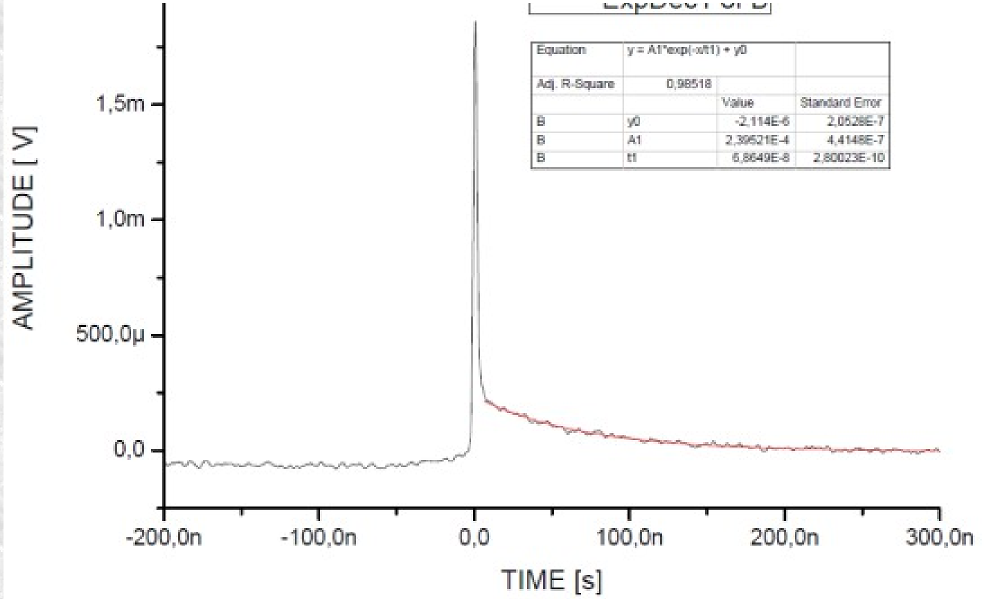


1.3 mm
HM

SiPM (continued)

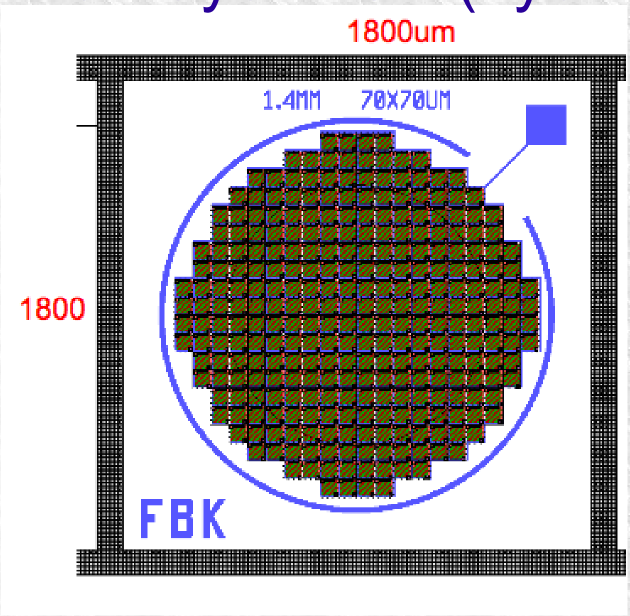
- Photo-detection efficiency (10%-60%)
- Linearity (if n photons << n cells)
- High gain (10^5-10^6)
- Single photon detection sensitivity
- No excess noise factor (at first order..)
- Fast (≈ 1 ns rise time)
- Good time resolution (< 100 ps)
- Low bias voltages (< 100 V) very low power consumption (10 µW)
- Insensitive to B field
- Extremely compact and robust
- **Breakdown voltage and dark rate depend on temperature**





SiPM from IRST for MuRay

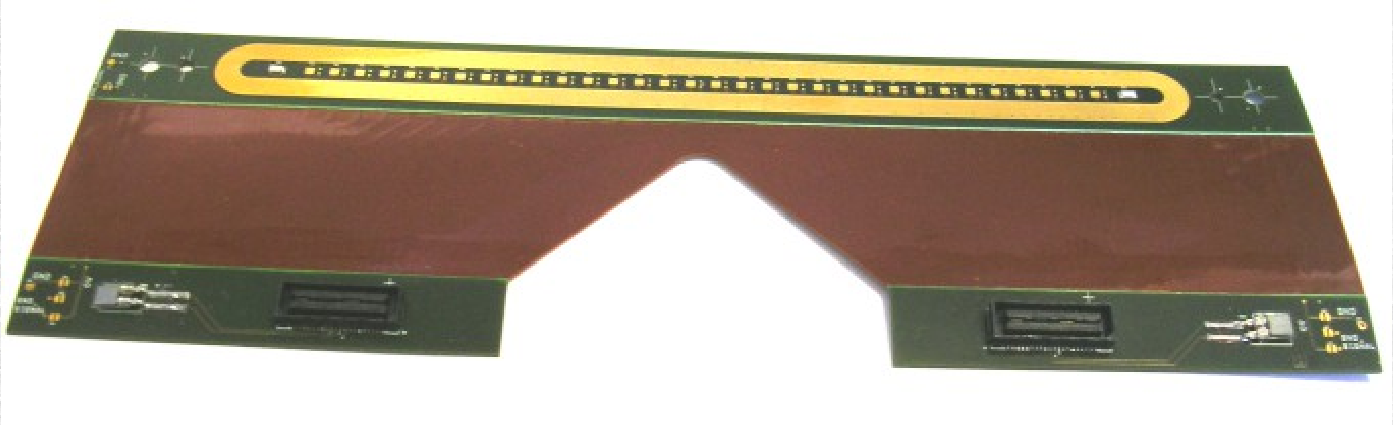
- SiPM active area: circular 1.4mm diam.
- Pixel size: 70 μm x 70 μm
- Number of pixels: 292
- Die, with only a thin transparent protective epoxy layer
- The SiPM are glued and bonded on a multilayer PCB (hybrid)



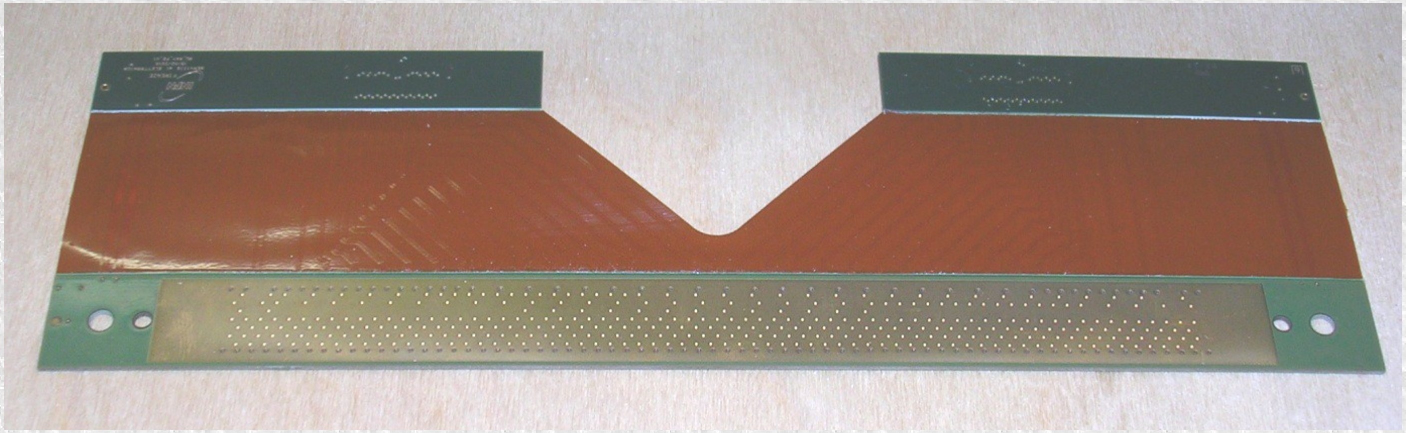
Wafer	Epoxy thickness	1.4mm diameter	1.2mm diameter
W1	35	235	40
W2	35	227	37
sub-total		**462**	**77**
W5	65	220	36
W6	65	226	38
W8	65	214	34
W11	65	227	40
W12	65	226	40
W13	65	229	38
W15	65	218	38
W3,4,7,10,14	65	1138	0
sub-total		**2698**	**264**
	Total	**3160**	**341**
		Total SiPM	**3501**

New hybrid support for SiPMs

- Improved flexibility for front-end acquisition board.

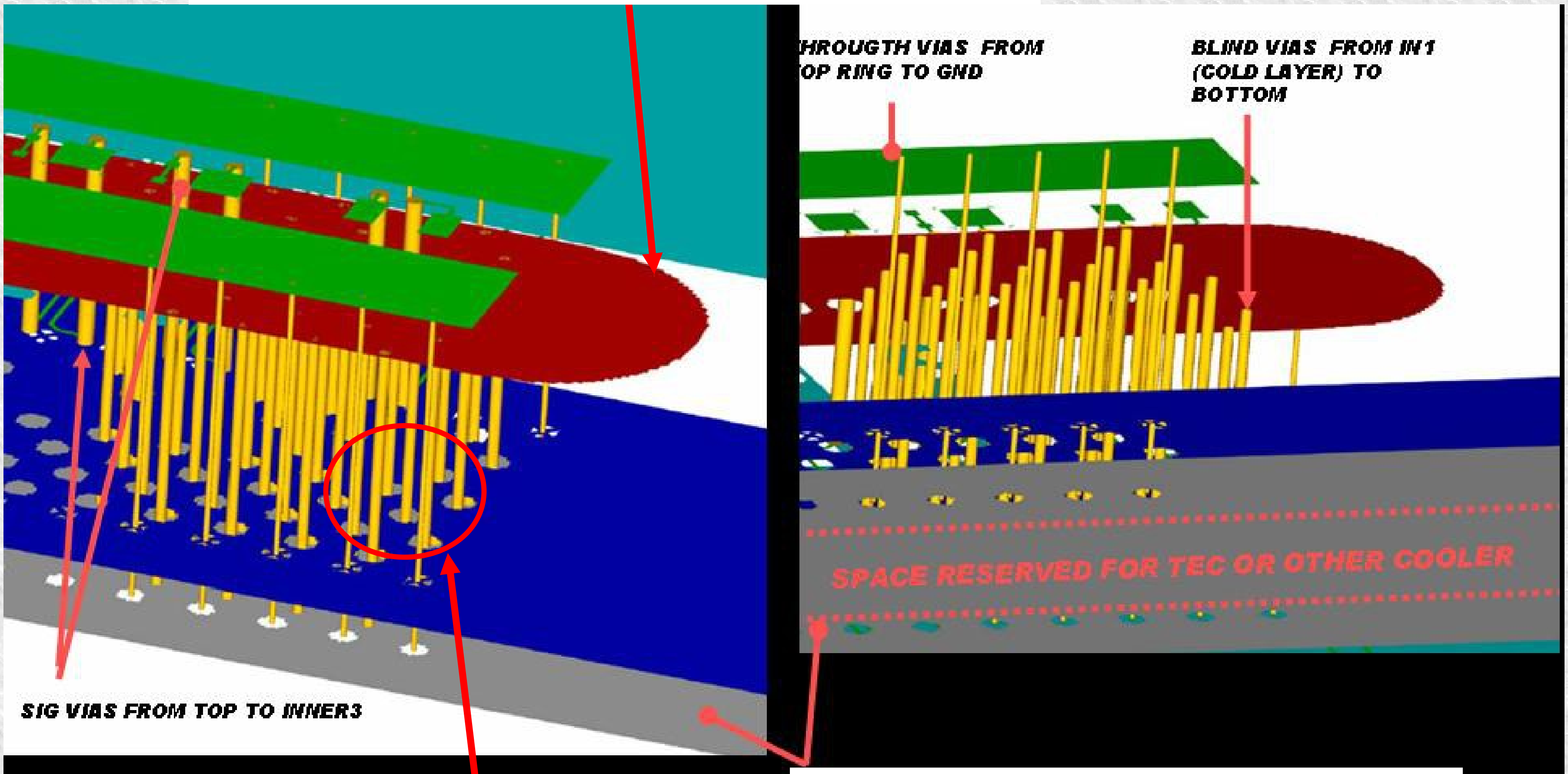


- Thermal connection between the TE cooler (Peltier) and the inner cold metal has been improved with many more vias.



Thermal configuration - SiPM side

INNER copper PLATE 75um from SiPM Bottom



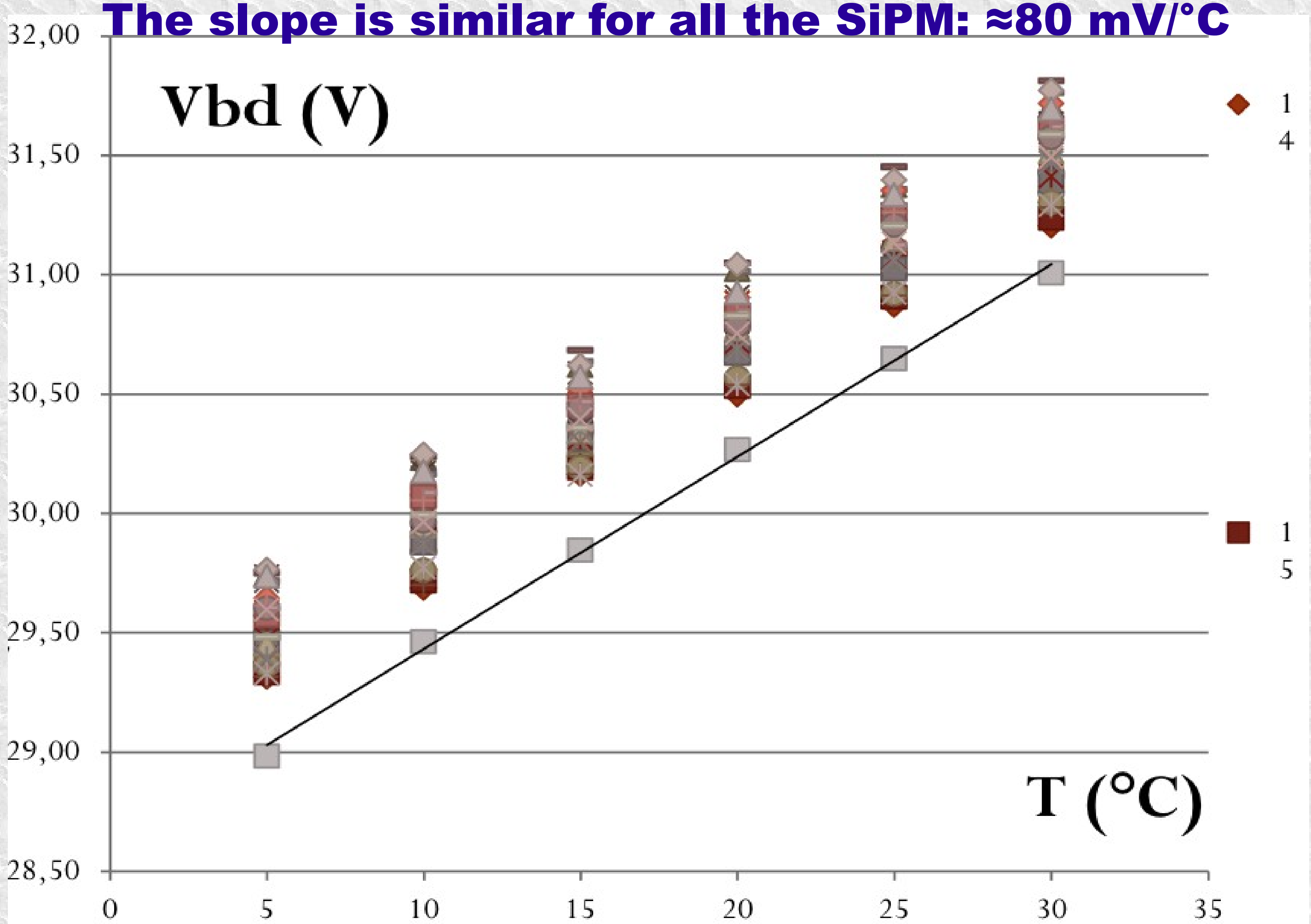
Copper vias to improve thermal conducibility between bottom cold plate and inner plate below SiPM

BOTTOM PLANE (COLD LAYER)

Cooling and Working Points

- SiPM breakdown voltage depends on temperature.
- Two possible approaches:
- Keep SiPM temperature fixed (e.g. using Peltier cells)
- Routinely compensate the temperature drift by changing Vbias to keep (Vb - Vbd) fixed

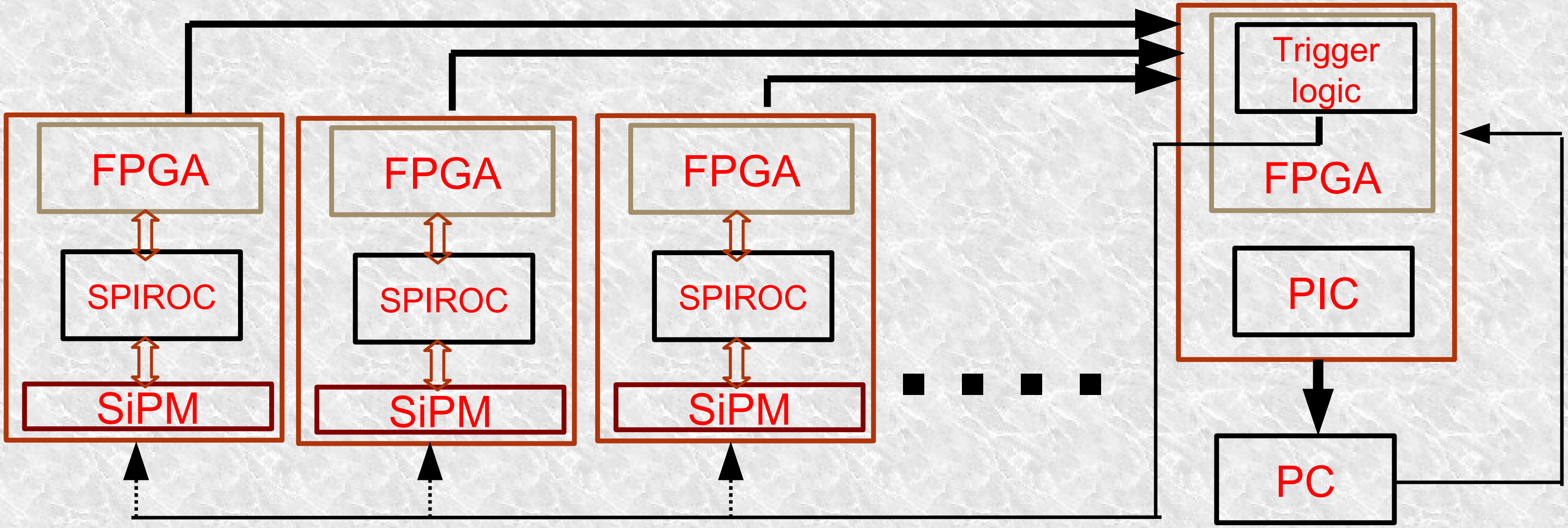
The slope is similar for all the SiPM: ≈80 mV/°C



- A mix of the two is the current MuRay approach: work at a temperature within 5-10 °C below ambient temperature in order to save power and keep dark count under control and then compensate residual variations by changing Vb.
- Need full characterization of SiPMs Vbkd at least for one value of T (the slope is almost the same for all sensors)

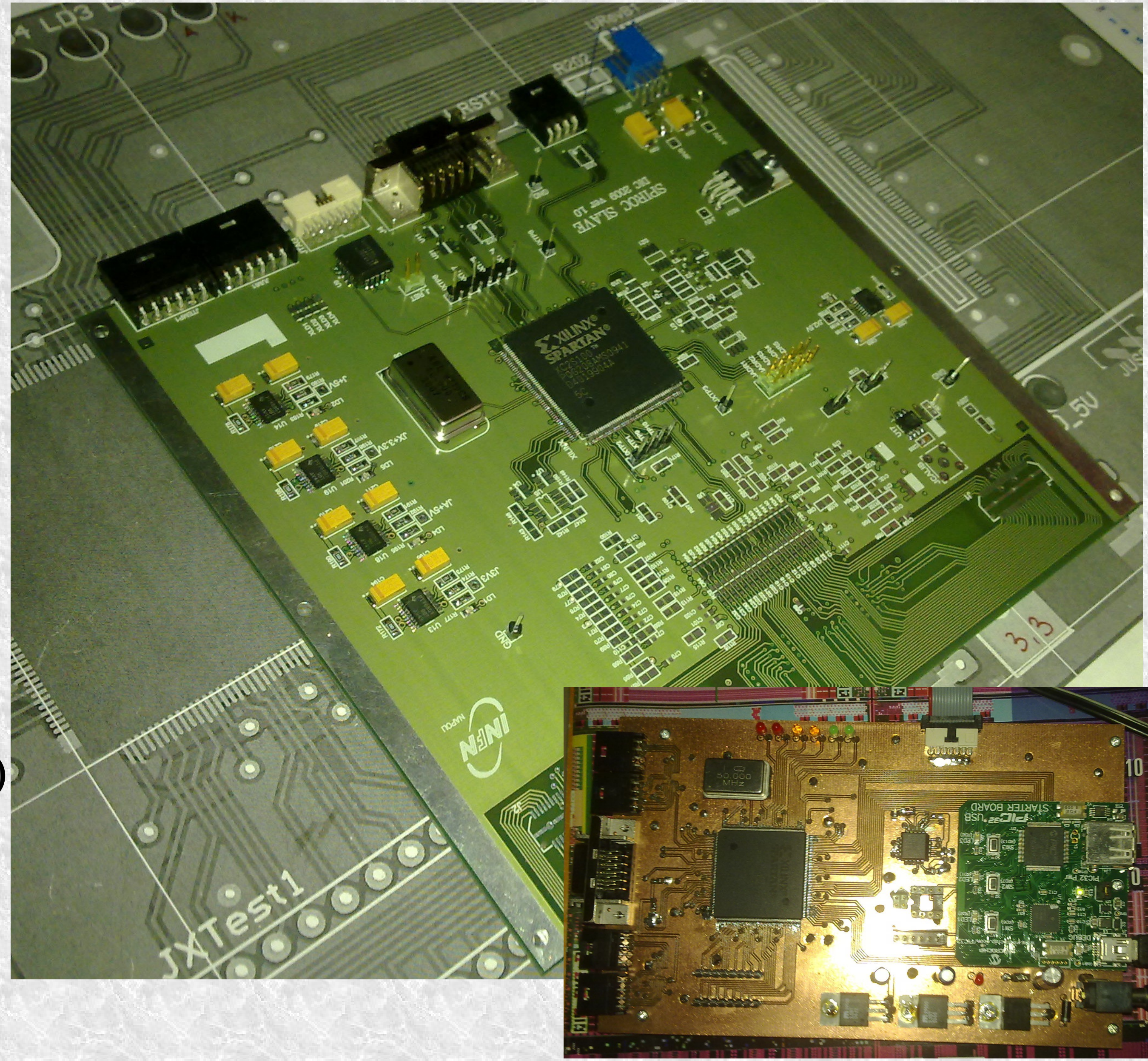
MuRay DAQ Layout

- Based on SPIROC chips, able to control 36 ch each (32 used)
- SPIROCs are host in boards controlled by FPGA (SLAVES)
- One MASTER provides the trigger logic.
- All the SLAVEs work in RUN mode, i.e. until a trigger is produced the FPGA clock is OFF and all the logic is combinatorial and power consumption is limited.
- Power consumption about 1.5 W /slave board (3 W for the Master)



The MuRay Prototype SPIROC Board

- Board designed by the Servizio di Elettronica in Naples
- Logic functions implemented XILINX Spartan FPGA
- Houses the SPIROC (LAL) chip
- Has a time expansion TDC.
- In the inset a board with a PIC to control temperatures (and other slow parameters)



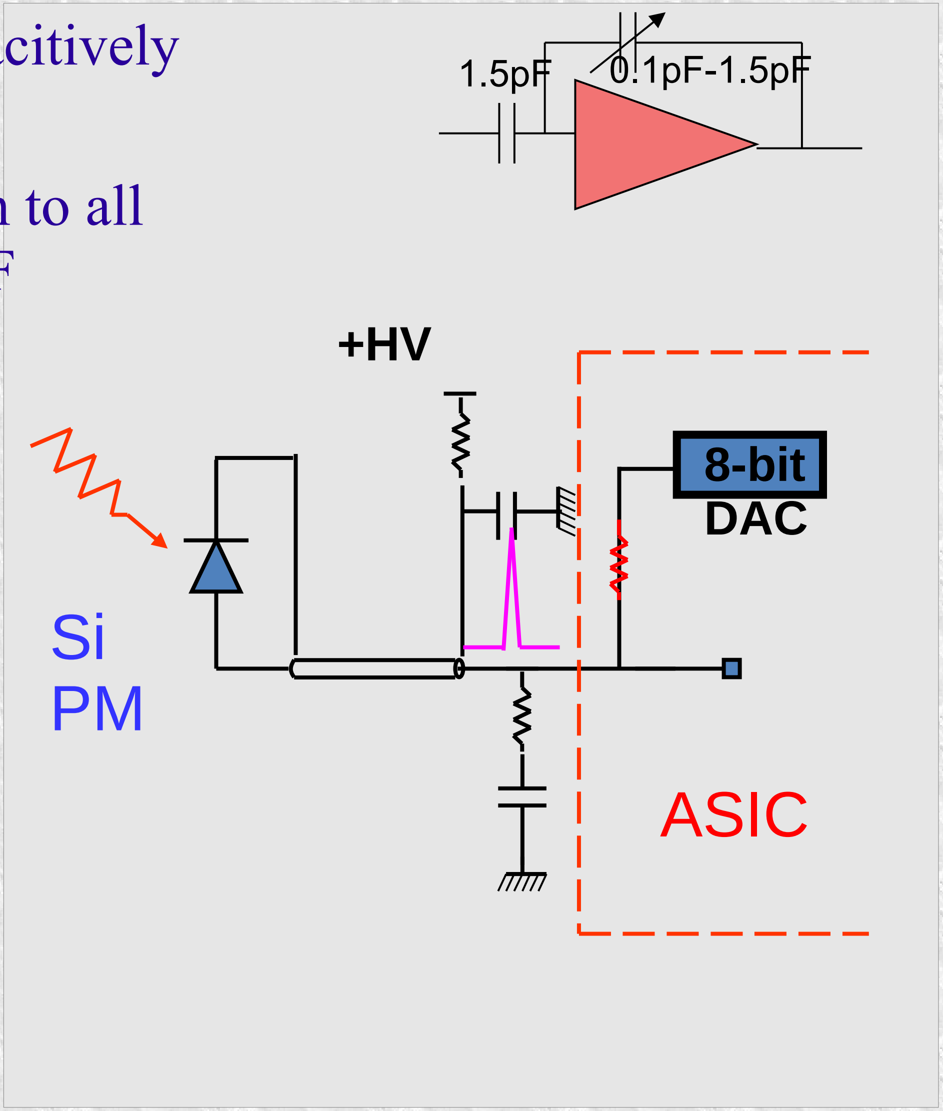
The SPIROC chip

Stéphane Callier, Frédéric Dulucq, Julien Fleury, Gisèle Martin-Chassard, Christophe de La Taille, Ludovic Raux
IN2P3/OMEGA-LAL - Orsay, France
raux@lal.in2p3.fr

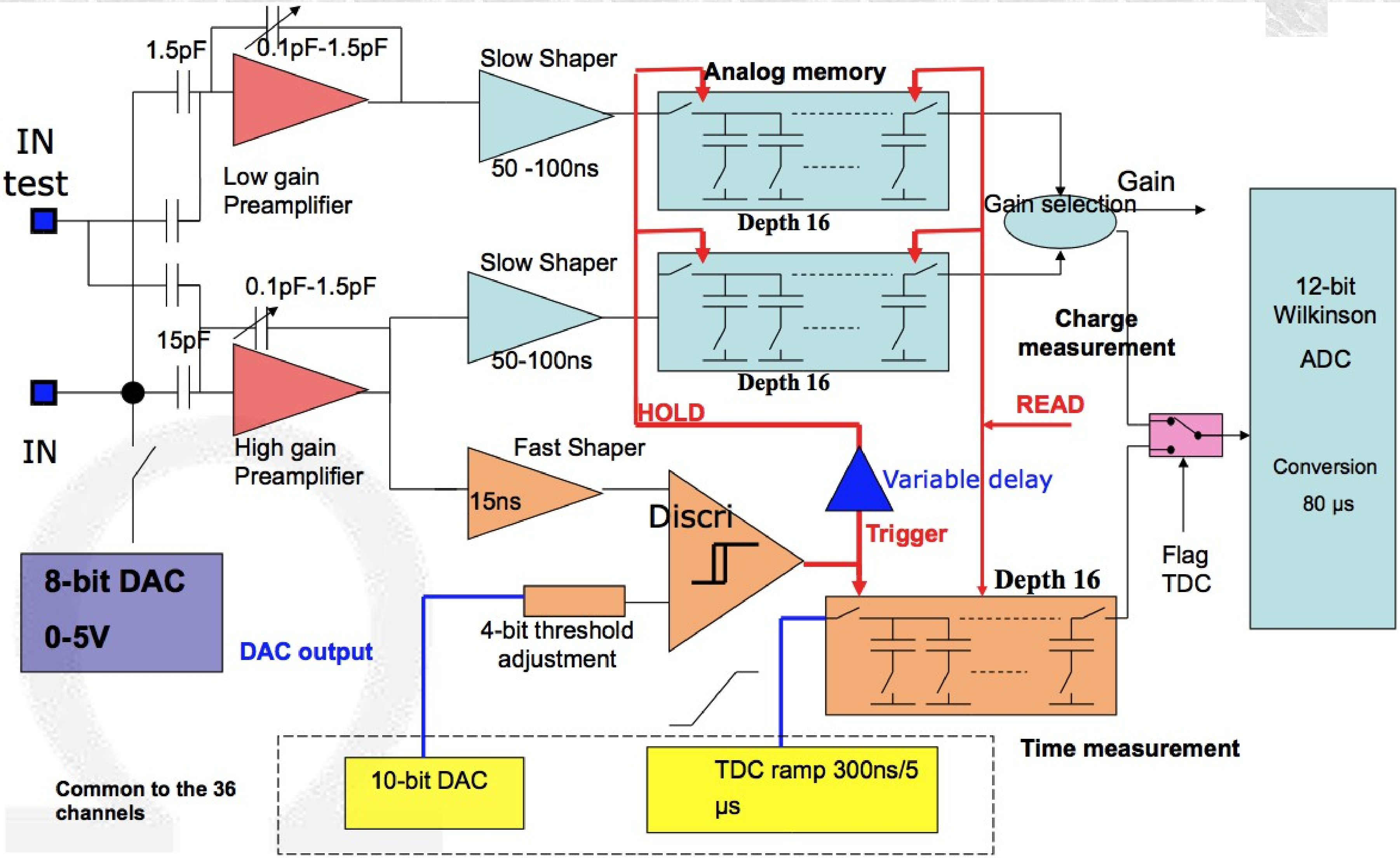
- 36-Channel ASIC
- 8-bit DAC(0-5V) for individual SiPM gain adjustment
- Energy measurement:14bits
  - 2 gains (1-10) + 12 bit ADC 1 pe!2000 pe
  - Variable shaping time from 25ns to 175ns
  - pe/noise ratio : 11
- Auto-trigger on MIP or spe
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~15ns
  - Auto-Trigger on 1/3 pe (50fC)

SPIROC (2)

- Bi-gain low noise preamp
  - Low noise charge preamplifier capacitively coupled = voltage preamplifier
  - Gain adjustable with 4 bits common to all preamps : Cf=0.1, 0.2, 0.4, 0.8 pF
- Positive input pulse
- 8 mV/pe in High Gain
- Noise : 1.4 nV/sqrt(Hz)
- Power : 2 mW (unpulsed)
- Low gain at preamp level
- 0.8 mV/pe, MAX : 2000 pe (300pC)



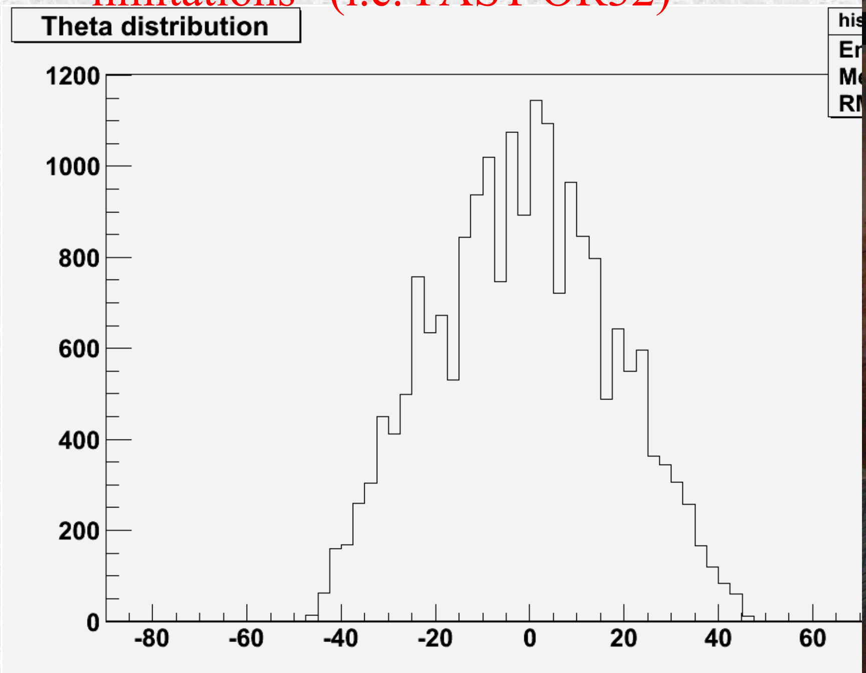
SPIROC Chip (3)

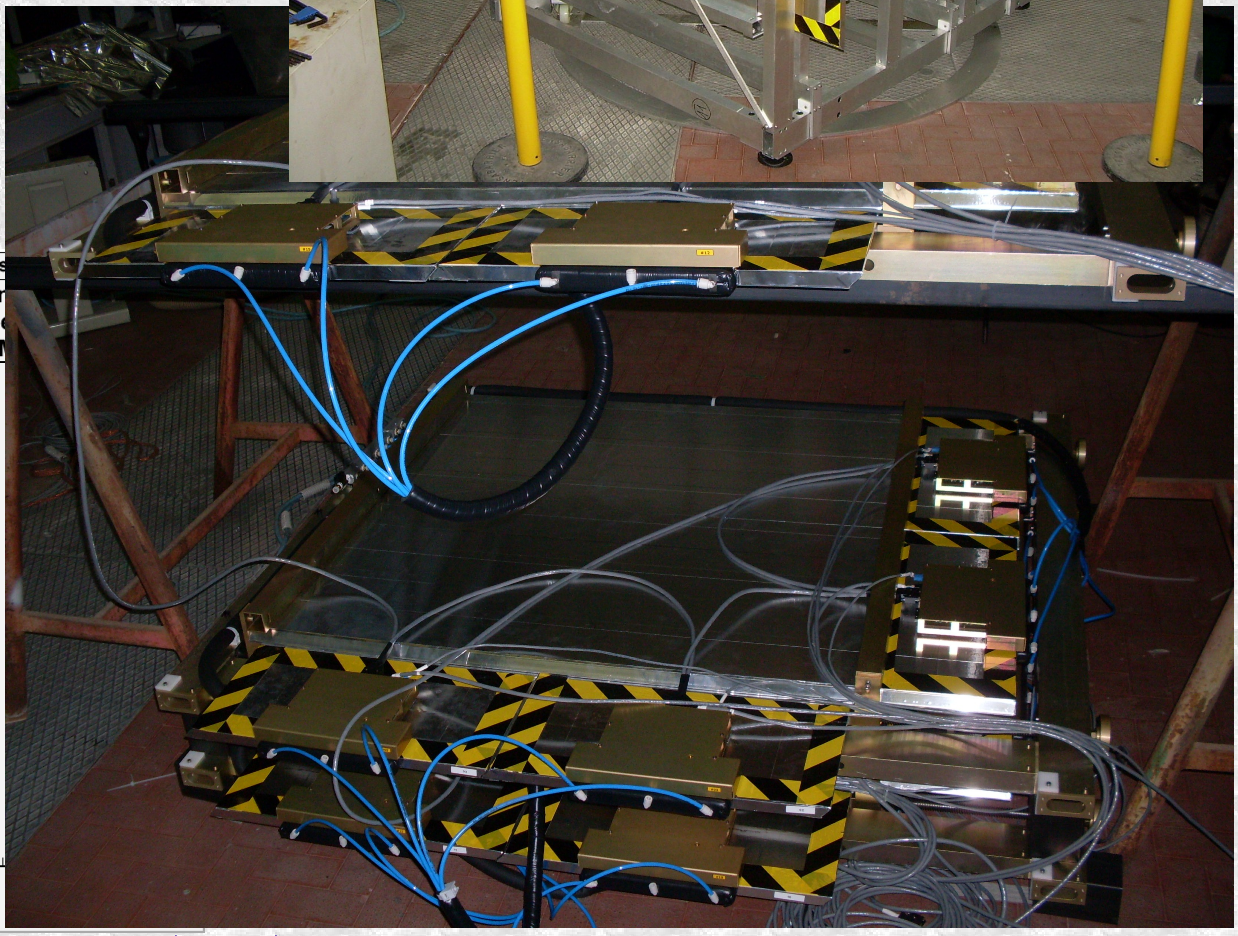


A complete module & plane

Telescope Prototype

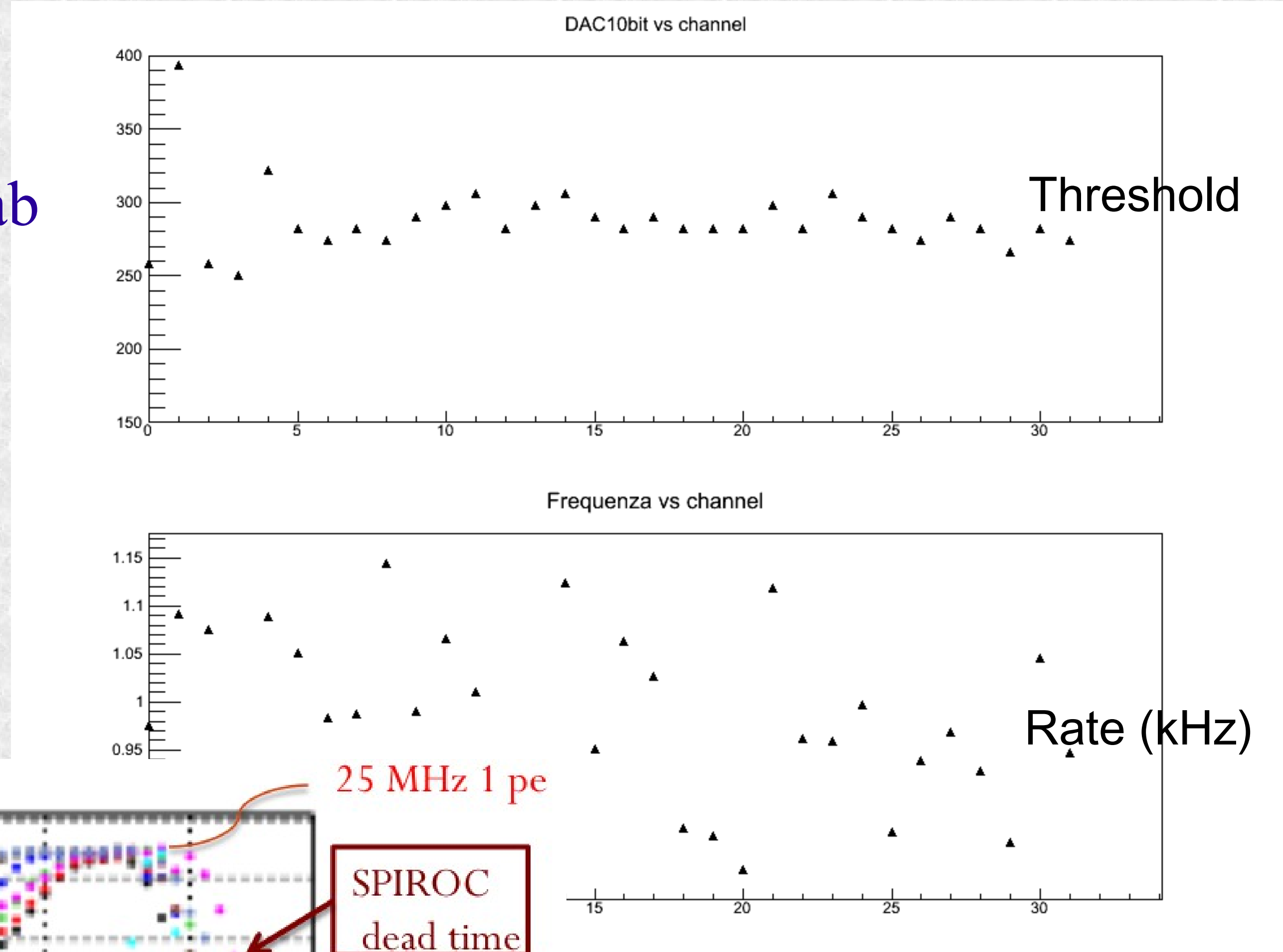
- Now taking data in Naples
- Commissioning and understanding the detector given:
- Dark Count in excess of 5 MHz
- Possibly low PDE
- OLD Spiroc technology which imposes "limitations" (i.e. FAST OR32)

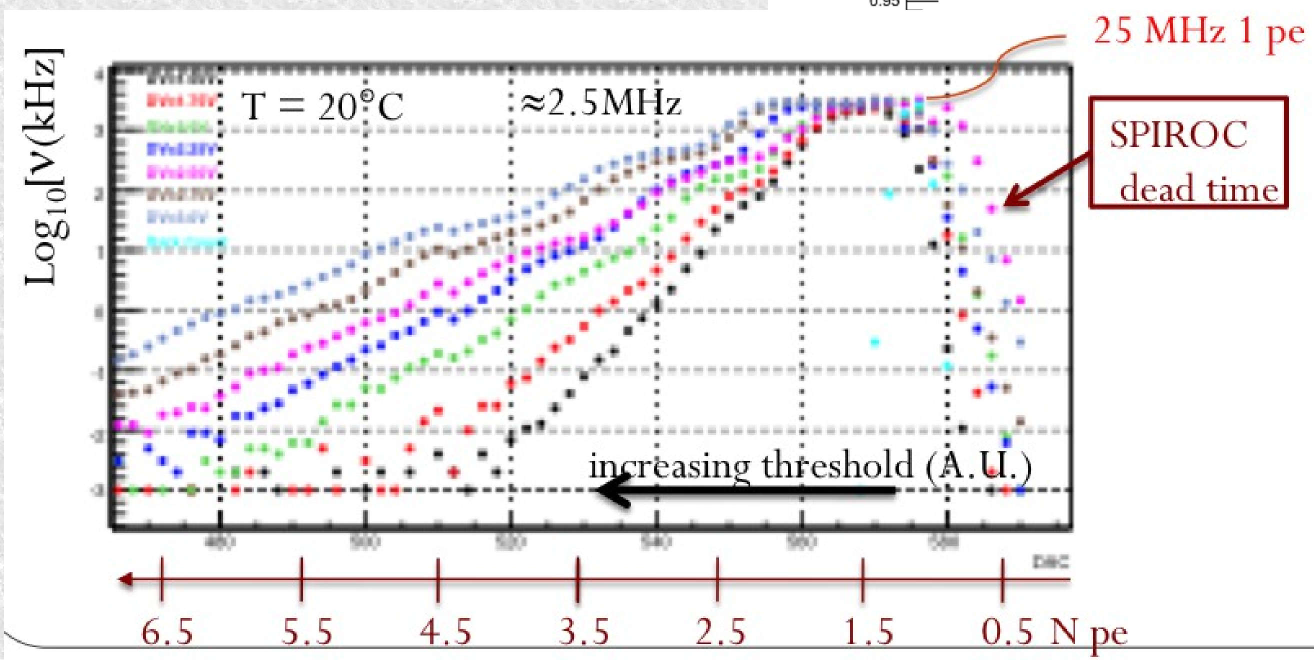




Commissioning

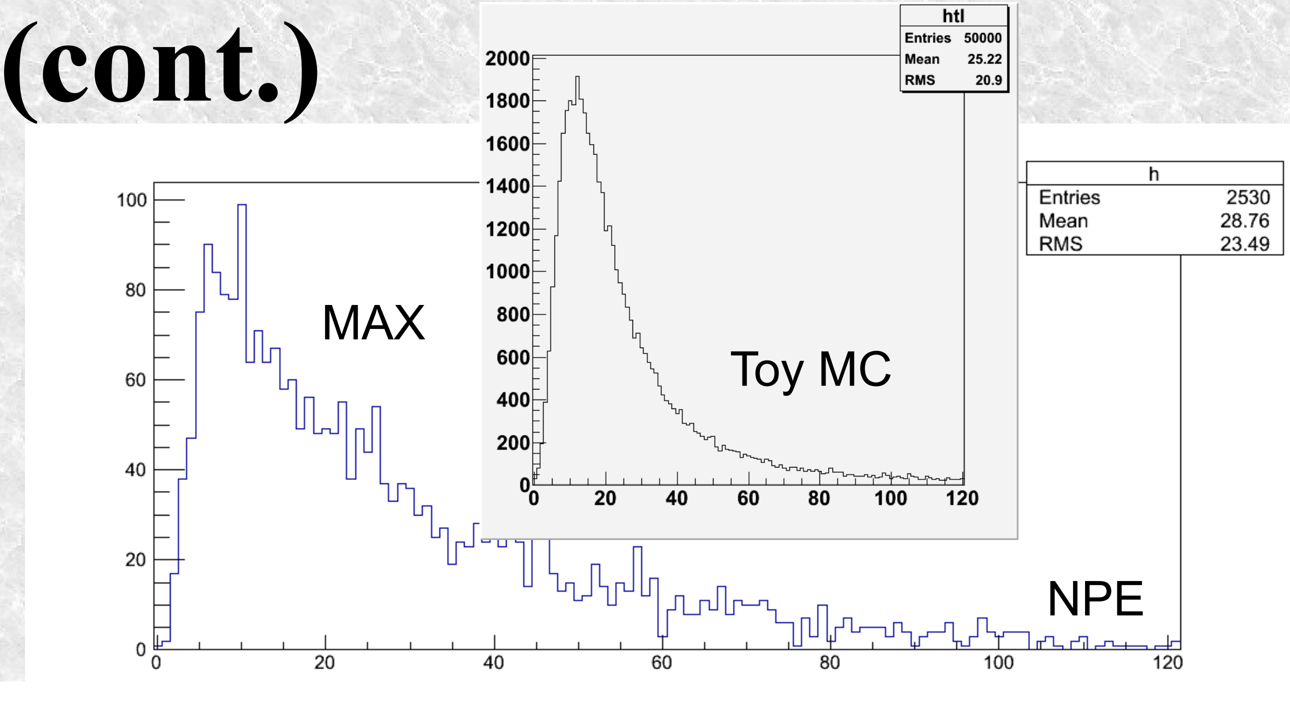
- Detector mounted in the lab pointing at the zenith
- Choice of working point (threshold and Vbias equalization)
- Testing of reconstruction and analysis software

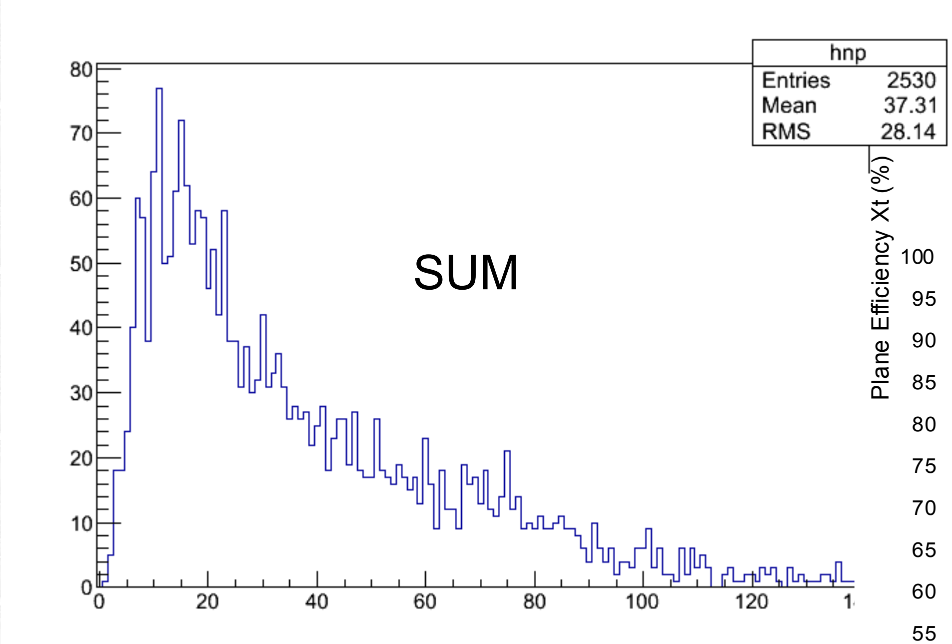


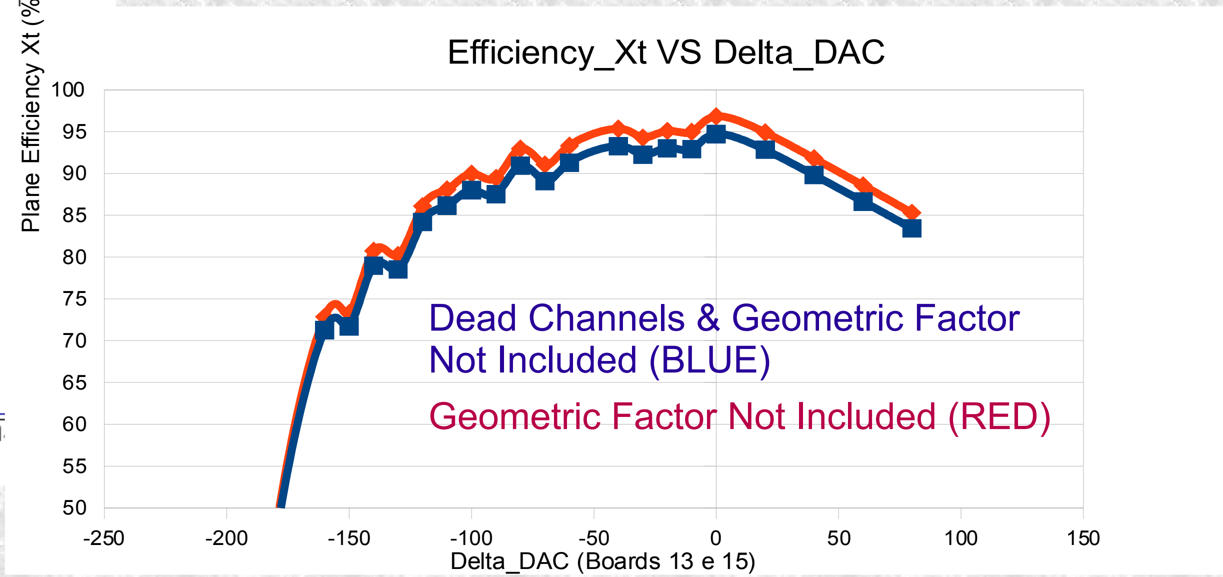


Telescope Tests (cont.)

- SUM Signal of two bars and MAX Signal of highest bar with custom amplifier coupled to FBK SiPM.
- Using FAST OR32, looking at plane efficiencies with FBK SiPM and SPIROC.

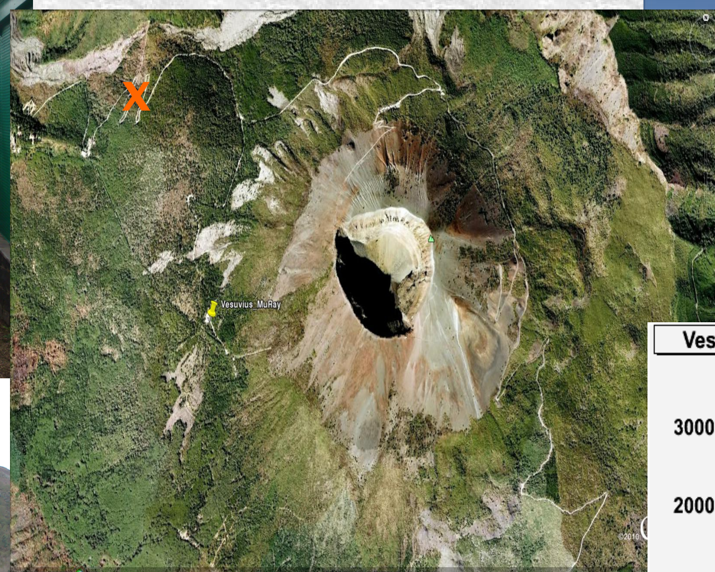


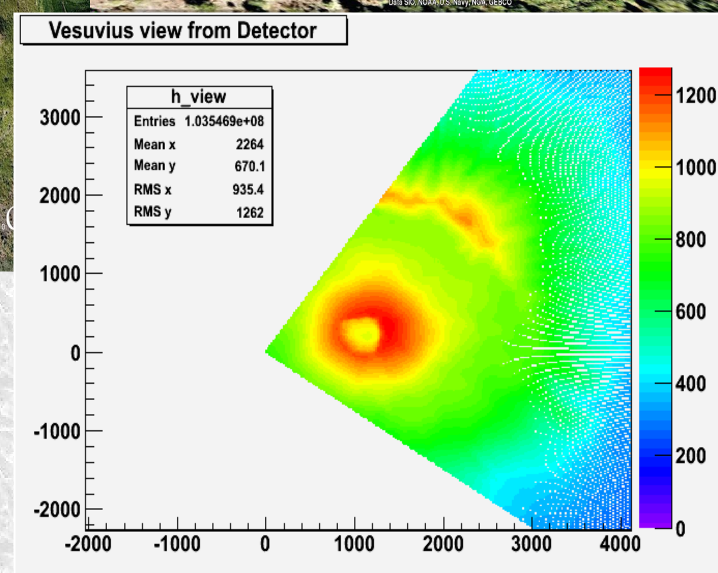




First Field Test

- After the commissioning and characterization of the detector in the laboratory we plan to move the detector to Mt Vesuvius, where the infrastructure is already available.





Another possibility ...

- Monte Olibano (duomo di lava)

- Campi Flegrei

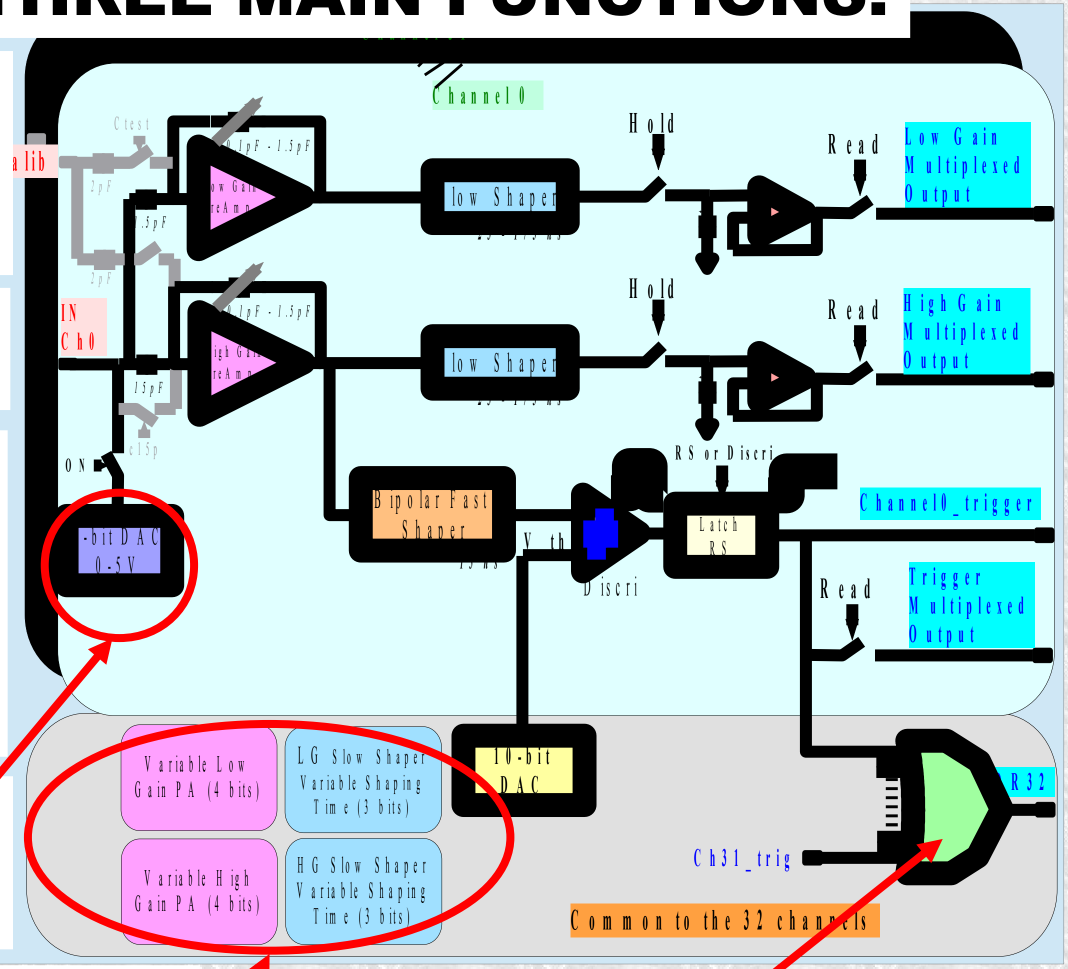
«EASIROC»

EASIROC 32 CH ASIC HAS THREE MAIN FUNCTIONS:

1) 32 CH LOW GAIN, PROGRAMMABLE SHAPING, VOLTAGE MEASUREMENT PATH THAT HAS SAMPLE AND HOLD CAPABILITY

2) 32 CH HIGH GAIN , PROGRAMMABLE SHAPING, LIKE PREVIOUS ONE

3) 32 CH FAST TIMING PATH, WITH COMMON THRESHOLD PROGRAMMABLE COMPARATOR WITH 32 OUTPUTS. MAIN DATA IN TIMING APPLICATION AND ARE FED TO THE FPGA CHIP TO BE PROCESSED AS REQUESTED.



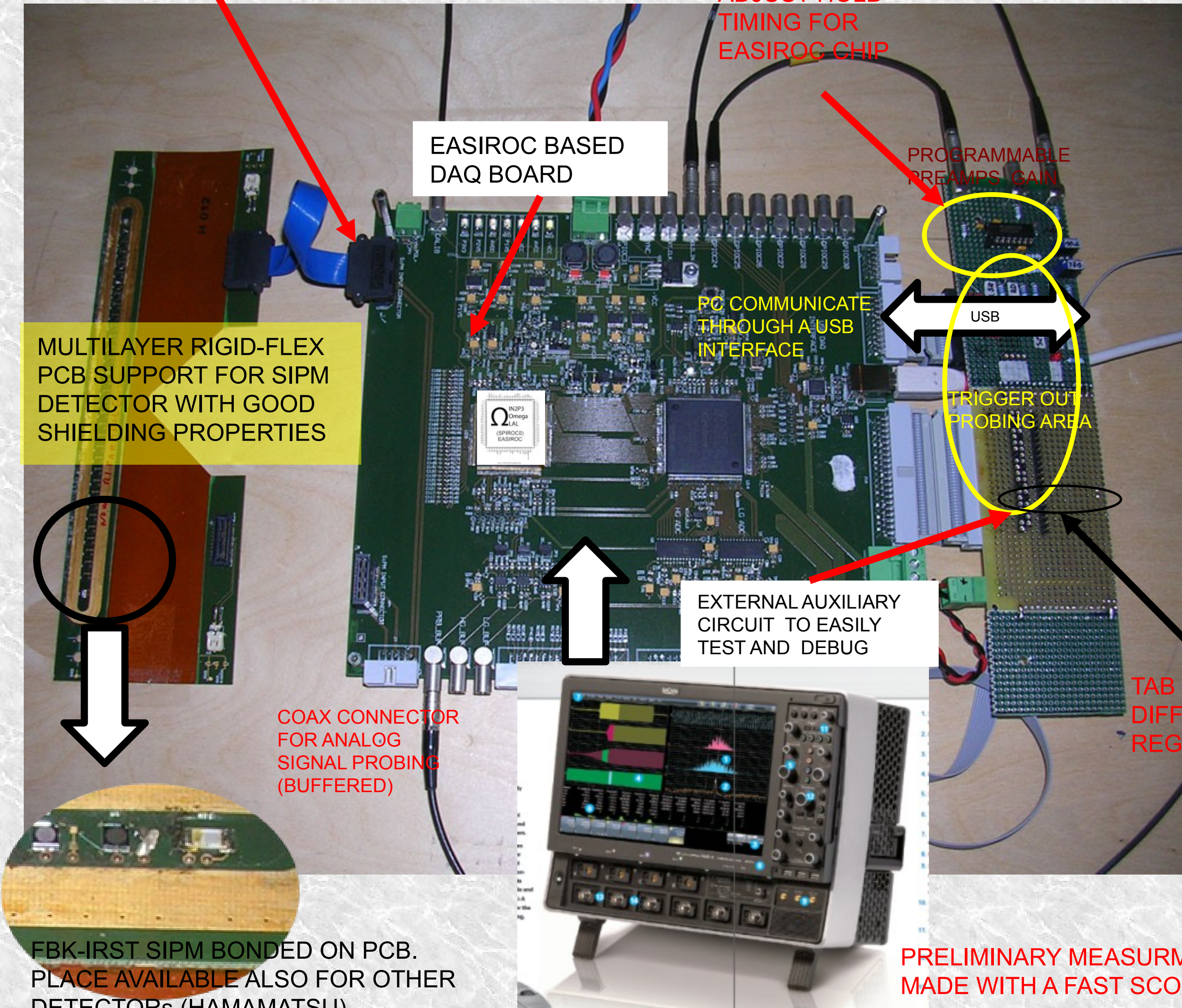
SiPM BIAS VOLTAGE CAN BE PRECISELY ADJUSTED FOR EACH CHANNEL BY A PROGRAMMABLE 5V DAC

IN ORDER TO PROPERLY CONFIGURE AND PROGRAMM THE CHIP, 3 REGISTERS CAN BE SERIALLY ACCESSED : «SLOW CONTROL» REG, »READ» REG. , «PROBE» REG.

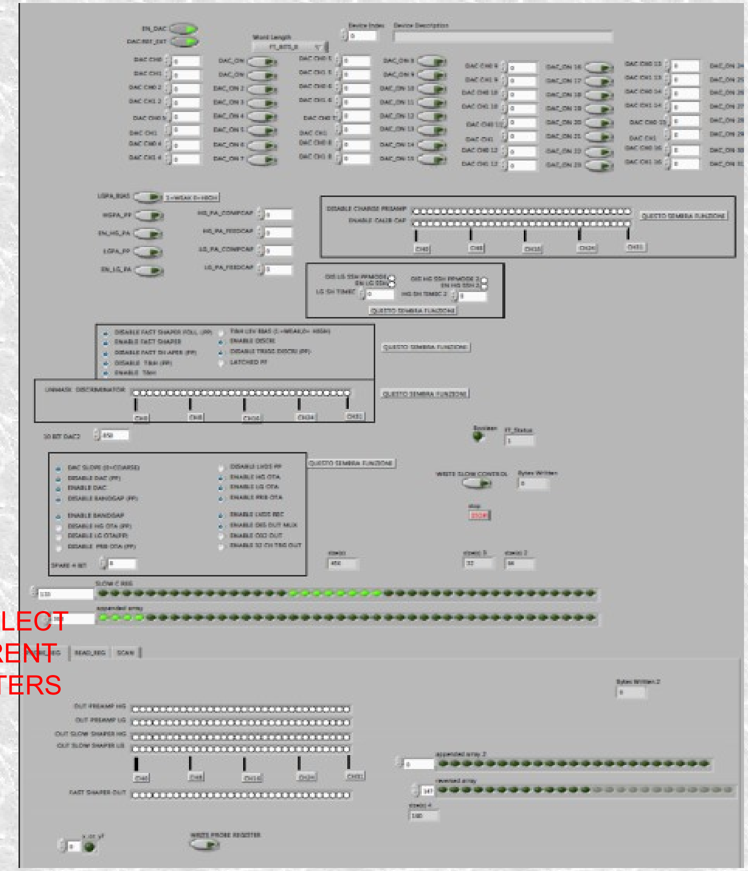
«OR32» FAST SIGNAL USED TO TRIGGER ACQUISITION SEQUENCE

EASIROC with single SiPM

SIPM TEST SET-UP using the modified hybrid



-LABVIEW SIMPLE INTERFACE ALLOW TO PROGRAM EASI-ROC CHIP REGISTERS
-SLOW CONTROL,
- READ AND PROBE REGISTERS
- WE CAN ALSO SET OVER-BIAS FOR EACH SINGLE SIPM THROUGH A DAC SETTING

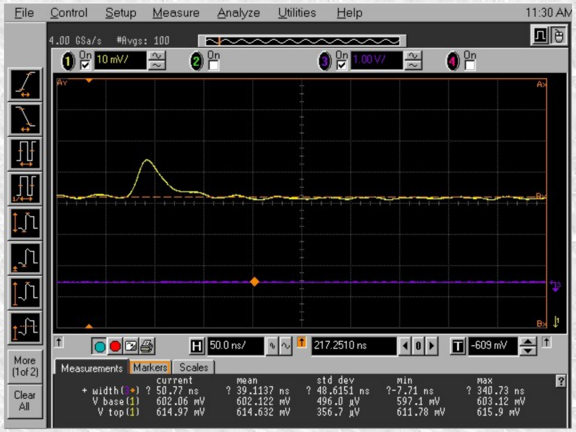


PRELIMINARY MEASURMENTS MADE WITH A FAST SCOPE

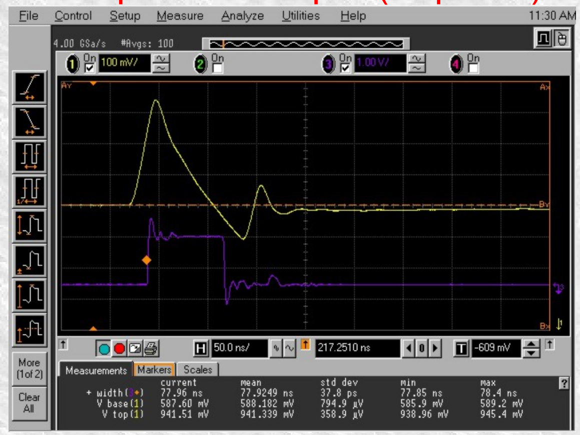
EASIROC tests (1)

- Tested response of comparator channel and “slow” (60ns) channel.
- Use of an appropriately formed input pulse.

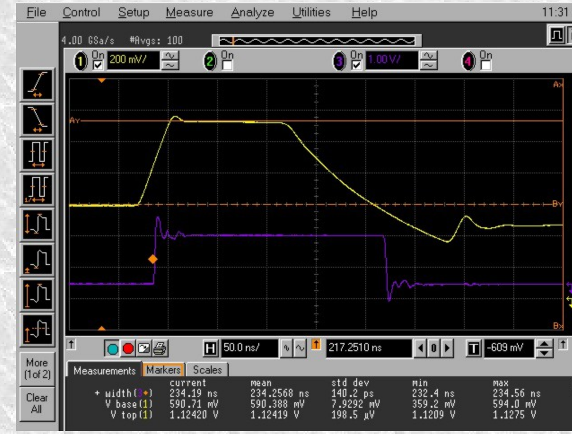
Comparator Shaper (“Bipolar”)



HIGH GAIN =15, VIN = 0.25mV

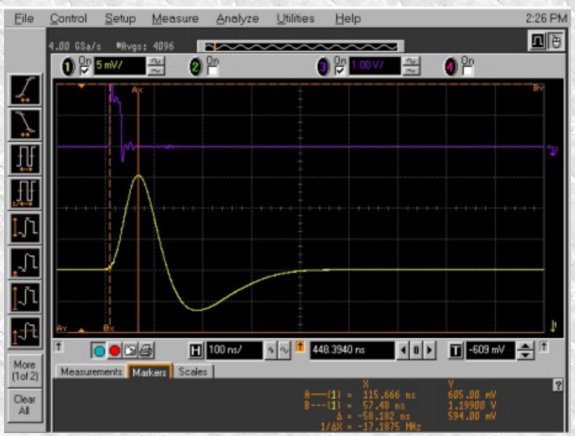


HIGH GAIN =15, VIN = 8mV

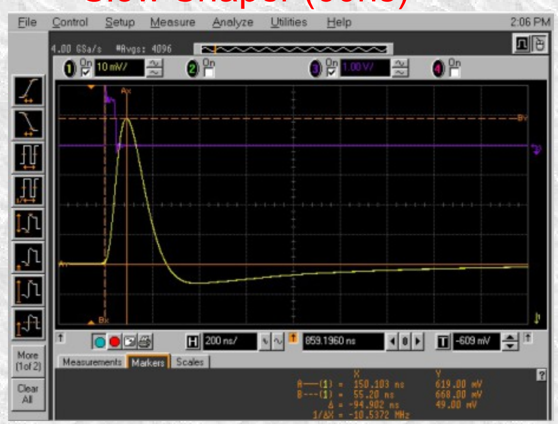


HIGH GAIN =15, VIN = 80mV

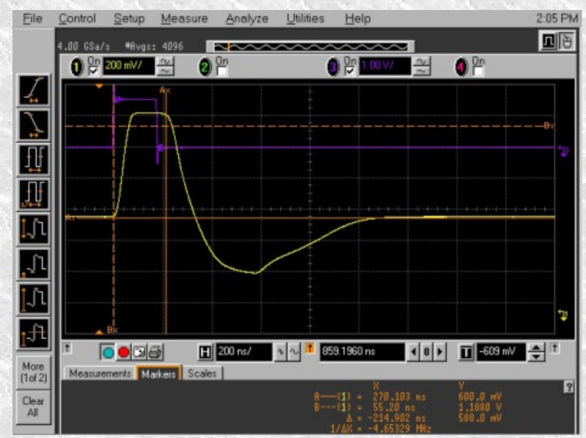
Slow Shaper (60ns)



GAIN HGPRE=0 SSTIME=6 VIN=2.2mV



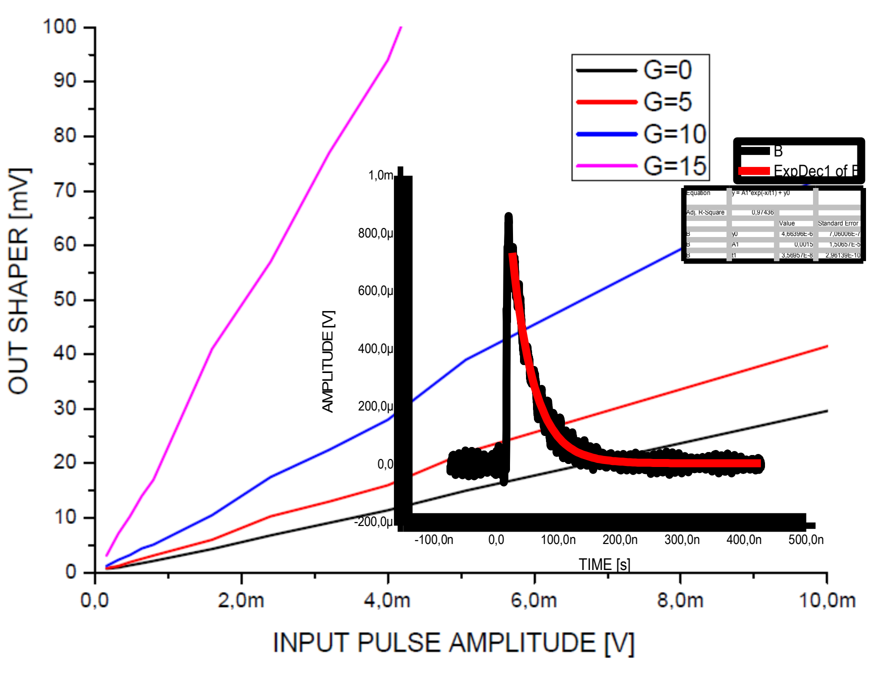
GAIN HGPRE=15 SSTIME=6 VIN=2.2mV

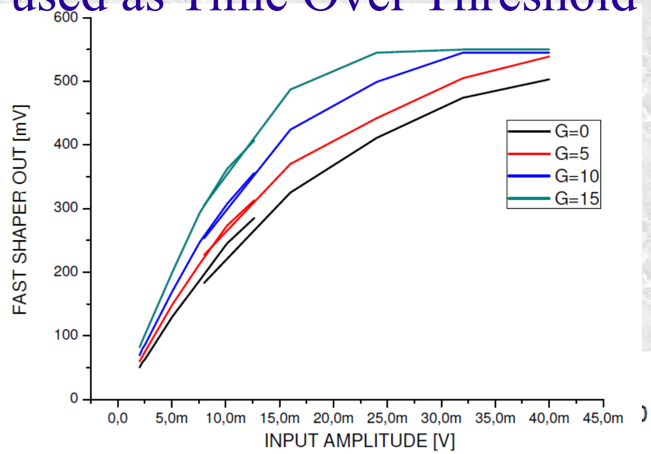


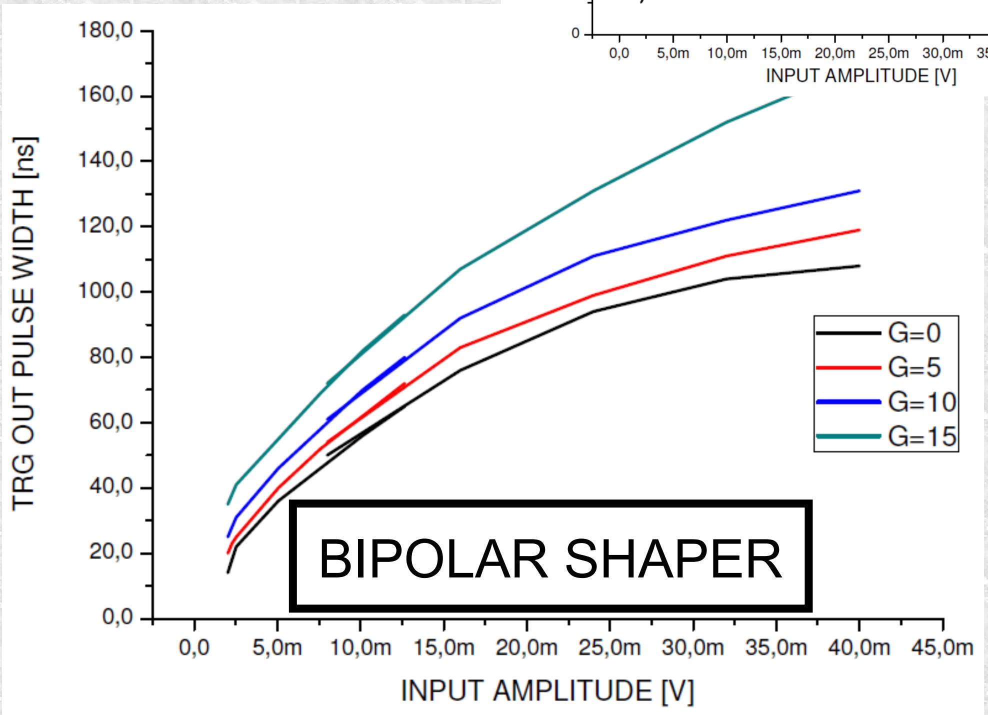
GAIN HGPRE=15 SSTIME=6 VIN=126mV

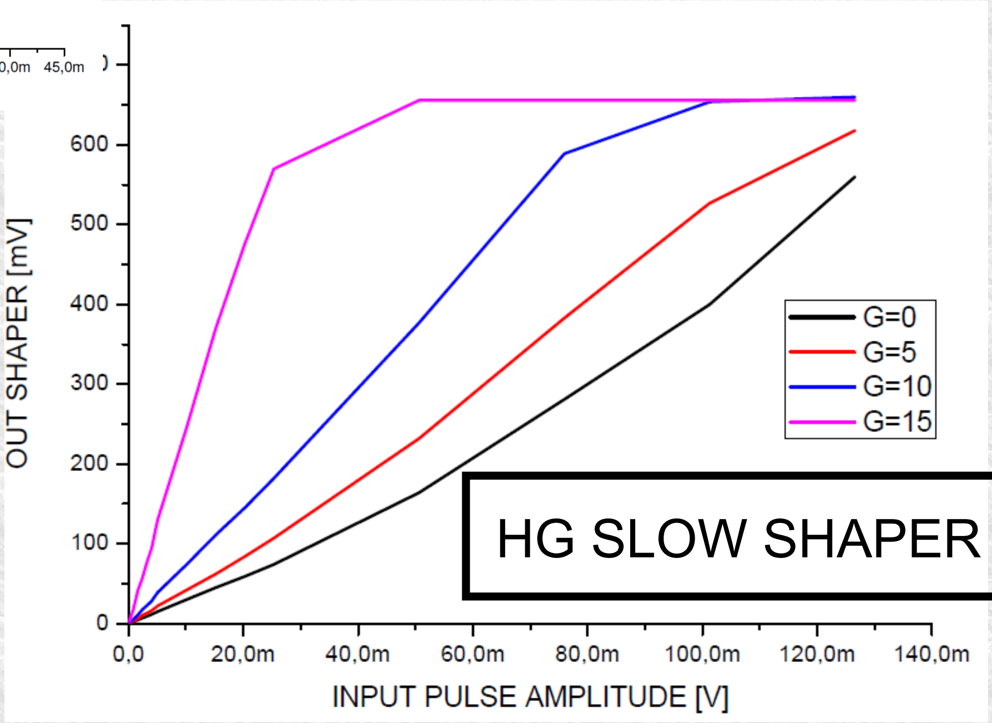
EASIROC tests (2)

- Slow shaper (60ns) channel well behaved.
- If Dark Count Rate too high ….
- Comparator Output used as Time Over Threshold ?



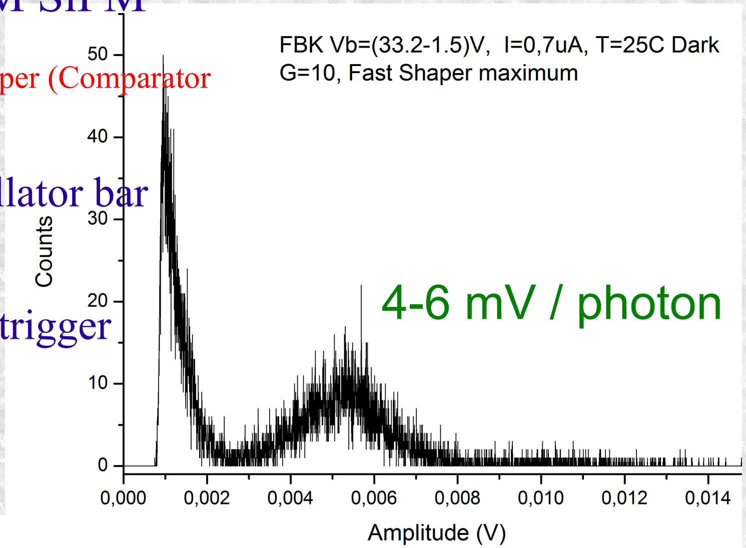


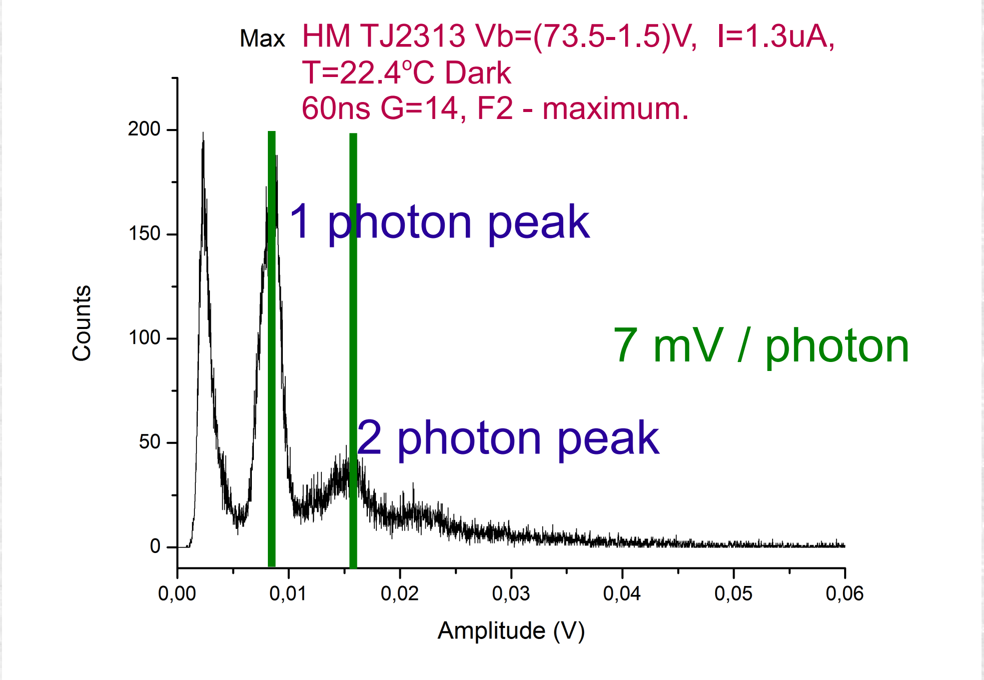


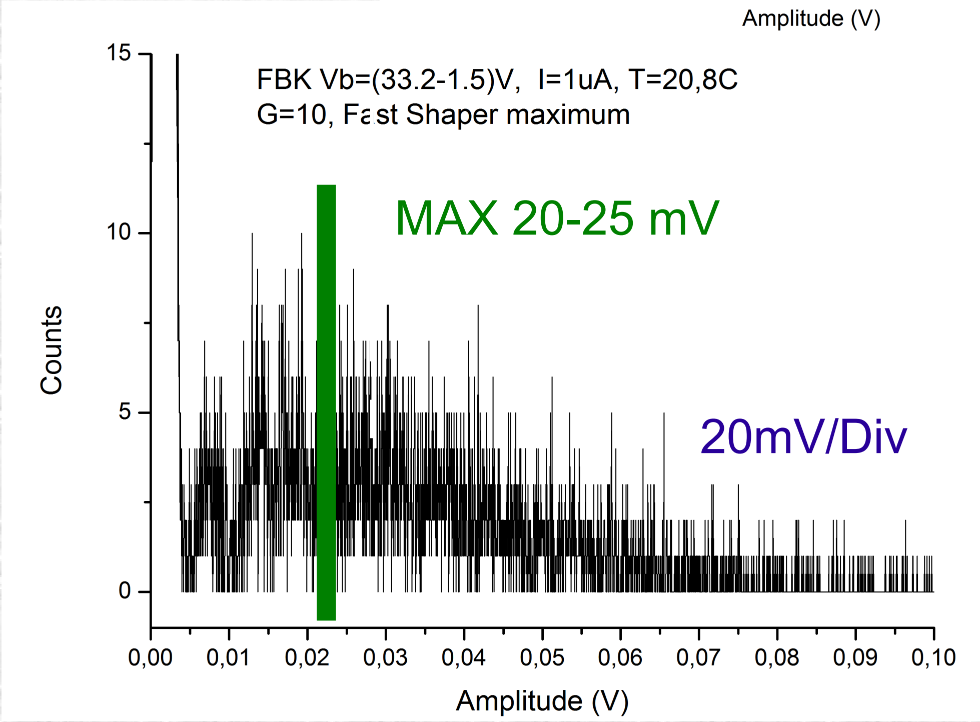


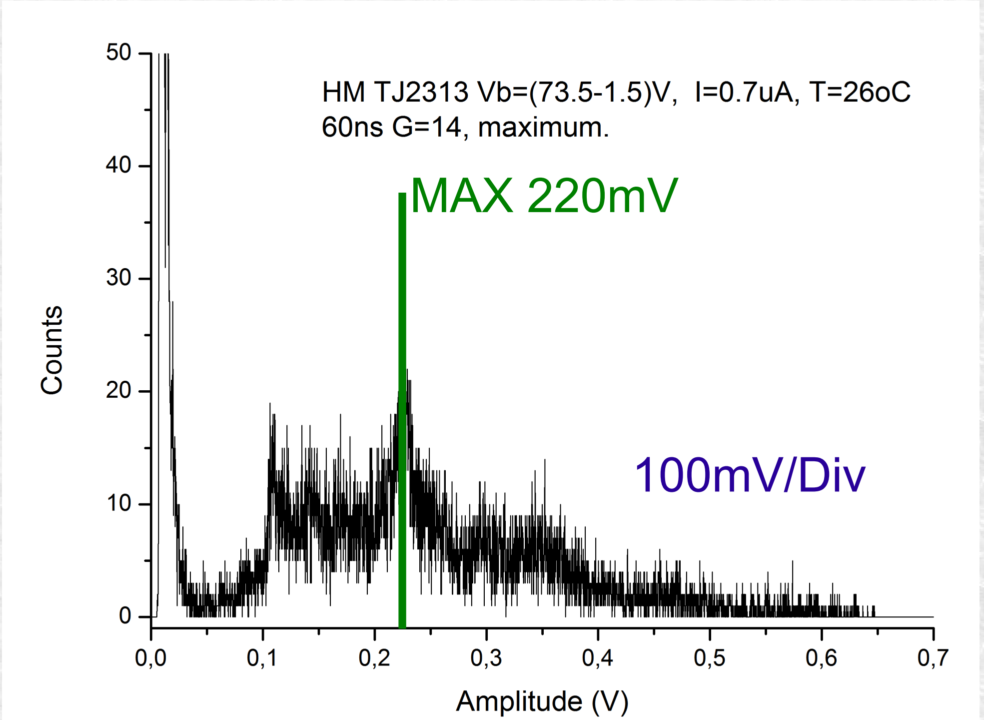
EASIROC tests (3)

- Used EASIROC coupled to FBK and HM SiPM
- NB. FBK --> Fast Shaper (Comparator channel) !!
- Triangular scintillator bar with WVLS
- External cosmic trigger





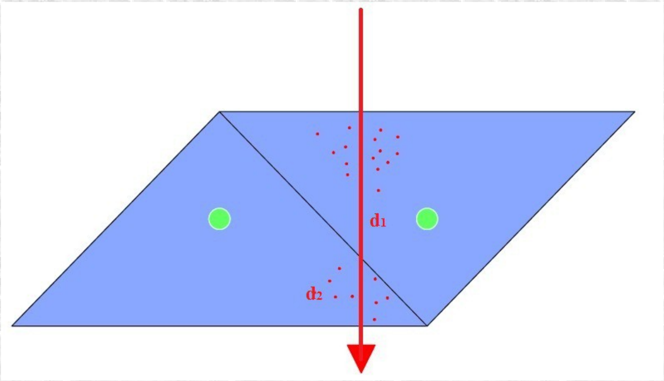


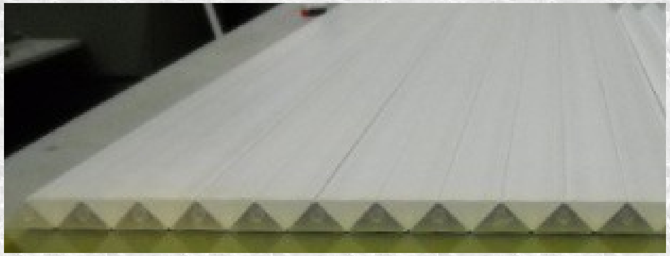


Conclusions

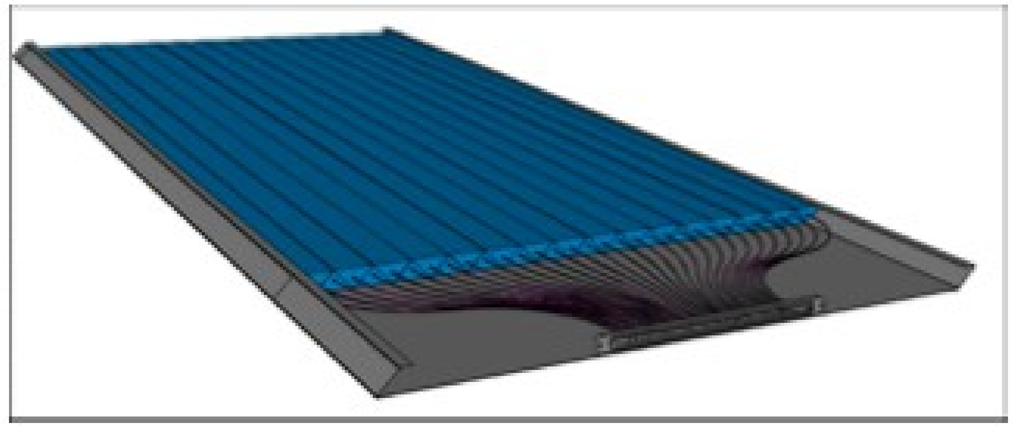
- The MuRay telescope concept (MNT2012 workshop (Clermont Ferrand-France)) has now become the basis for new proposals in the field of Muon Radiography
- This field is truly interdisciplinary and apart the obvious scientific interests involves also civilian protection and mineralogy interests.
- Our group is in the final stages of testing the 1m^2 prototype
- Plans are ahead for a new production run of SiPM at IRST
- The SPIROC based FE board will be replaced by a newer and more functional one based on EASIROC
- Four 1m^2 modules will be the next step
- The goal is a 10 m^2 modular structure for "real time" and/or stereoscopic observations.

Backup:Fermilab scintillator factory





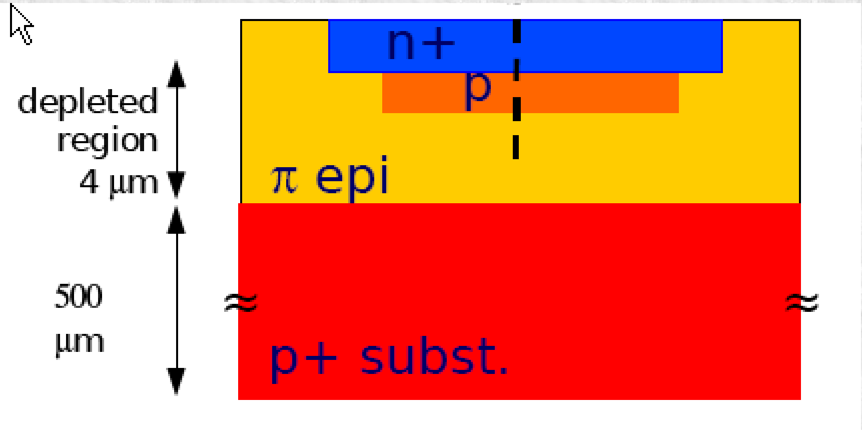
Detector Plane with stacked scintillator bars

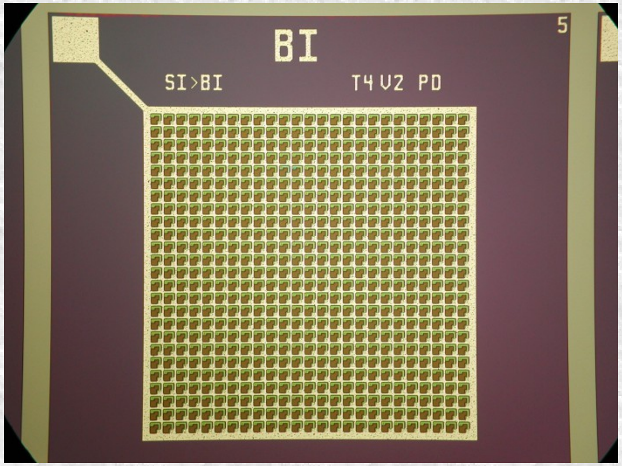


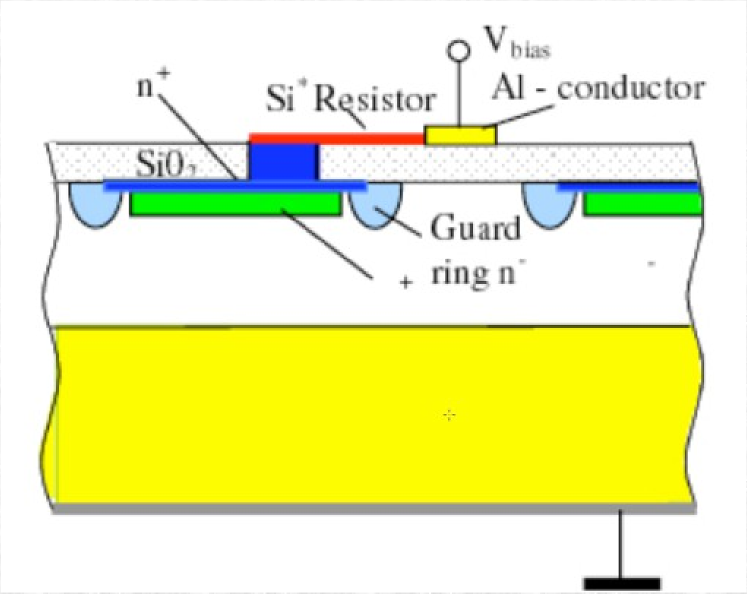
- Scintillator extruded in triangular bars
- A 1.8 mm hole runs through the scintillator bar

Backup:SiPM

- SiPM
- High gain
- Low noise
- Low voltage
- Small form factor







Avalanche diodes used in Geiger mode (avalanche quenched by a series resistor)

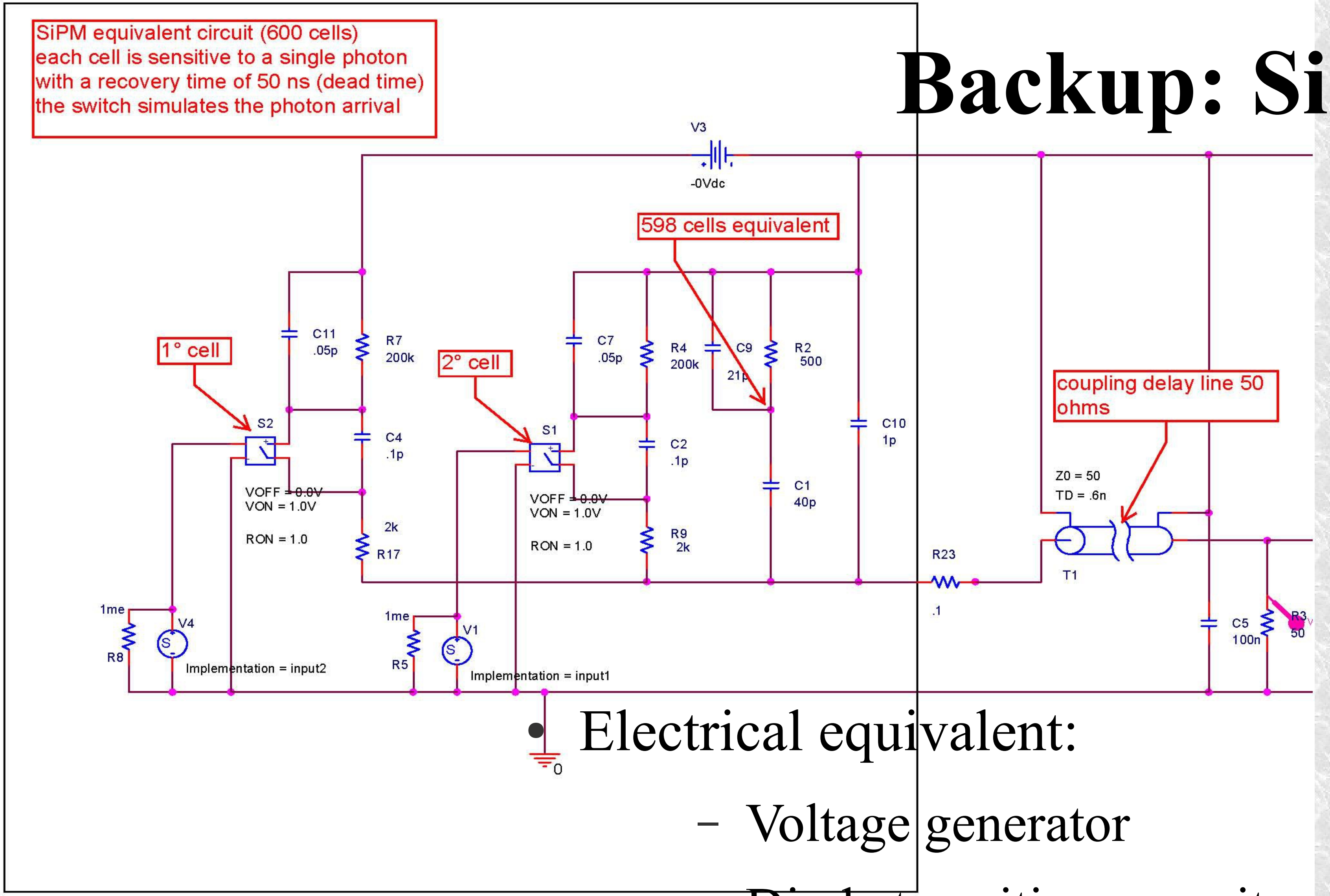
Quenching resistance made of doped polysilicon

Anti/reflective coating optimized for 420 nm

Single cell size 40µm to 400µm

Sensor size up to 3x8 mm^2 (used 1.4x1.4 mm^2)

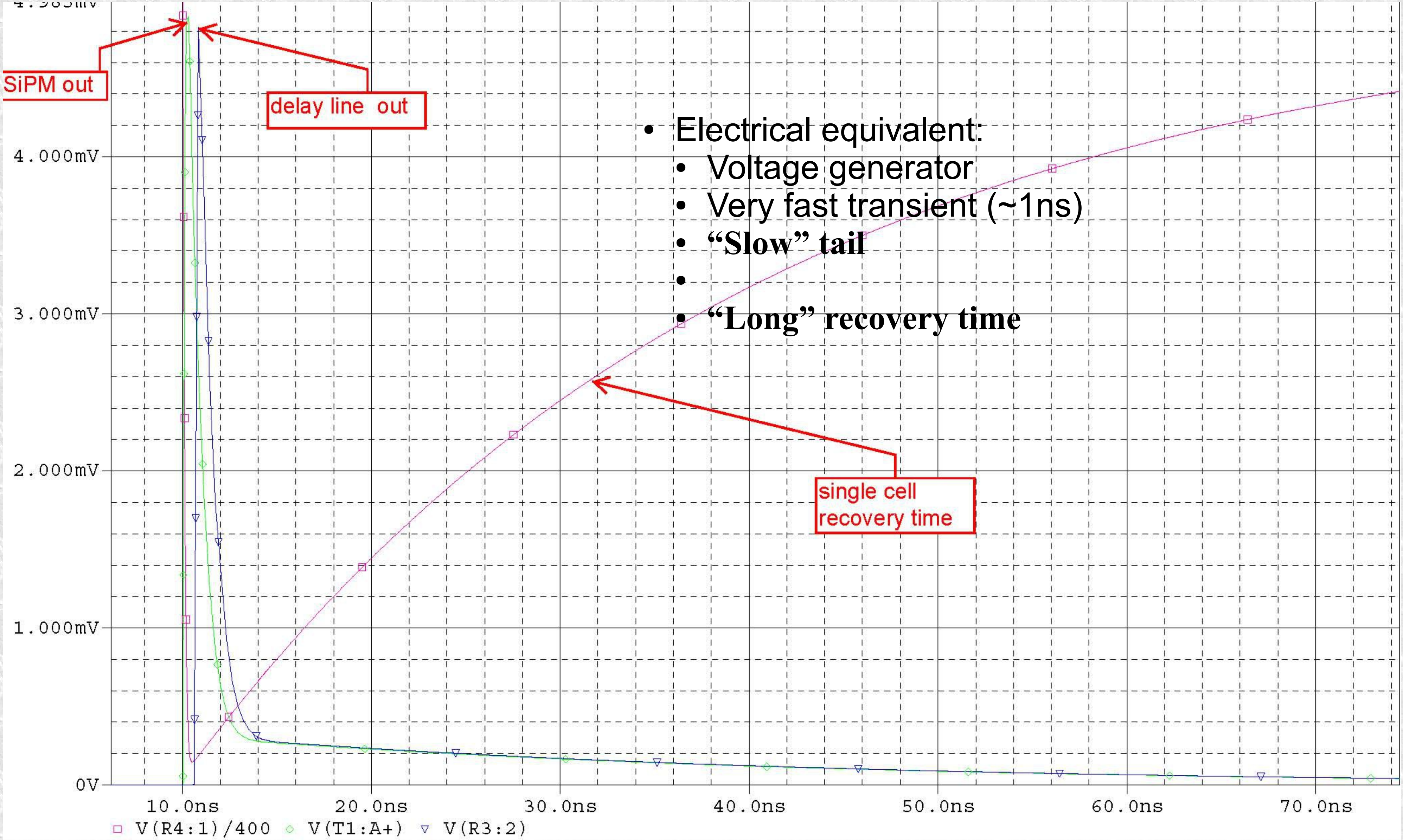
Backup: SiPM (1)



- Electrical equivalent:
  - Voltage generator
  - Diode transition capacitance
  - Avalanche discharge
  - **Charge released = $\Delta V * C_T$.**

Backup: SiPM (2)

- Electrical equivalent:
  - Voltage generator
  - Very fast transient (~1ns)
  - **“Slow” tail**
  -
  - **“Long” recovery time**

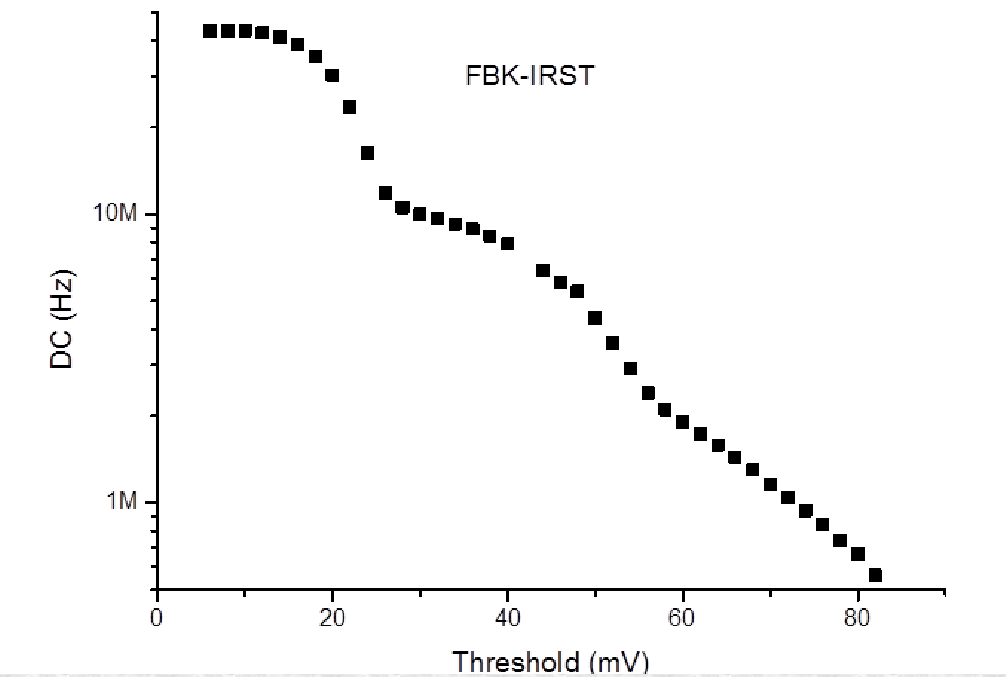


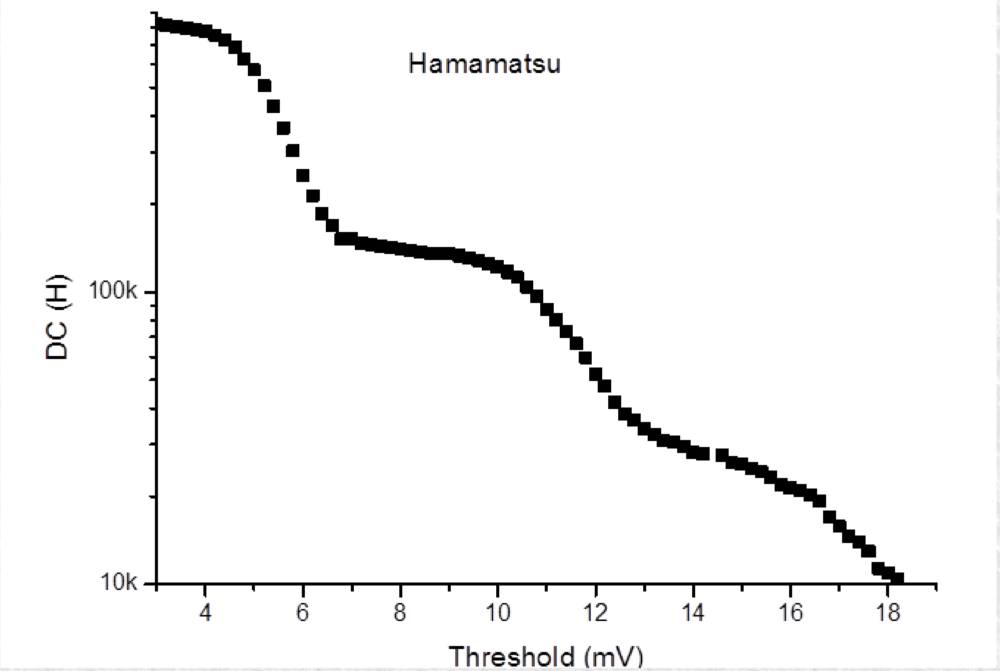
Backup: SiPM characterisation

Dark count rate vs threshold **(obtained with LeCroy SDA 760Zi: 6 GHz)**

DC at 20 °C and 5,5 V overvoltage

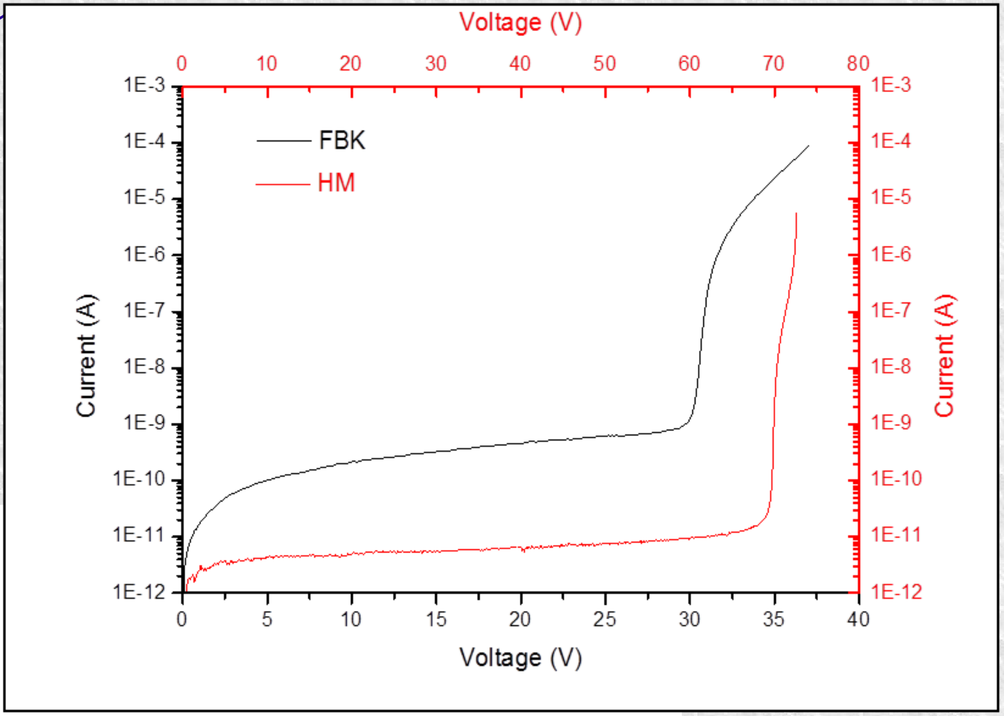
DC at 20 °C and 2 V overvoltage

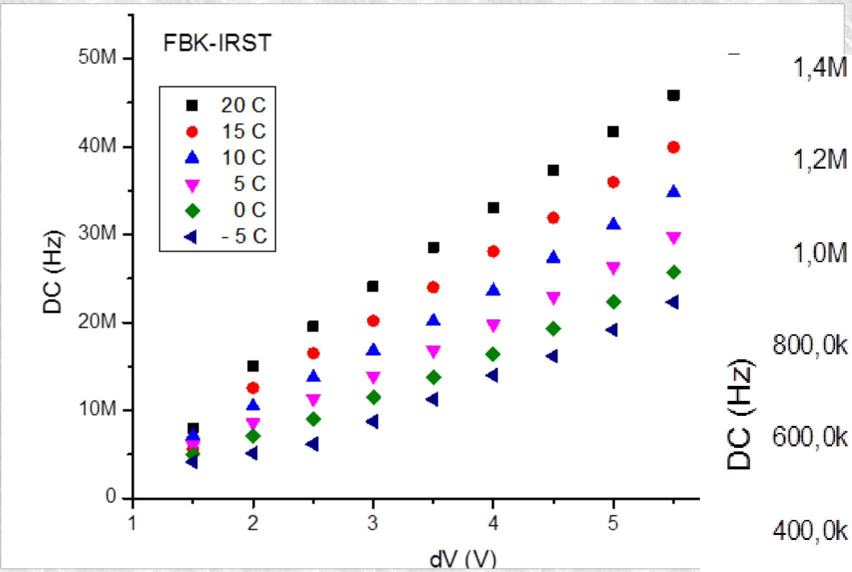


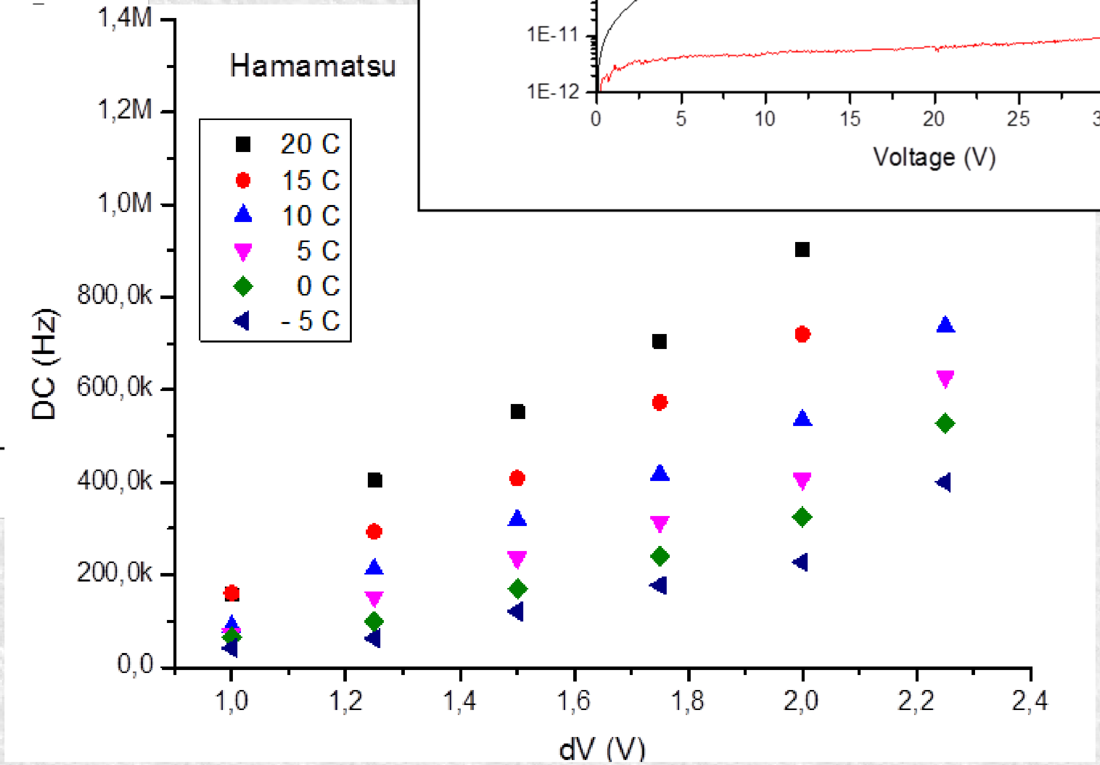


Backup: SiPM characterization

- Reverse IV curves for Hamamatsu and FBK at 20°C
- Dark Count rate
- Gain
- Etc.



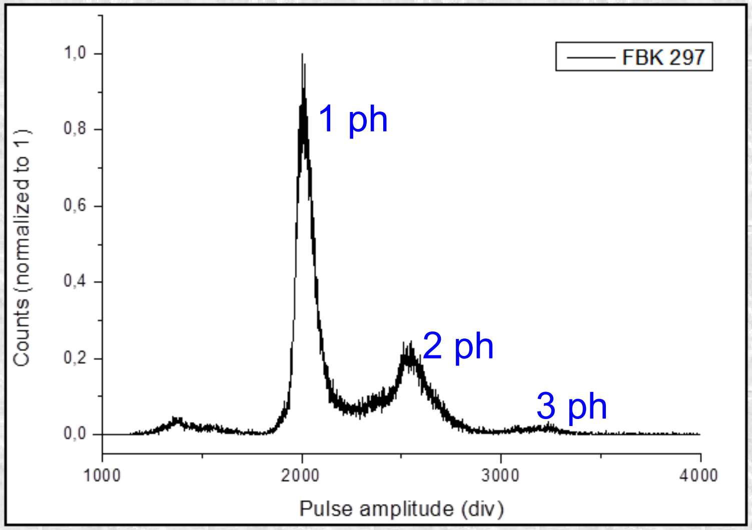


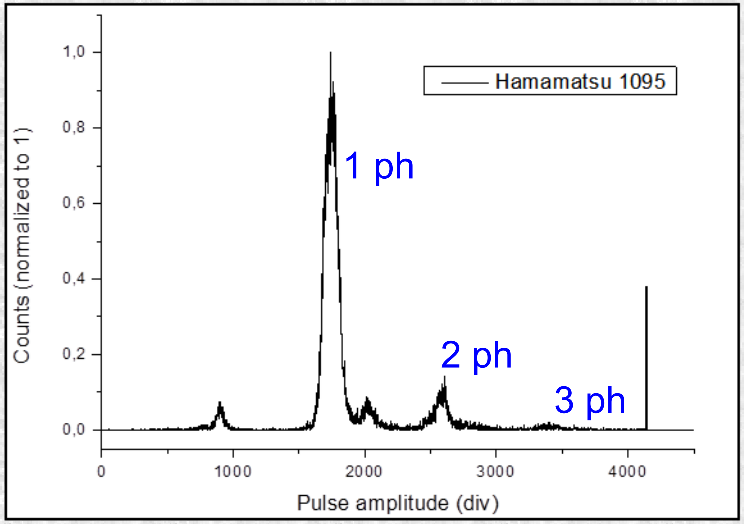


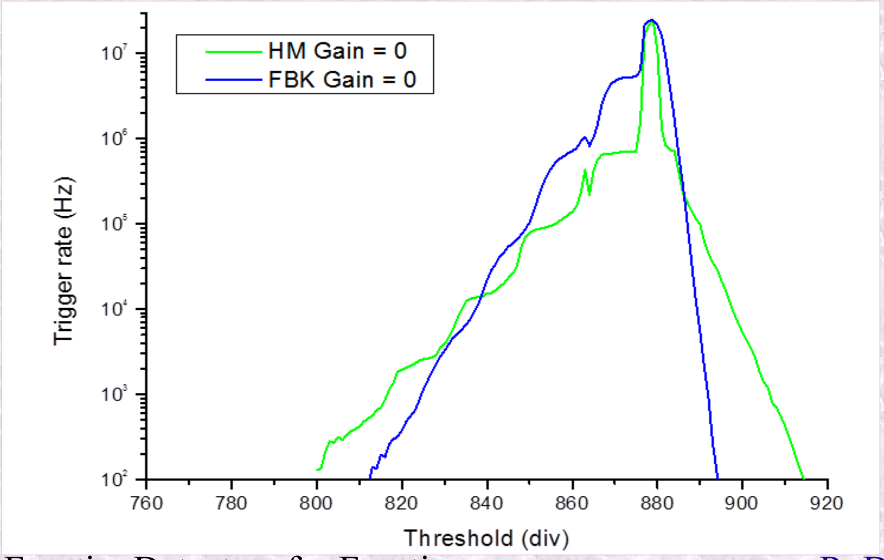
Backup: EASIROC with single SiPM

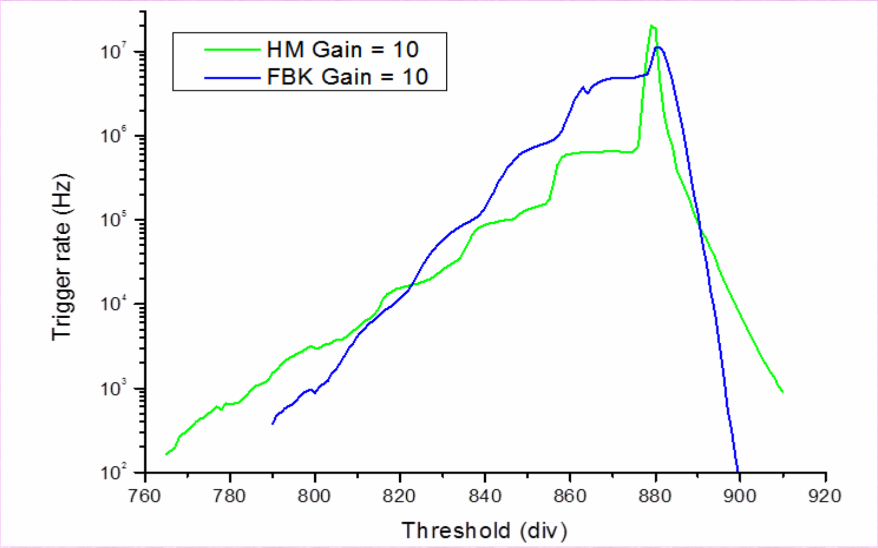
Pulse amplitude distribution for both devices measured with (EASIROC) probe connected to fast bipolar shaper. (Self trigger, threshold just above noise).

EASIROC trigger rate vs comparator threshold for two different Gains.





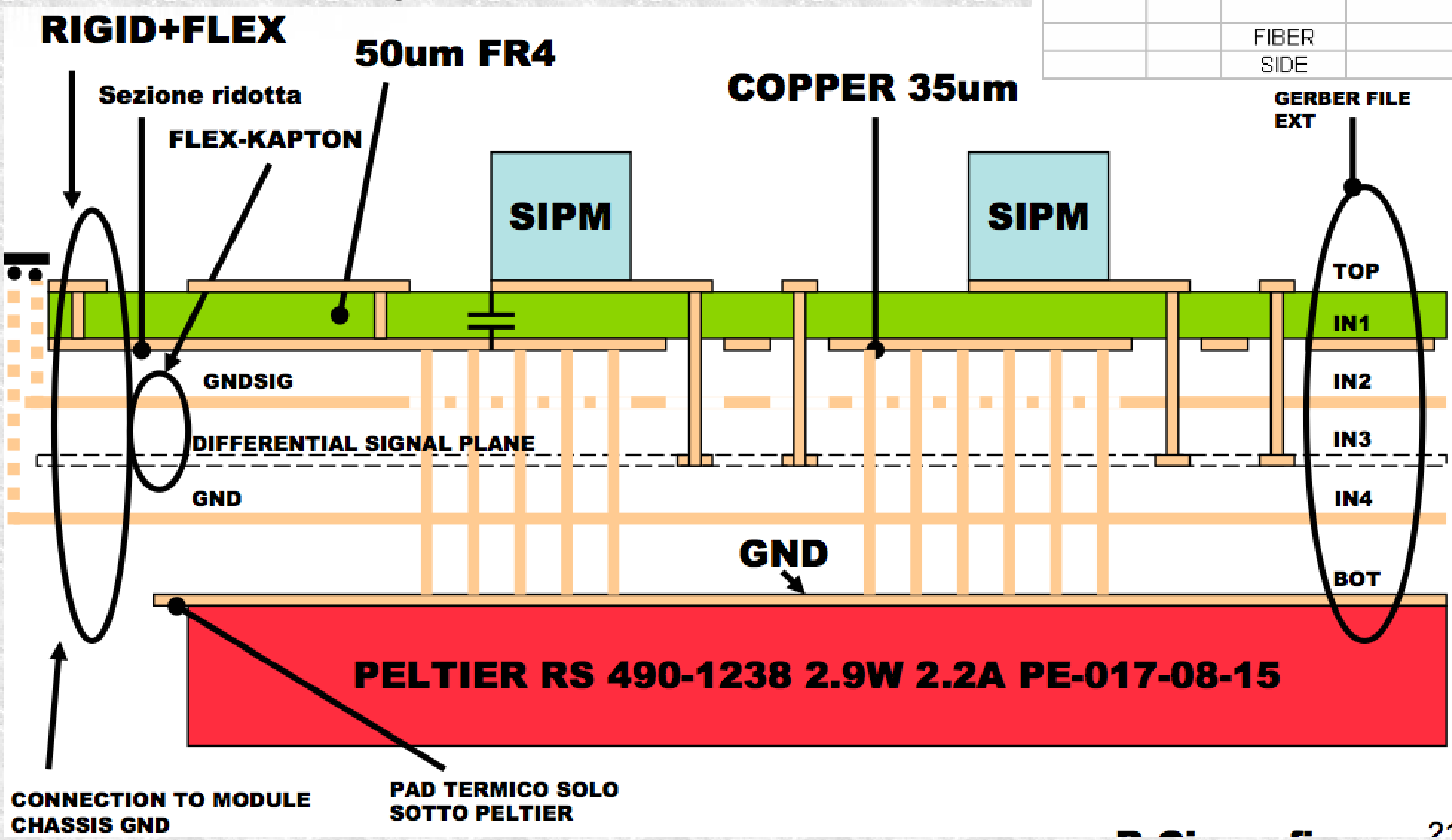




Backup: Hybrid Vertical Slice

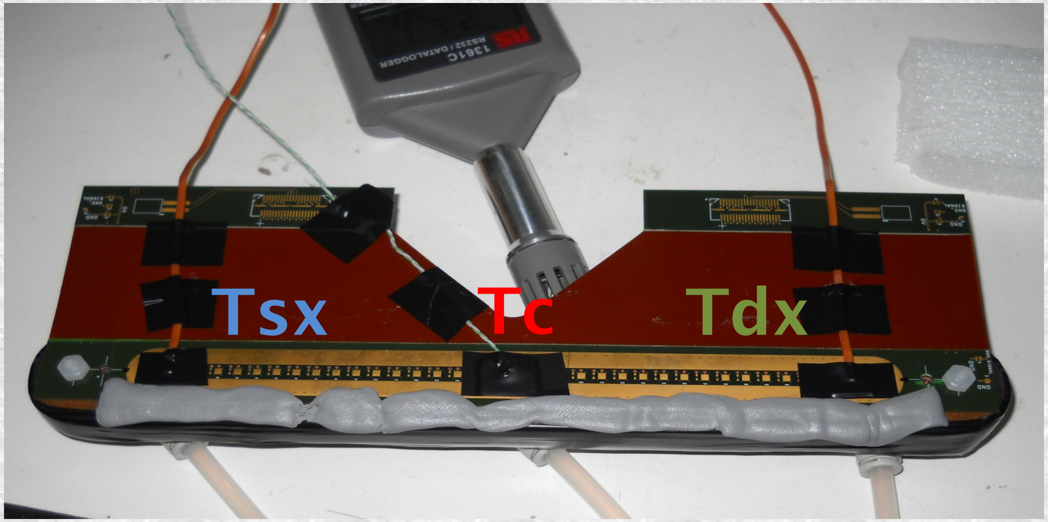
- GND planes
- Impedance controlled lines
- Thermal Vias
- Bondable gold finish.

		RIGID PCB 20 mm	FLEXIBLE KAPTON 40mm	RIGID PCB 15 mm
TOP	1	17+25		17+25
	FR4	100		100
IN1	2	35		35
	FR4	350		350
IN2	3	35	35	35
	kapton	100	100	50
IN3	4	35	35	35
	FR4	350		350
IN4	5	35		35
	FR4	100		100
BOT	6	17+25		17+25
		FIBER SIDE		CONNECTOR SIDE

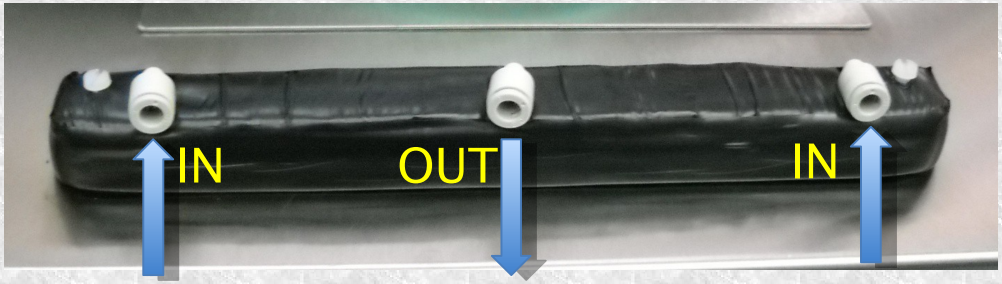


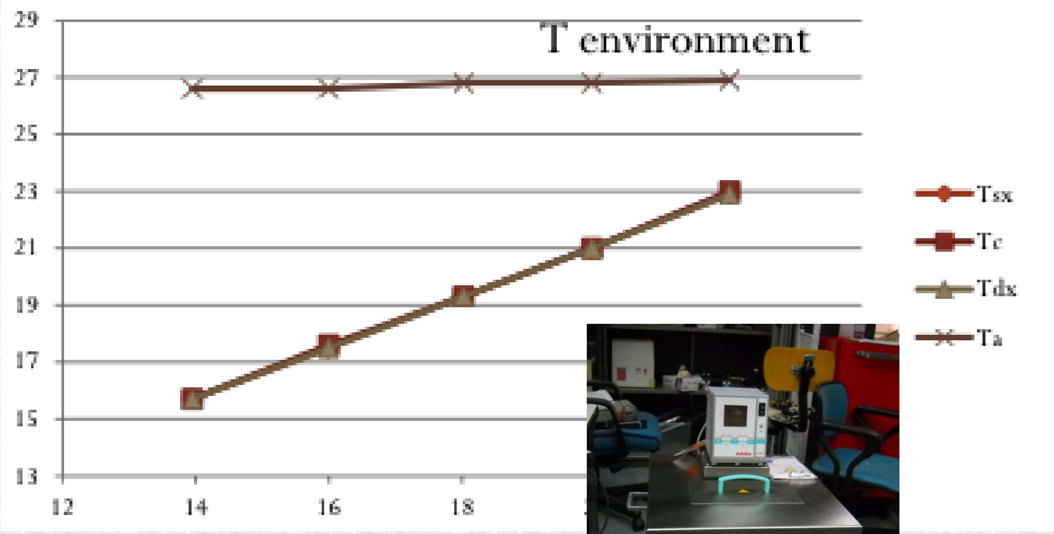
Backup: Cooling

- Hybrid optimized for cooling (Peltier based)
- For the moment a heat exchanger with a closed circuit with a chiller is used.
- Temperature differences below instrument accuracy: 0.1 °C

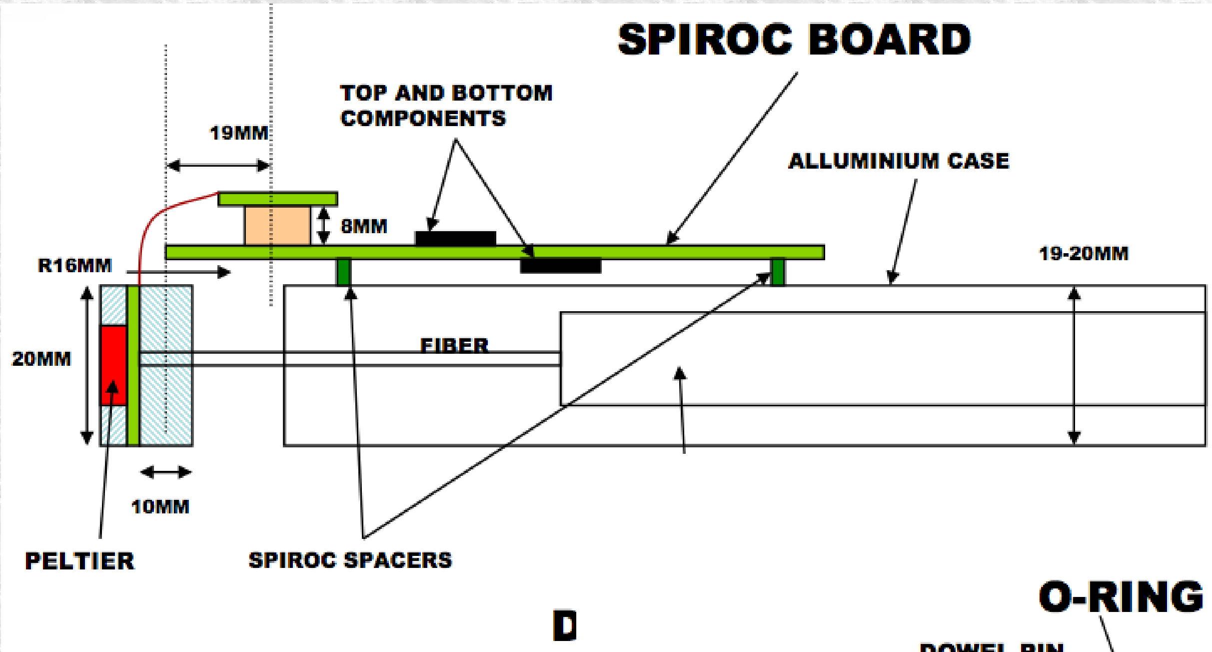


Thermal exchanger

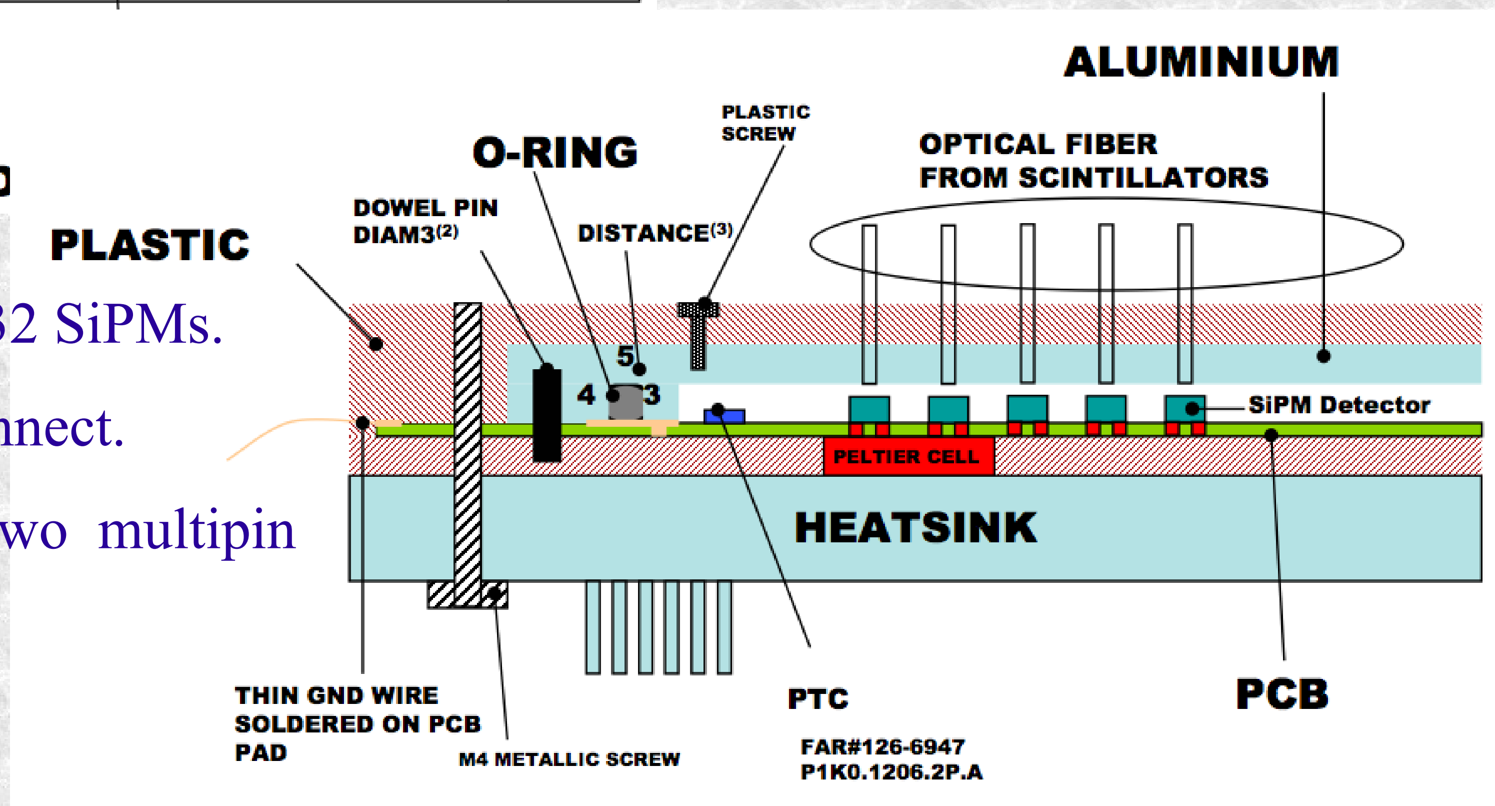




Backup: Hybrid Placement



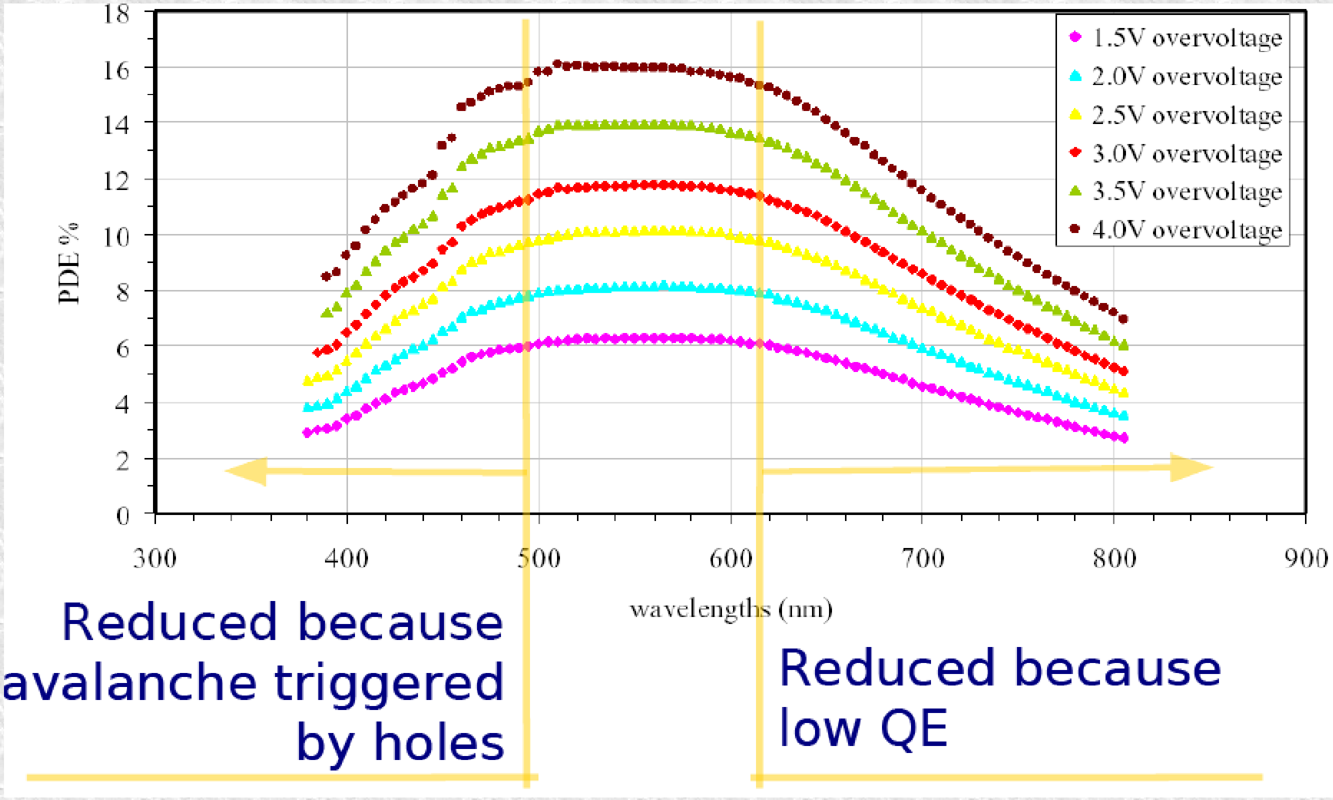
- Light and air tightness.
- Peltier cooling.
- Precision assembly (less than 50 µm.



- Rigid PCB holding 32 SiPMs.
- Kapton Flex interconnect.
- Rigid PCB holding two multipin connectors.

Backup: IRST PDE

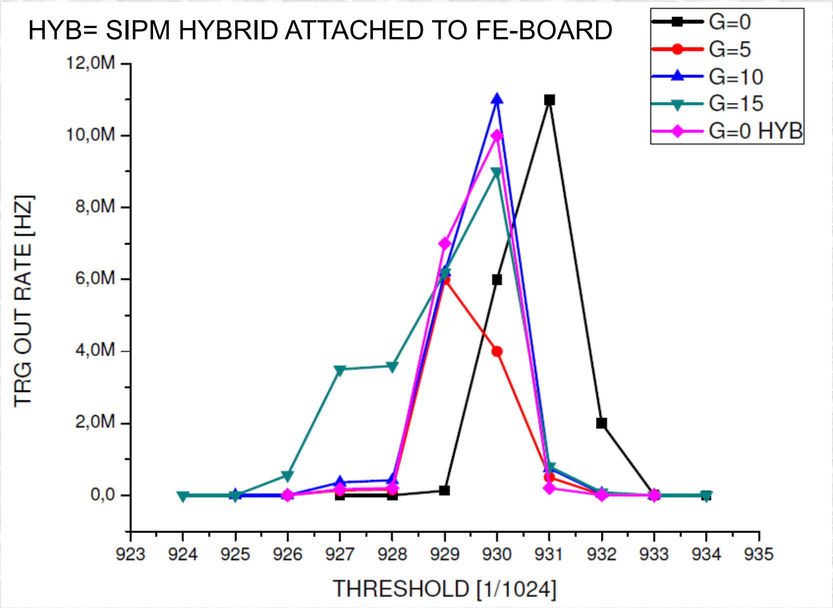
- IRST Data
- Careful with Dark Count Rate

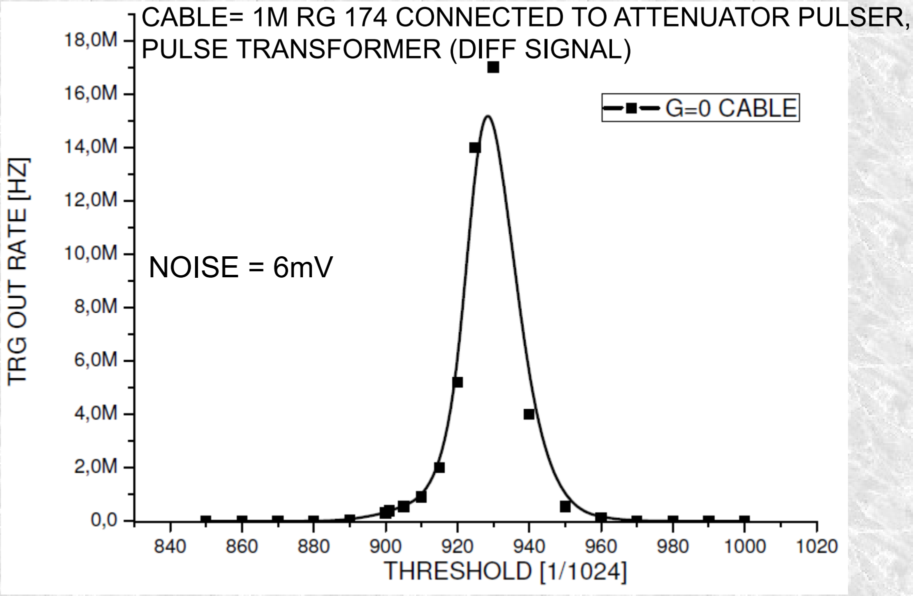


Backup: EASIROC noise on the comparator channel

MEASUREMENT OF TRIGGER OUT RATE vs INTERNAL COMPARATOR THRESHOLD WITH TREE DIFFERENT FRONT-END SIGNAL COUPLINGS

Each bin in threshold correspond to 1.1 mV (Settings in High Gain PRE)





NOISE = 0.65 mV FOR GAIN = 0,5,10
NOISE 1.1 mV FOR GAIN = 15