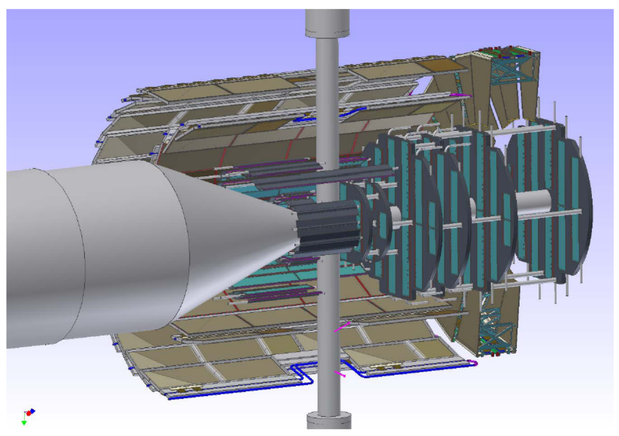
The Pixel Detector Readout ASIC for the Micro Vertex Detector of the PANDA Experiment

Abstract *:* The PANDA experiment at the future FAIR facility under construction near the GSI research center at Darmstadt, Germany, aims to the study of the antiproton-proton and antiproton-nucleus annihilation reactions. The Micro Vertex Detector (MVD) is the innermost part of the experiment and will consist of silicon pixel and silicon strip detectors. Owing to the high track density (up to 11.4 MHz/cm^2) and the absence of an hardware trigger signal, an ASIC based custom solution for the electronic readout of the pixel detector has been chosen. The ASIC, named ToPiX, will provide the time position of each hit and a measure of the charge released with the Time over Threshold (ToT) technique. A reduced scale prototype in a CMOS 0.13 µm technology has been designed and tested. The prototype includes four columns made of 128 pixel cells, four columns of 32 cells and and the end of column readout with a 32 cells deep FIFO for each double column. Each cell embeds a charge amplifier with constant current feedback capacitor discharge, a comparator with per cell adjustable threshold, 12-bits leading and trailing edge register for time and ToT measurement and an 8 bits bit configuration register. All the readout logic has been SEU-hardened by design using either Hamming encoding or triple redundancy. The chip has been tested both electrically via a test pulse input and connected to a detector in a beam test. Radiation test for both TID and SEU tests have been performed.

PANDA Micro Vertex Detector layout



- Barrel

  Layer 1 : radius 28 mm, SPDs
  Layer 2 : radius 53 mm, SPDs
  Layer 3 : radius 92 mm, SSDs
  Layer 4 : radius 120 mm, SSDs

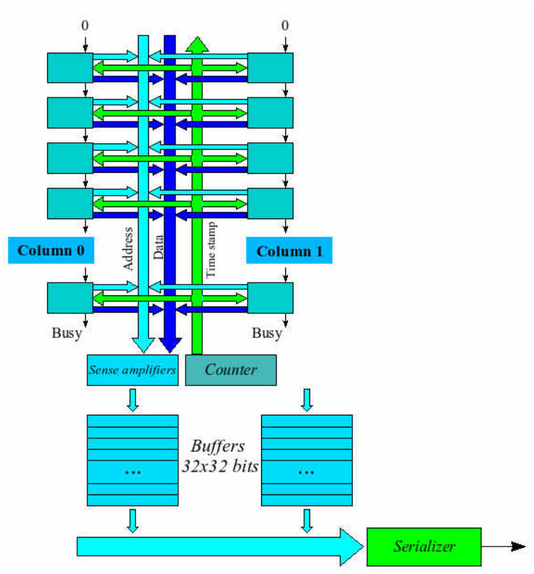
- Forward

  Disks 1-2 : radius 37.5 mm, SPDs
  Disks 3-4 : radius 75 mm, SPDs
  Disks 5-6 : radius 130 mm, SPDs + SSDs

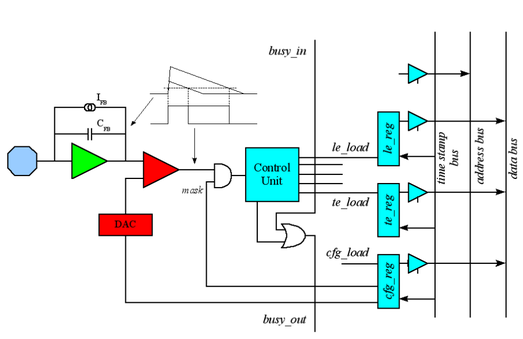
Pixel requirements

Pixel size	100 × 100 µm^2	Clock frequency	155.52 MHz
Chip active area	11.4 × 11.6 mm^2 (116 rows, 110 columns)	Time resolution	6.45 ns (1.9 ns r.m.s.)
dE/dx measurement	ToT, 12 bits dynamic range	Power consumption	< 750 mW/cm^2
Maximum input charge	50 fC	Maximum event rate	15.1×10^6 events/s
Noise floor	< 32 aC (< 200e$^-$)	Total ionizing dose	< 100 kGy

Readout architecture



Pixel cell schematic

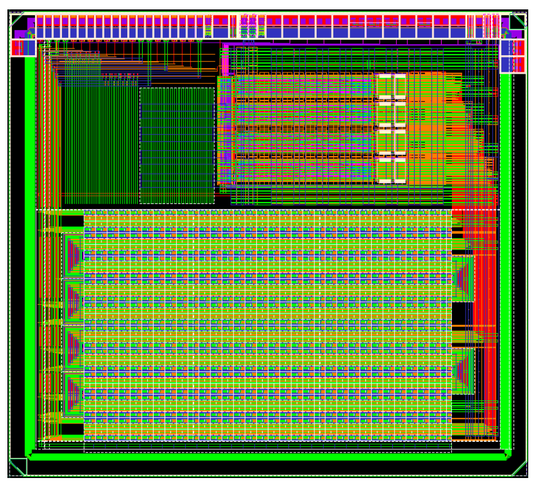


No trigger → data is sent out continuously

A counter provides absolute time info to all pixels and is also used for ToT

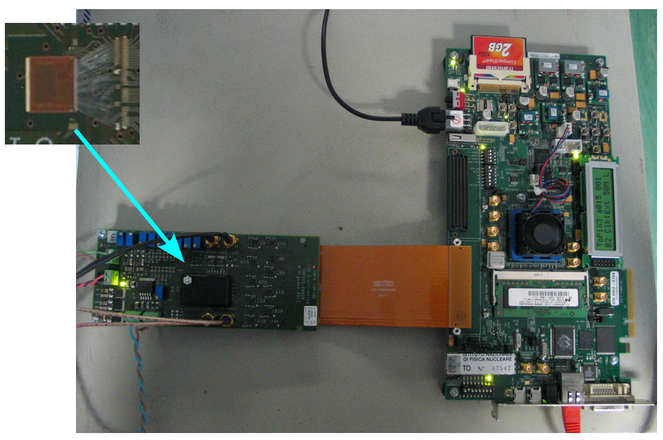
3×312.5 Mb/s SLVS serial links

ToPiX v3



- ➔ Die size : 4.5 × 4 mm^2
- ➔ Technology : CMOS 0.13 µm
- ➔ Single 1.2 V power supply
- ➔ Bump bonding pads
- ➔ 2 × 2 × 128 cells columns
- ➔ 2 × 2 × 32 cells columns
- ➔ 32 cells EoC FIFO
- ➔ SEU protected logic via TMR (pixel cell) or Hamming encoding (EoC)
- ➔ Serial data output
- ➔ SLVS I/O

Test setup



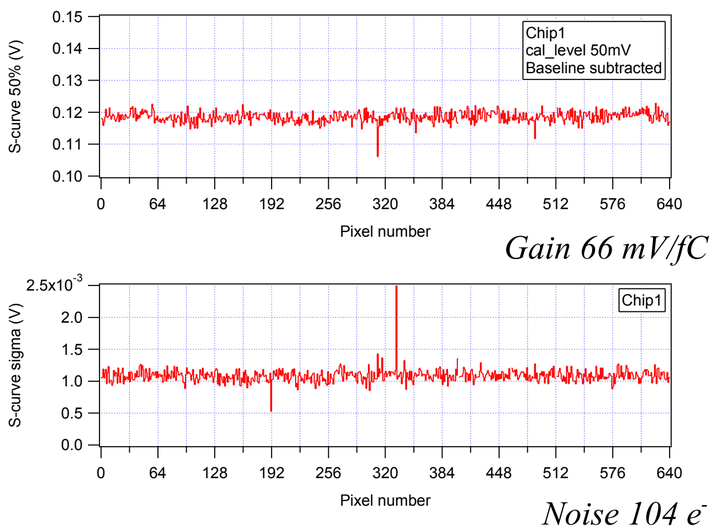
Based on Xilinx Virtex-6 ML605 Evaluation Kit

Remote control via TCP/IP. Up to 4 boards controlled in parallel by a single PC.

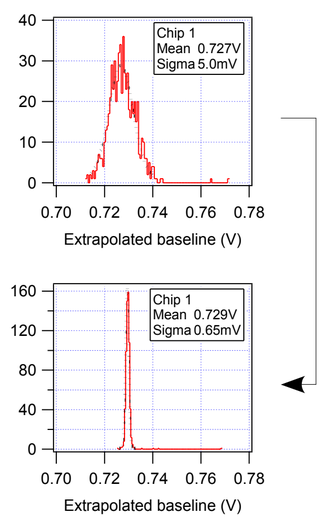
Limited number of external interconnections → *very flexible*

Already used in a beam test at COSY (Juelich) → *see D.Calvo presentation on Monday afternoon*

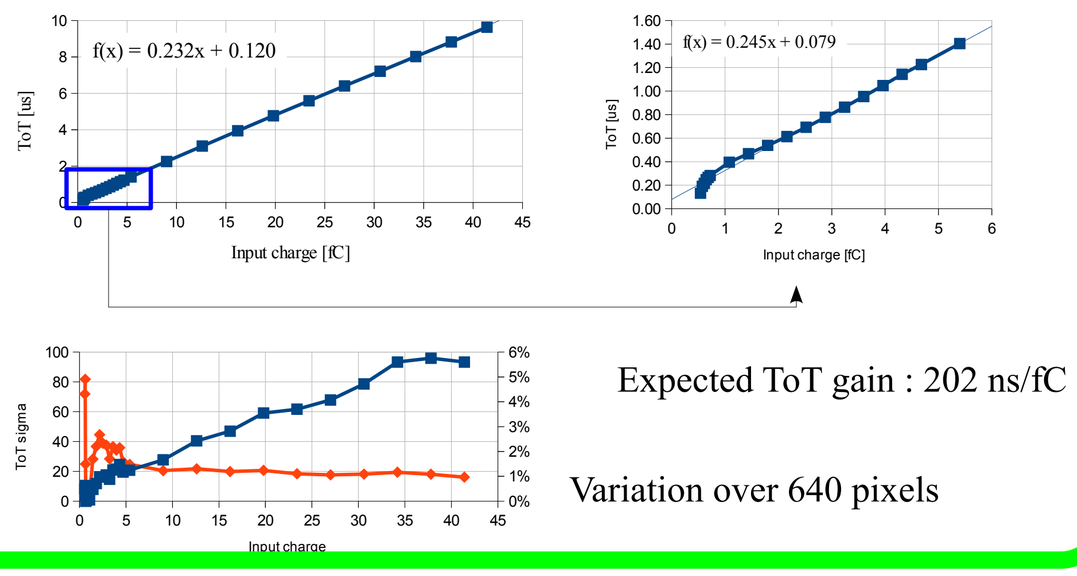
Analogue gain & noise



Baseline correction



ToT gain and linearity

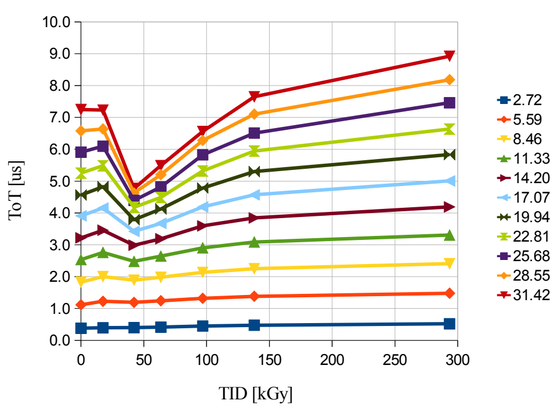


Expected ToT gain : 202 ns/fC

Variation over 640 pixels

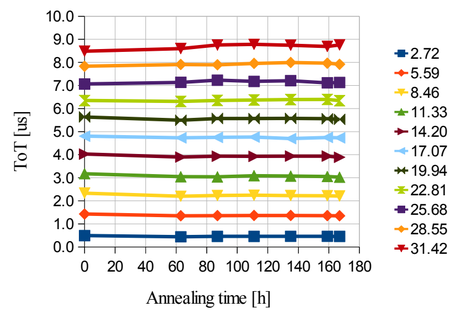
TID tests

During irradiation



DR compression due to leakage current in the clipping circuit → *to be fixed*

Annealing @ 80 ºC



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