ARAMIS

Advanced Real-time Architectures of Data Processing, Pattern Recognition and Data Transmission for Frontier Applications in High Energy Physics, High Reliability Systems and Visual Science

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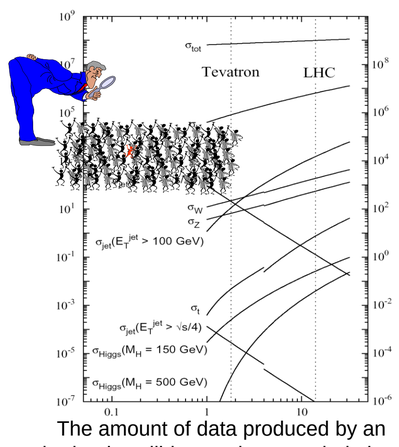
The goal of the ARAMIS project consists in the development of real-time architectures for event analysis in High Energy Physics. The complexity of the problems suggests to consider complementary approaches: Serial Link Processors (SLP), fast custom hardware, high performance computing platforms based on Graphical Processing Units (GPU). The solutions can be adopted by different HEP detectors: ATLAS, CMS, LHCb and the future Cabibbo-lab Super-B experiments. The project includes the participation of experts in Psycho-Physiology of Perception with the goal of exporting the real-time filtering and processing mechanisms adopted by the human brain in vision to the events-of-interest analysis, bringing new concepts and ideas from other fields to the HEP paradigms.

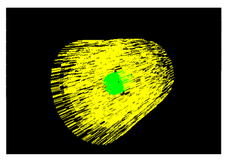
Trigger at hadron colliders

The needle in the haystack



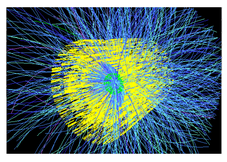
The amount of data produced by an hadronic collider can be overwhelming. The capability of the trigger in discriminating the interesting events is crucial for the success of an experiment

The Hits



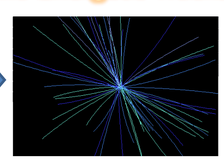
The typical silicon tracker or the same event produces a huge amount of data that has to be analyzed fast

The Tracks

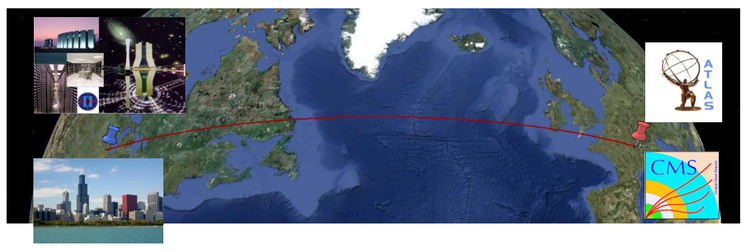


Reconstruct all the tracks in the events is challenging

The Energetic Tracks

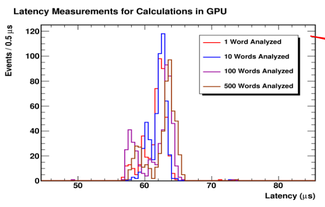


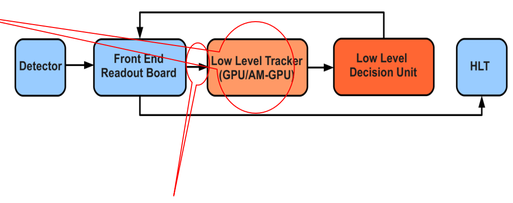
A real-time tracking system can select high-p_T tracks helping in the identification of the event topology

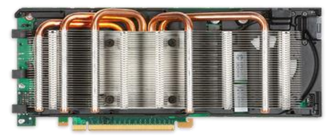


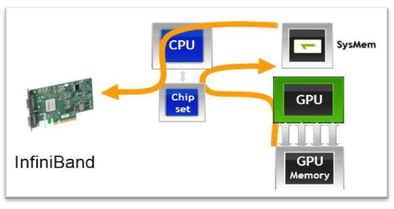
GPUs for real-time event selections

GPUs suited for parallel task as track reconstruction in online selections**. 500 tracks fitted in 60 ms** on the NVIDIA GTX285 @ CDF trigger test-stand. Processing time *dominated by GPU-CPU data transfer:* GPUDirect to eliminate CPU overhead.





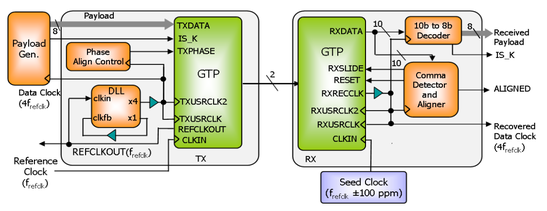




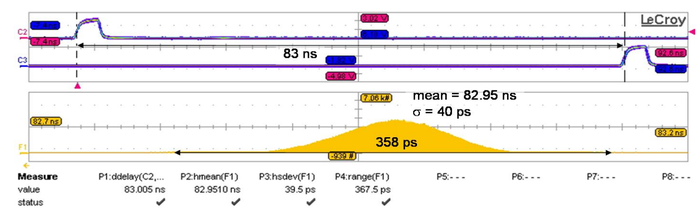
Fast data **transmission** between readout boards and GPU trigger units: ***Mellanox Infiniband technology***.

High Reliability Serial Links

The development of high-performance serial links with distinct real-time characteristics constitutes a basic element for the construction of the SLP and more in general for the synchronization of the entire event selection pipeline.



Serial link up to 2.5 Gb/s with minimum and fixed latency, based on FPGA Xilinx Virtex 5



Histogram of the latency of the link. Topmost trace: transmitted payload bit. second trace: corresponding received bit. Down: histogram of the latency.

Protocols and line encoding

The study of an optimal or near-optimal encoding of data is one of the key points of this line. Solutions based on self-synchronizing scramblers that can offer the best use of the bandwidth will be evaluated.

Analysis of embedded serializers in new generation FPGA

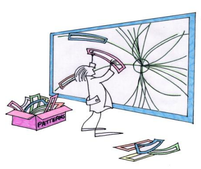
For real-time applications an original configuration of the FPGA-immersed serializers must be developed allowing their use at fixed and minimum latency. This requires a detailed study of the the serial stream's alignment mechanism and the design of a circuit external to the serializer, but residing on the FPGA, that can hook on the stream with a fixed and predictable phase. The most innovative devices on the market compatible with the requirements for real-time running and reliability will be evaluated.

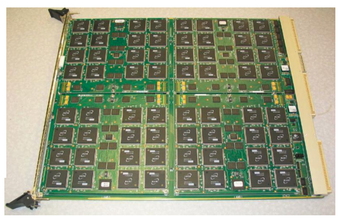
Fault tolerance links

FPGAs offer a powerful, flexible and economical platform, yet their use in areas subject to radiation requires the development of particular error moderation and fault-tolerance techniques. FPGAs compatible with the design specifications will be tested on a 62 MeV proton beam and on heavy ion beams at the INFN Laboratori Nazionali del Sud, in Catania. The Single Event Errors (SEEs) rate will be measured, as well as the cross section in a reference serial link project. The cross section of the configuration memory bits will be measured separately. The tests will allow a thorough examination of the SEU moderation algorithm performances

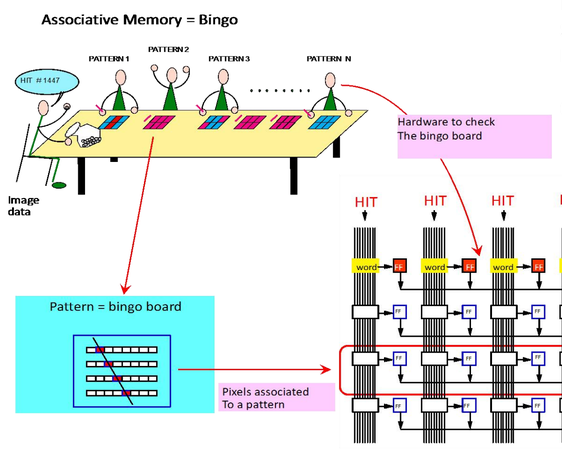
Serial Link Processors

The core of the SLP there is composed by the associative memory technology. It allows a parallel approach in the pattern matching stage, using a massive bank of pre-calculated trajectories.
The approach is effective and flexible: it was a key features of the SVT system of the CDF detector, is going to be installed at ATLAS within the FTK processor, moreover the use of the same technology is under investigation in both ATLAS and CMS for the Level 1 trigger.

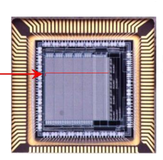




In the AM board up to 128 chip can be installed, such high density gives the possibility to store millions of patterns.
High speed serial links distribute the incoming data and send the information of the found roads.

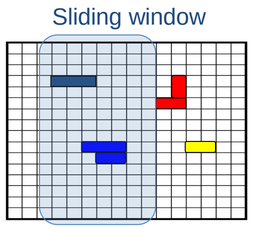


The single AM chip is a CAM-like memory with parallel match lines. This design is well suited for the typical data flow produced by HEP detectors. The last version uses a full custom VLSI design in a 65 nm architecture, with about 80K patterns per chip.



Online Clustering

FPGA clustering algorithm

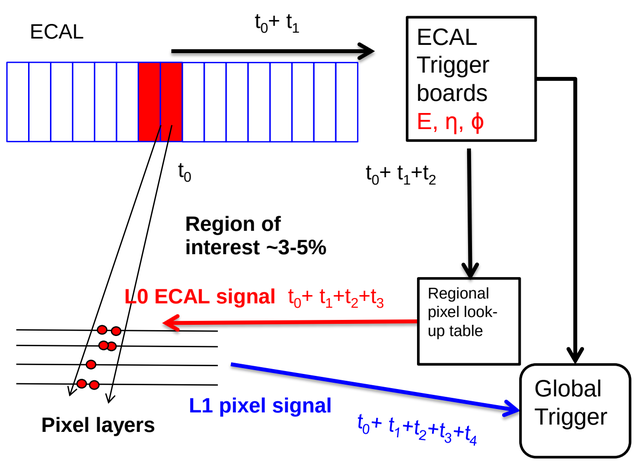


We propose the development, the construction and test of an innovative algorithm for clustering of data from modern pixel detector. This algorithm should be implemented with FPGA chips. This algorithm will be integrated on a clustering mezzanine that will be the input gate to the SLP. It will receive silicon data over S-Link fibers. The key feature is a processing time that scales linearly with the amount of data to be processed. This means that clustering can be performed in pipeline with the readout, without suffering from combinatorial delays due to looping multiple times through all the data.

This feature makes this algorithm especially well suited for problems where the data has high density, e.g. in the case of tracking devices working under high-luminosity condition such as those of LHC or Super-LHC. In order to achieve this goal, the algorithm maps in the FPGA logic a part of the pixel module area.
Clusters in this area are found using local logic. The area mapped in the FPGA virtually slides through the pixel module to process all its data.

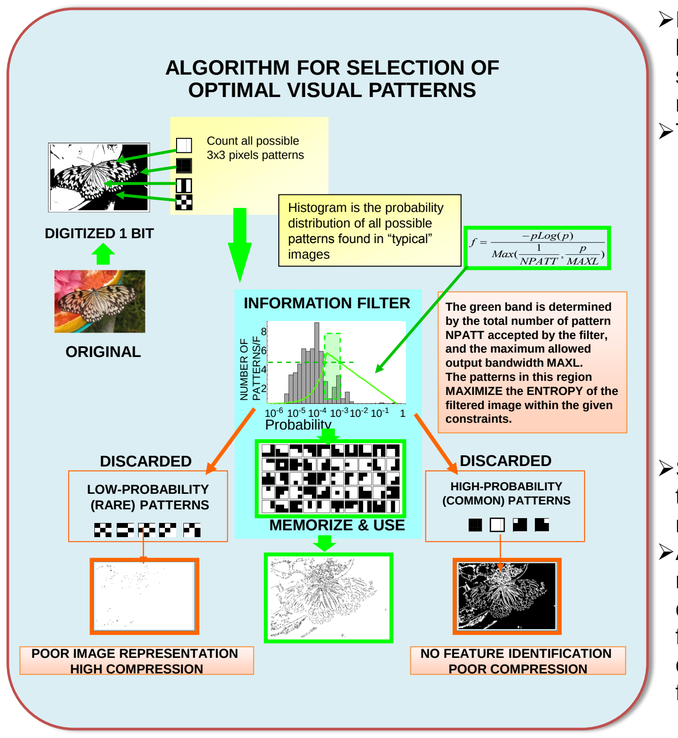
"Intelligent detector": clustering on FE chips

The high number of pileup events per bunch crossing will impact in many ways the performance of the Level-1 (L1) triggers. The extremely granular information of the pixel detector could locate signals from tracks originating from the same primary vertex.
Increasing the miniaturization of the technology opens up the possibility to organize the readout region into larger groups of pixels, thus providing clusters at L1 after a L0 ECAL trigger accept. These could be used to determine the primary vertices or linked to muons/electrons/tau-jets at L1, thus enhancing the trigger selectivity. We will address the feasibility study of on-chip cluster pattern recognition for a Level-1 pixel based trigger, thanks to the VDSM technologies (such as the 65 nm)



Visual Science

The visual system faces the problem of extracting biologically-relevant information from a large flux of input data. A strong compression of information must happen in the early stages of processing. This model (Punzi & Del Viva 2006) is based on a pattern-filtering architecture, partly **inspired by high-speed digital data reduction in experimental high-energy physics** (Ristori & Punzi, 2010; Dell'Orso & Ristori, 1989).The assumption of this model is that the early stages of the visual system act as a filter that selects only a limited number of visual patterns (or features) for further processing, based on the principle of maximal information transmission under real-world limitations. The model, applied to black and white images, predicts "a priori" from very general principles a structure of visual filters that closely resemble well-known receptive fields (Hubel & Wiesel, 1962) and identifies salient features (edges, lines) providing highly compressed "primal sketches" (Marr 1976) of visual scenes (Del Viva & Punzi,2008). Human subject are able to identify such sketches (2AFC procedure) in rapid identification tasks (10-20 ms) with very high accuracy (up to 90%), comparable to that for fully detailed original images (Del Viva et al. , 2010).



- Extend research to more realistic conditions containing a large amount of information, that must be subjected to strong compression: **multiple luminance levels, color, motion and object recognition**.
- To do so we will
  1. extract optimal features according to the model in each modality **with extensive computational simulation** on real-world images and movies. Given the high computational load these simulations will be implemented on **dedicated hardware;**
  2. measure **with psychophysical techniques** the visibility by human observers of the features selected by our model, comparing them with features selected according to other criteria, to prove the correctness of the simulation in reproducing the performance of human observers.
- Study the feasibility of an **hardware implementation** of the process of extraction of visual salient features from natural sequences of images based on AM or GPUs.
- Apply algorithm and software developed for vision to the reconstruction of clusters in tracking detectors corresponding to track hits. The goal is to determine the feasibility of implementing an adaptive hardware based cluster-finder, that can learn automatically the local features of detectors and track their variation over time.