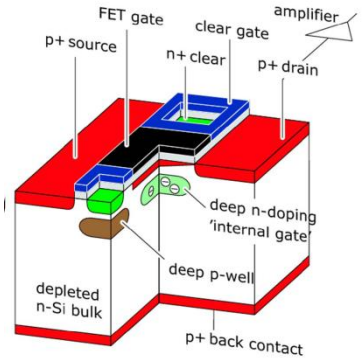
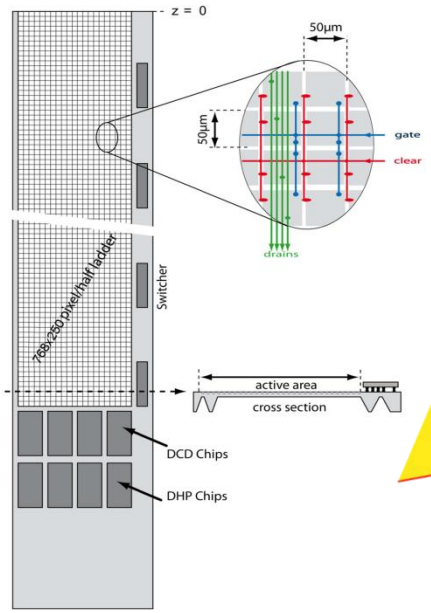
Ultra-thin fully depleted DEPFET active pixel sensors for future e+/e- collider

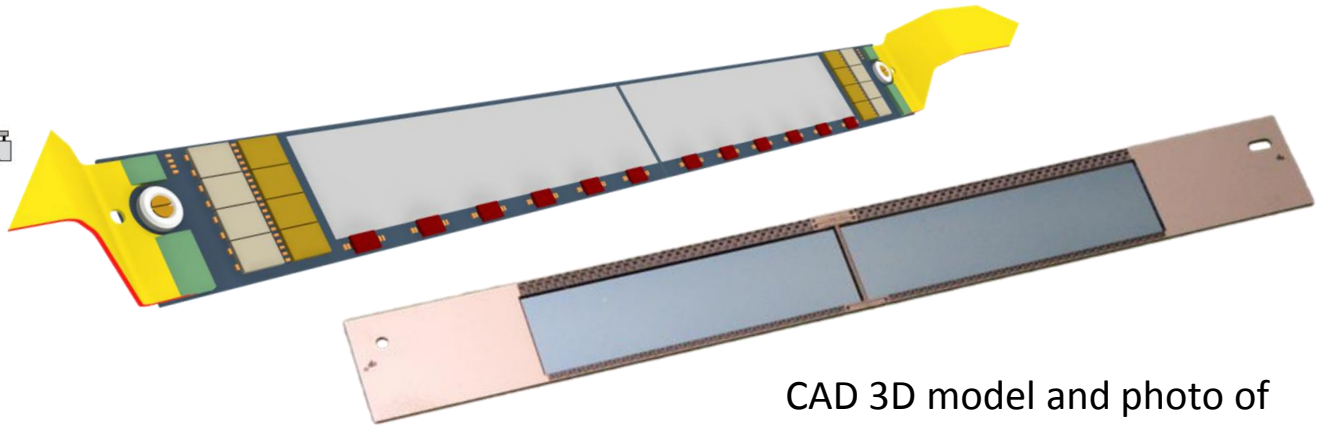
Christian Koffmane on behalf of DEPFET collaboration



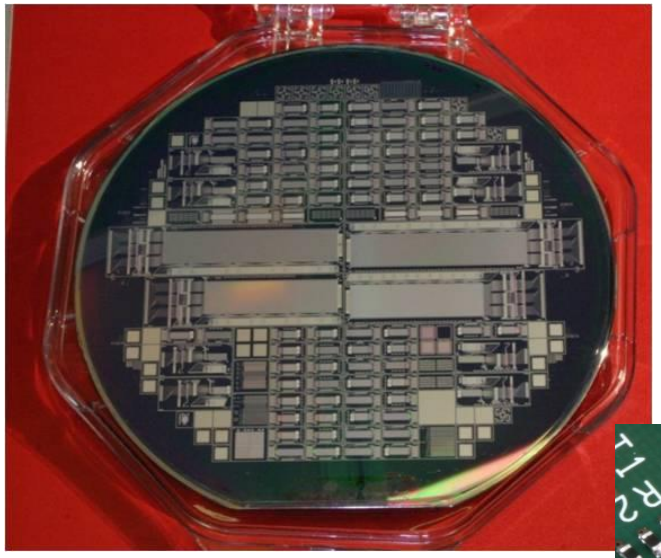
- DEPFET pixel combines the signal detection with the first amplification stage and therefore provides the necessary signal-to-noise ratio for very thin pixel detectors
- Silicon-on-isolator (SOI) wafers are used in the thinning process (the top wafer is already partly processed before the wafer bonding to the handling wafer)
- DEPFET pixels are arranged in an array and the control and readout ASICs (SwitcherB, DCDB and DHP) are bump bonded on a All-Silicon-Module

  → Half –ladder: integrated DEPFET pixels and assembled ASICs

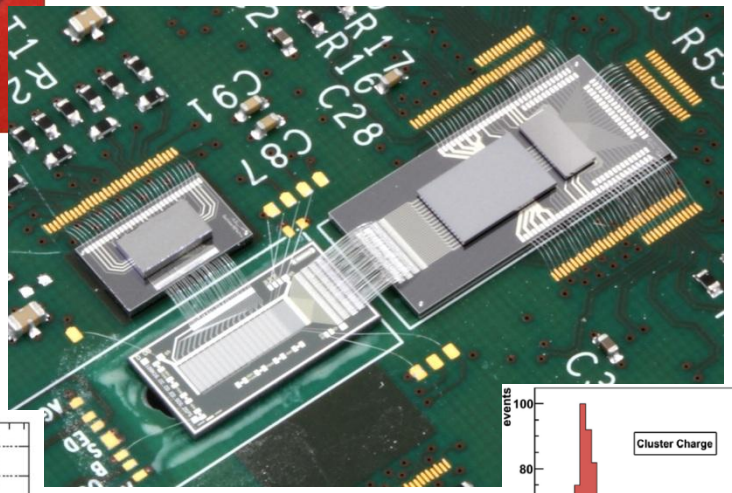




CAD 3D model and photo of two joined half ladders

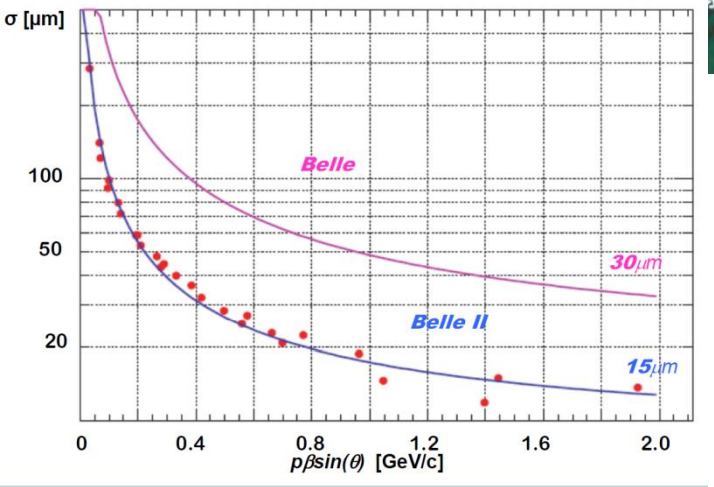


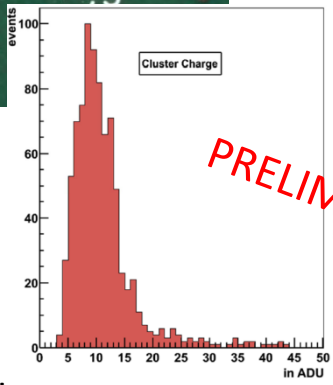
- 50micron thin DEPFET detectors have been produced with prototype designs for Belle II and ILC
- Hybrid Boards with the DEPFET matrices and control and read-out ASICs have been developed and studied in beam tests



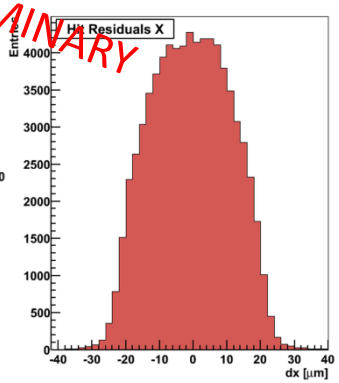
Latest results on beam test shown in poster by P. Kodys!

- MIP signal charge of a cluster of pixels
- Resolution in x direction (pixel size 50µm x 50µm)





PRELIMINARY



Expected improvement of the z vertex resolution of Belle II (SVD and PXD)