The electronics system of the TOTEM T1 telescope

M. Bozzo[1,2], F. Ferro[1], M. Lo Vetere[1,2], **S. Minutoli**[1], E. Robutti[1]

[1] I.N.F.N Genova, via Dodecaneso, 33 - 16146 GENOVA (Italy); [2] University of GENOVA (Italy)

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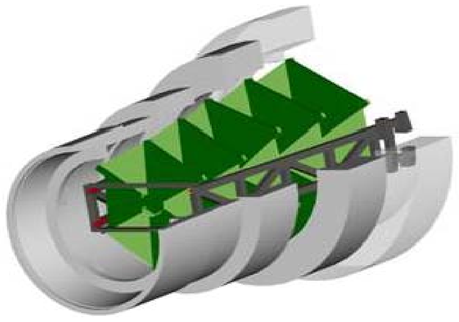
Abstract

The TOTEM experiment is devoted to the measurement of the proton-proton elastic and total cross section at LHC. It is composed of three detector using different technologies. The TOTEM detector that will measure the inelastic rate in the pseudo-rapidity region $3.1 \leq |\eta| \leq 4.7$, named T1, is made of Cathode Strip Chambers. Signals from about 11000 anodes and 16000 cathodes must be processed and optically transmitted to the counting room. The complete electronic readout chain of the Cathode Strip Chambers is presented here: the anode and cathode front-end boards, and the readout-control card. The electronics system has been developed keeping into account the hostile environment from the point of views of both radiation and magnetic field. Dedicated VLSI circuits have been extensively used in order to optimize space and power consumption.

The Detector



The T1 telescope, installed in two cone-shaped regions in the end-caps of CMS, delimited by the beam pipe and the inner envelope of the flux return yoke of the magnet, detects charged particles in the pseudo-rapidity range $3.1 \leq |\eta| \leq 4.7$.

Each telescope arm consists of five planes of CSC equally spaced in *z* at a distance between 7.5 m and 10.5 m from the interaction point. Each detector plane is composed of six trapezoidal CSC covering roughly a region of 60° in ϕ.

Each telescope arm is built in two vertically divided halves (half arms), in order to allow the installation and removal of T1 when the vacuum chamber is in place.

Electronic system architecture

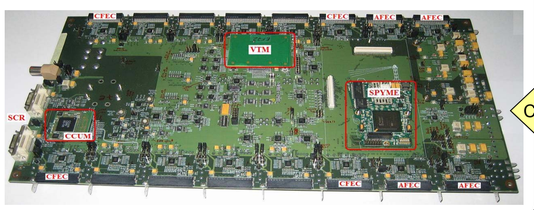
On Detector Region

The orientation of the cathode strips and of the anode wires provides three measured coordinates of the position of each hit in the CSC plane, useful to reduce the number of fake hits from random combinations ("ghosts") in case of multiple hits.
The CSC anode and cathode signals are collected by custom designed anode front-end cards (**AFEC**) and cathode front-end cards (**CFEC**), equipped with a custom ASIC called **VFAT** designed at CERN by the TOTEM collaboration.

Data Path / Control Path

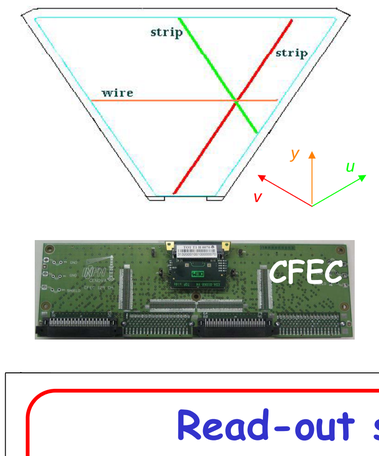
Local Detector Region

The serial digital data stream and the trigger bits coming from the AFEC and CFEC are collected by a custom designed Read-Out Card (**ROC**), where they are serialized and optically transmitted to the DAQ system by means of a dedicated CMS Gigabit Optical Hybrid (**GOH**). The configuration and monitoring of the system is performed using the I^2C standard protocol distributed through the optical CMS Slow Control Ring, based on the Digital Opto-Hybrid Mezzanine (**DOHM**) and the Communication and Control Unit Mezzanine (**CCUM**).



Control Path

CSC detector



The **AFEC** is the board that collects and groups signals from the anode wires of the CSC detector. Ten different types of AFECs have been adapted to the chamber shapes, for a total of 60 boards for the whole detector.
The **CFEC** board collects and groups the charge pulses induced in the CSC strips by the positive ions created by the crossing particle and moving towards the cathode. Each board processes 128 input signals.

Data Path / Control Path

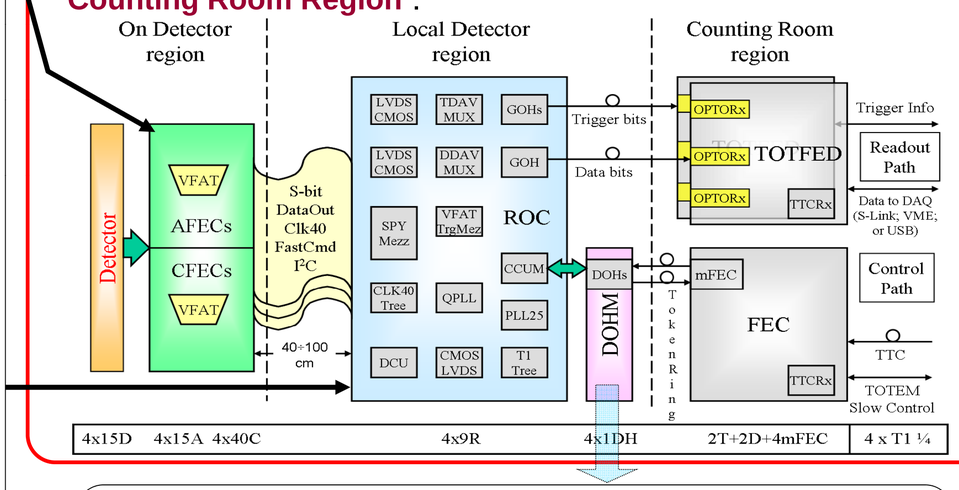
VFAT hybrid

The **VFAT** produces both "Hits" and "Trigger" information. The VFAT has 128 channel inputs.
Each channel contains a low noise pre-amplifier and shaper followed by a comparator. Following the comparator are the digital circuits used for generating the "Fast-OR" outputs, data storage and data packet construction.

Read-out system block diagram

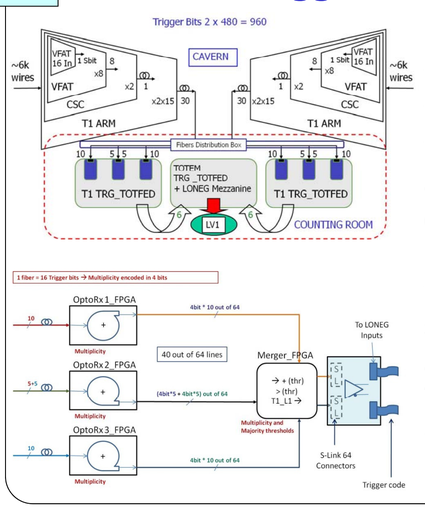
Trigger Path

Three logically and physically separated regions define the electronic system architecture. The "**On Detector Region**" where the Front-End ASICs are located, the "**Local Detector Region**" where the data are collected and optically transmitted to the "**Counting Room Region**".



Trigger architecture

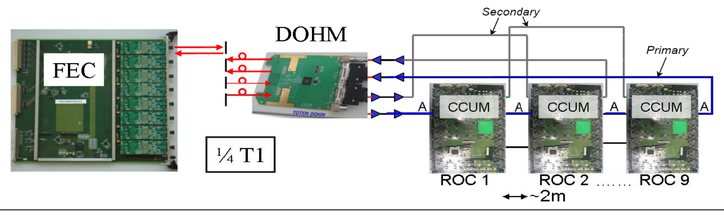
Trigger Path



Hit bits corresponding to triggered events are transmitted from the VFAT chip to ROC board. Here the hits are serialized by GOH and sent optically to the Front End Driver Boards (**TOTFED**) hosted in the CR. Hits multiplicity and sextants majority algorithms are implemented in FPGAs. Trigger primitives are sent to CMS via TOTEM Level One Generator (**LONEG**) board.

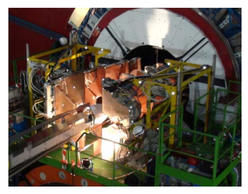
Slow Control Ring

The Slow Control Ring implements skip fault architecture for additional redundancy based on the doubling of signal paths and bypassing of interconnection lines between CCUM.

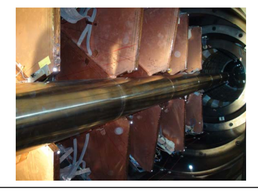


T1 installed inside CMS

The Genova team who designed and built the detector in front of the '+' arm of the telescope after final insertion.



The two half-arms under test on the installation platform, before insertion ('+' side).



Insertion test of one half-arm of T1 ('–' side).

Conclusions

The T1 detector was successfully installed into the end-caps of the CMS experiment over the 2010 winter technical stop – a delicate operation that required the CMS detector to be opened. The TOTEM T1 detector electronics system is fully integrated within the TOTEM DAQ and also fully compatible with CMS DAQ requirements. The completion with T1 allowed TOTEM experiment during 2011/12, to take precise measurements of the proton-proton interaction cross-sections, as well as detailed studies of elastic and diffractive pp scattering.