Timing performance of Timepix4, a large area four side buttable pixel detector readout chip

Riccardo Bolzonella, CERN, EP-ESE,
on behalf of Medipix4 collaboration

FATA2025 - Catania, 8th-10th October 2025

Overview

- Medipix4 collaboration and Timepix4 overview
- Timepix4 architecture and operating principle
  - pixels arrangement
  - Through-Silicon-Vias and Wire Bonds
  - acquisition modes
  - Time-of-Arrival (ToA) and Time-over-Threshold (ToT) measurements
- Measured performance in different applications
- Through-Silicon-Vias (TSV) assemblies status
- Future projects: the Picopix
- Conclusions

The Medipix4 collaboration

- **Timepix4 (2019)** [X. Llopart *et al* 2022 *JINST* **17** C01044]
  - 65nm technology
  - Pixel matrix of 512 x 448 pixels (55 x 55 μm^2)
  - Particle identification and tracking (Data-driven and zero suppressed)
  - 195 ps time binning
  - X-ray Imaging (full frame based with CRW sequential readout) with a single threshold and fine pitch mode only
- **Medipix4 (2022)** [V. Sriskaran *et al* 2024 *JINST* 19 P02024]
  - 130nm technology
  - Pixel matrix of 320 x 320 (75 x 75 μm^2) or 160 x 160 (150 x 150 μm^2)
  - Charge Summing architecture
  - Aimed at high rate spectroscopic imaging, optimized for high-Z material
- **Both chips have a 4-side buttable architecture:**
  - Periphery integrated inside the pixel matrix
  - **Prepared for readout using TSV (Through-Silicon-Vias)**
  - **Large active area ASICs**

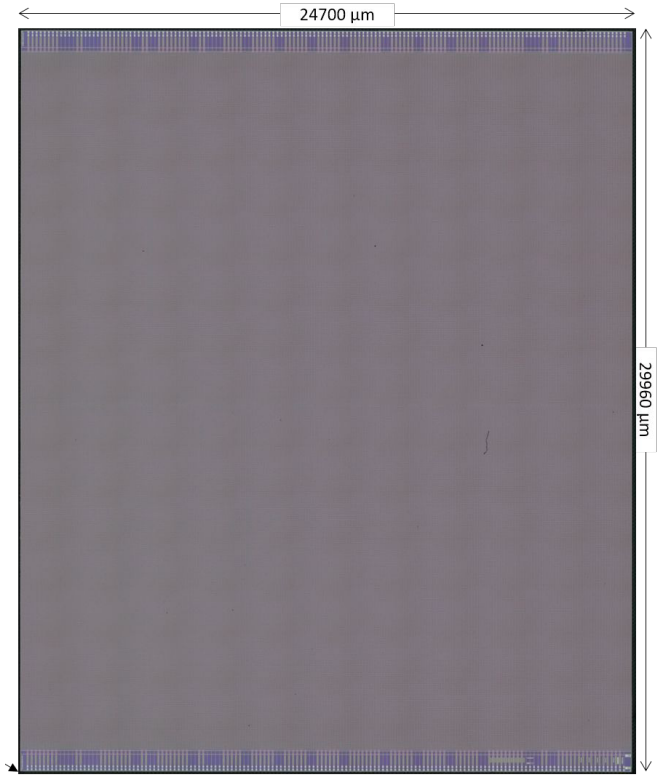
21 Medipix4 collaboration members

- CEA, Paris, France
- CERN, Geneva, Switzerland
- DESY, Hamburg, Germany
- Diamond Light Source, England, UK
- IEAP, Czech Technical University, Prague, Czech R.
- IFAE, Barcelona, Spain
- JINR, Dubna, Russian Federation
- NIKHEF, Amsterdam, The Netherlands
- University of California, Berkeley, USA
- University of Canterbury, Christchurch, New Zealand
- University of Geneva, Switzerland
- University of Glasgow, Scotland, UK
- University of Houston, USA
- University of Maastricht, The Netherlands
- University of Oxford, England, UK
- **INFN, Italy**
- LNLS, Brazil
- CSNS, China
- PNRI, Philippines
- University of Tennessee, USA
- Czech Academy of Science, Prague, Czech R.

- **Particle tracking:**
  - very high rate pixel telescope
  - sensor studies with < 100 ps timing resolution and ~10 μm spatial resolution
  - time-of-flight mass spectroscopy
  - radiation monitors
  - compton camera
  - gamma and neutron imaging
  - x-ray imaging
  - quantum applications (entangled photons measurements)
- **Frame-based imaging:**
  - x-ray imaging in synchrotrons with very high rates (> 10^9 particles/mm^2/s)

Timepix4 architecture and operating principle

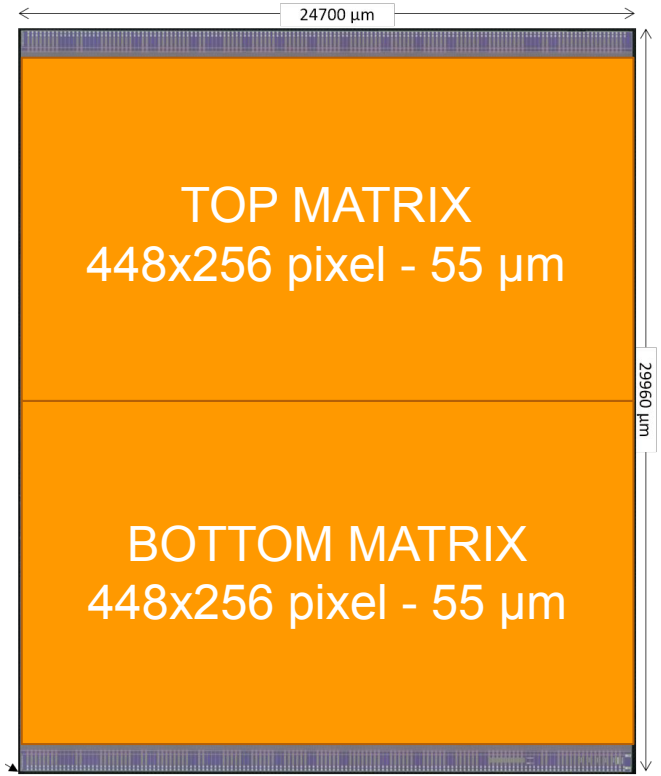
Timepix4 (multiple microscope pictures blended)



- 2 matrices: TOP and BOTTOM
  - 256 x 448 pixels each, 55 µm pitch

ASIC architecture

Timepix4 architecture
simplified schematic



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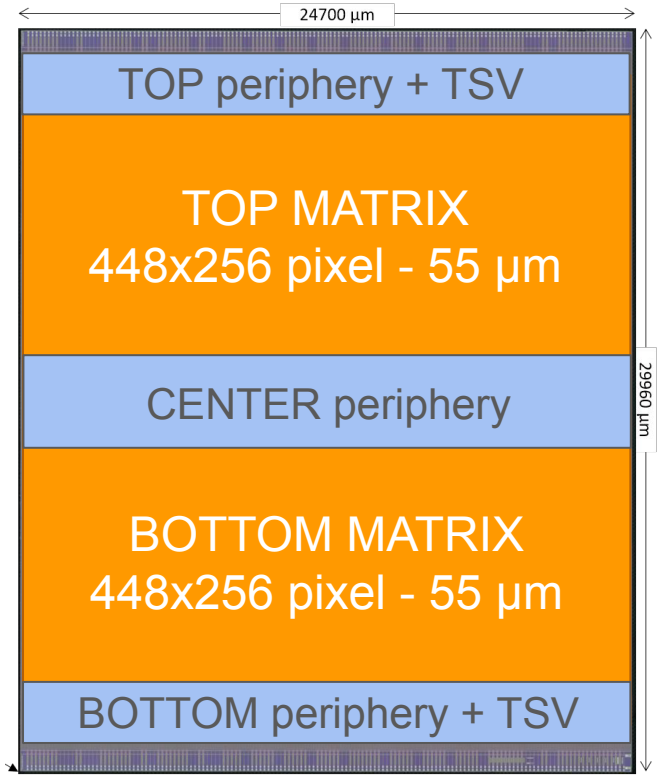

- 2 matrices: TOP and BOTTOM
  - 256 x 448 pixels each, 55 µm pitch
- 3 peripheries:
  - TOP and BOTTOM: data readout (16 x 10.24 Gbps serializers)
  - CENTER: analog blocks (global DACs and ADCs, …)

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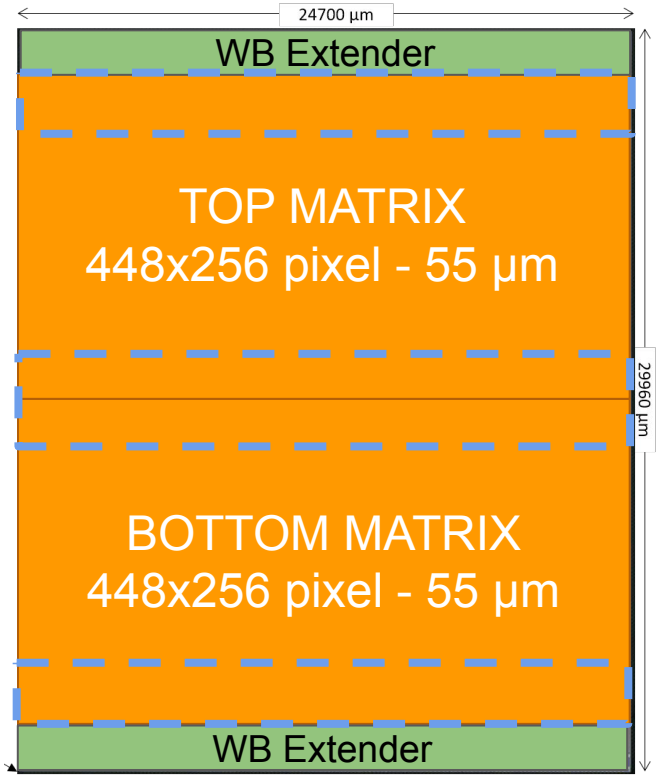

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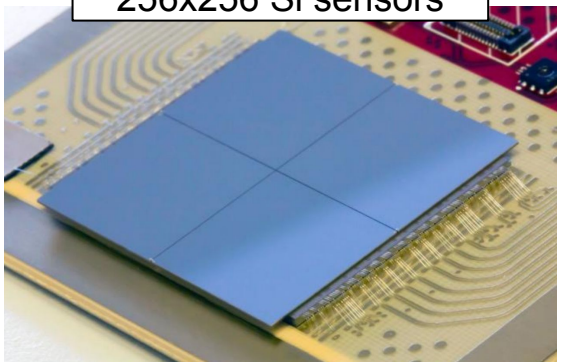
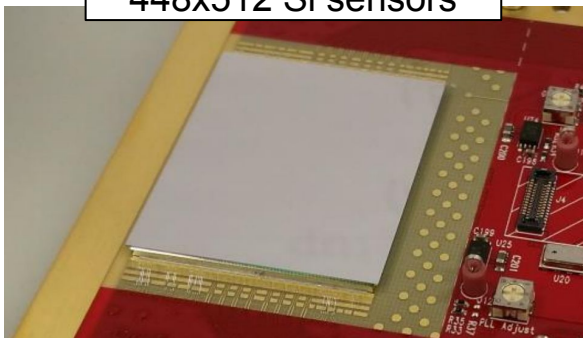
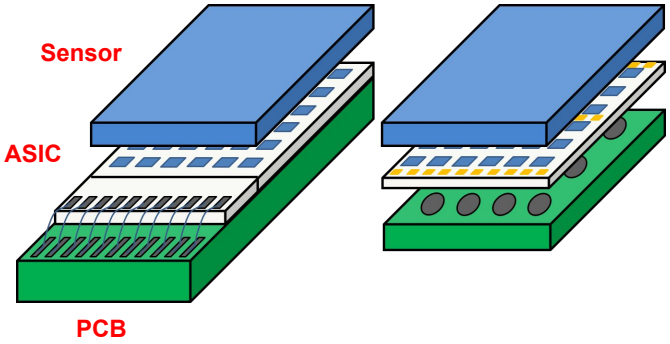
Timepix4 with 4 256x256 Si sensors

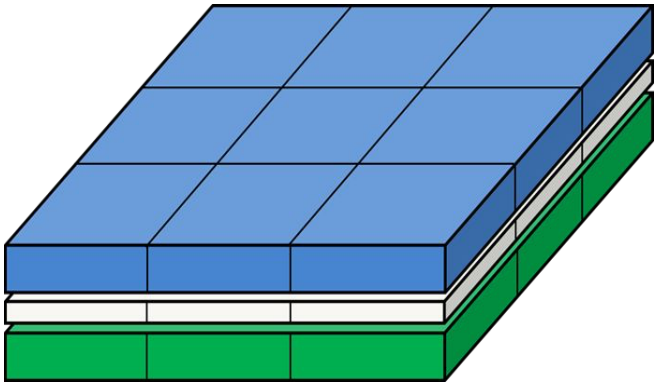


Timepix4 with a 448x512 Si sensors



ASIC architecture





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  - 4-side buttable
  - possibility to place several chips adjacent to cover larger detectors

ASIC architecture

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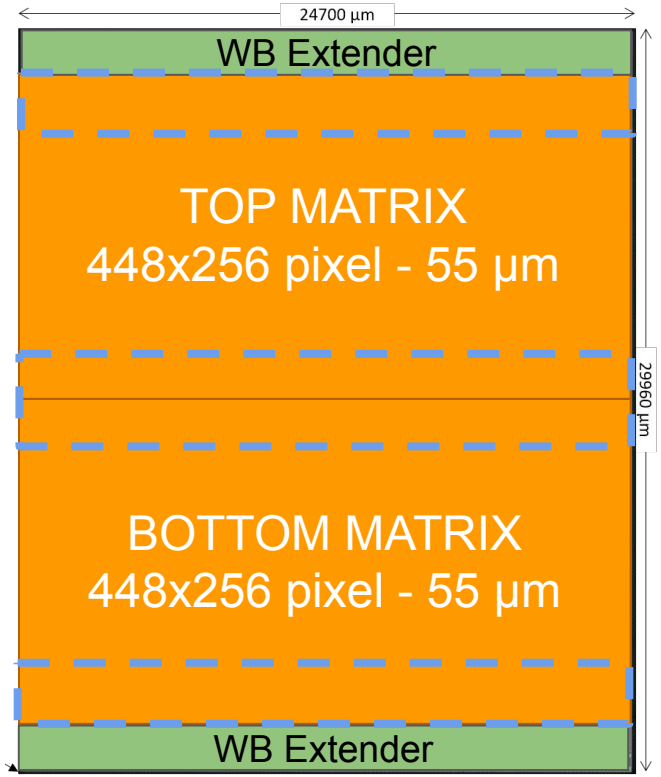

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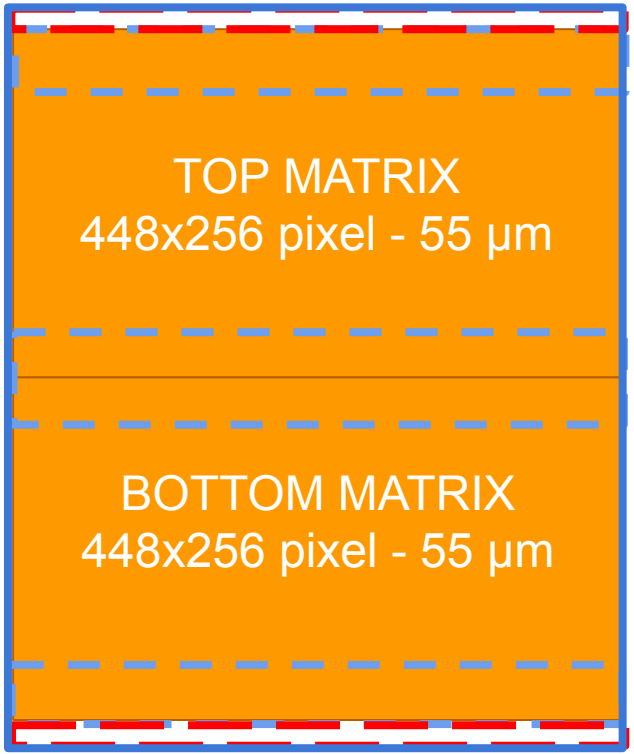
- Dicing options:
  - with wire bonds: ~93.7 % active area
  - with TSV: ~99.5 % active area

Timepix4 architecture simplified schematic



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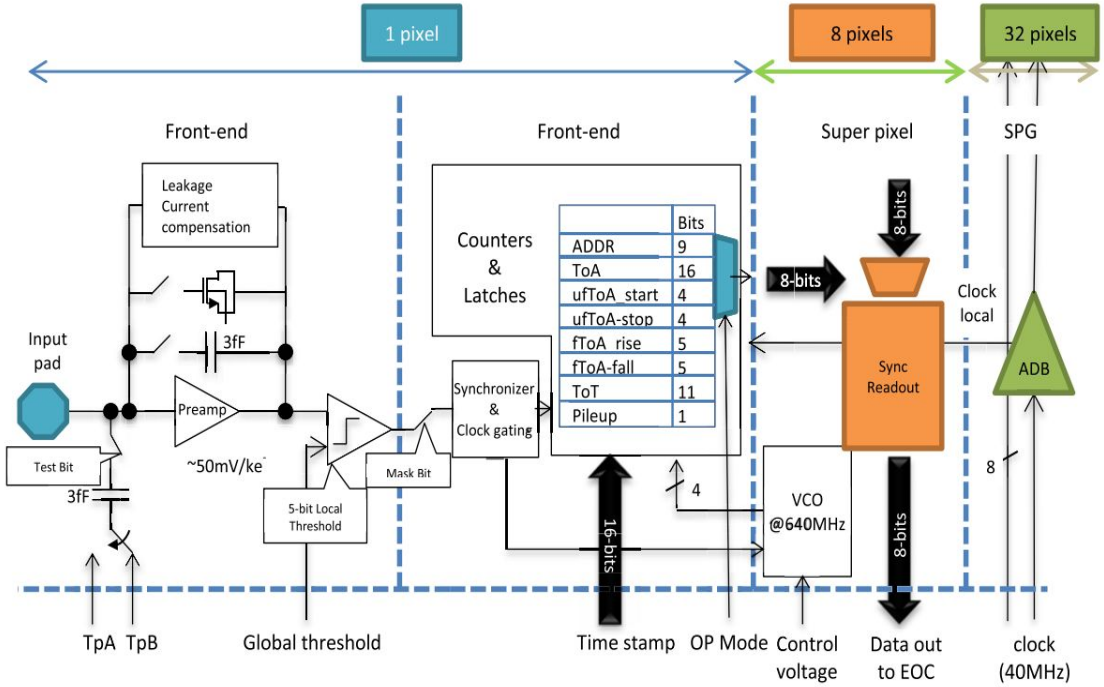
  - with TSV: ∼99.5 % active area

- Pixel level:
  - analog front-end:
    - pixel enable
    - input pad
    - charge integration circuit
    - local threshold
    - local test pulse
  - digital front-end:
    - pixel mask
    - TDC and time stamp



[X. Llopart *et al* 2022 *JINST* **17** C01044]

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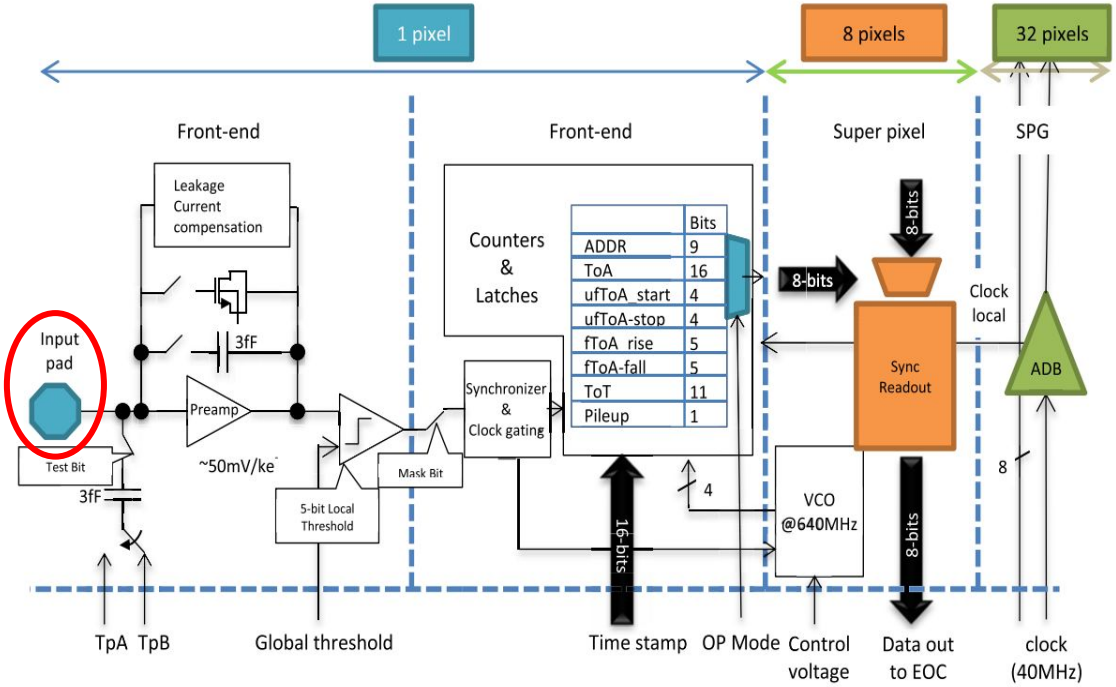

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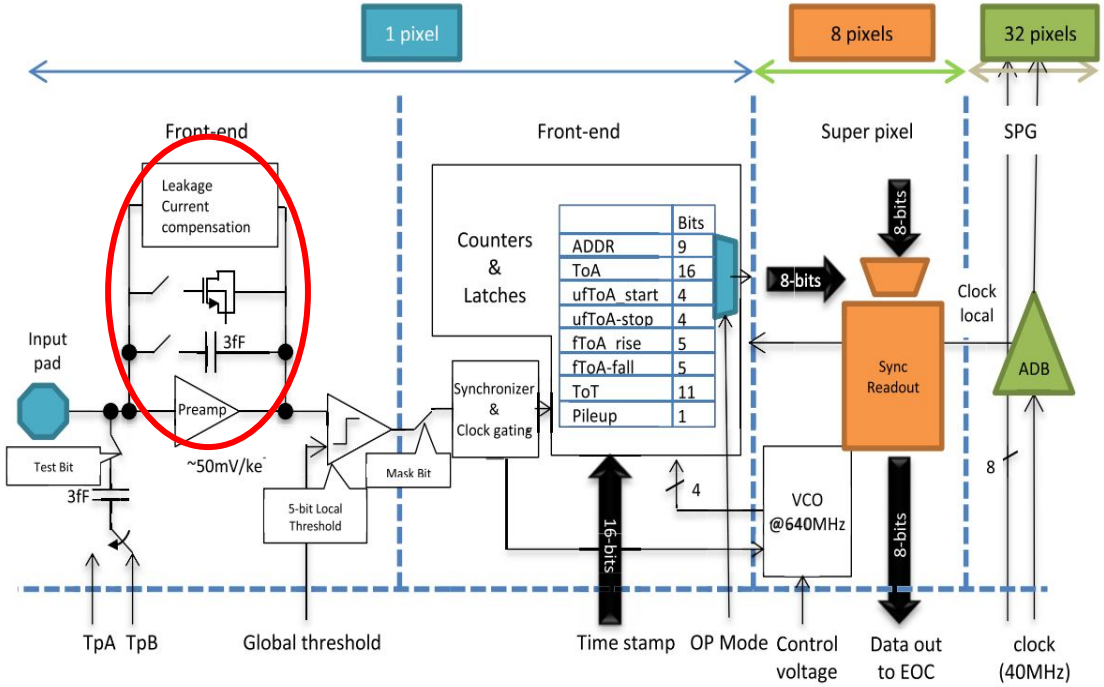

[X. Llopart *et al* 2022 *JINST* **17** C01044]

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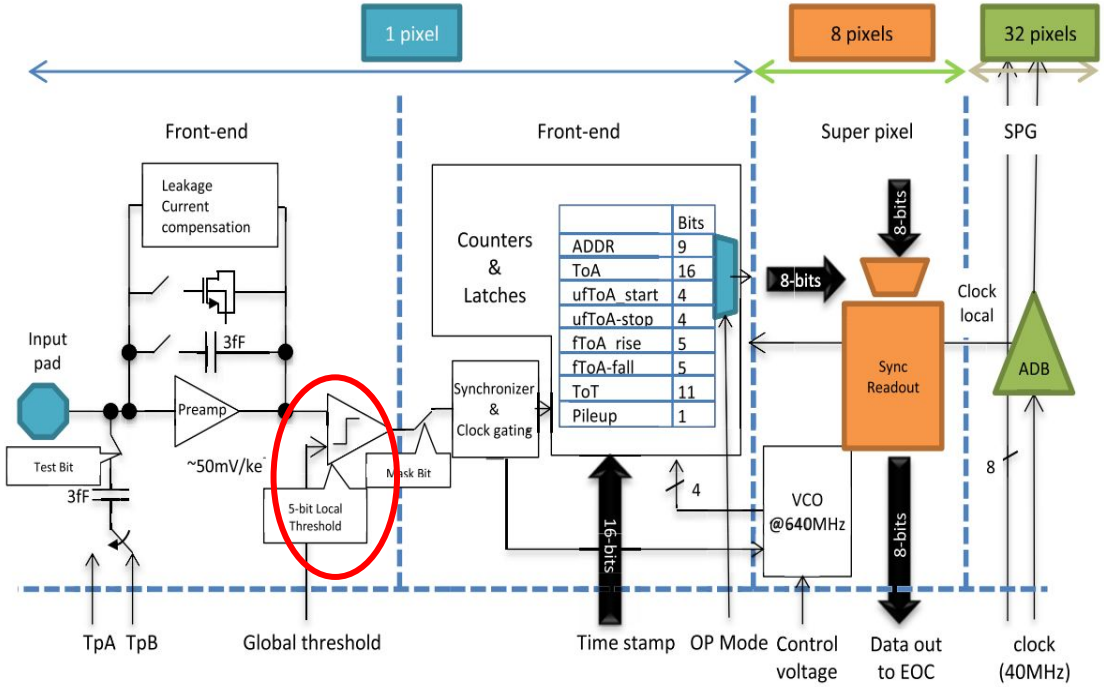

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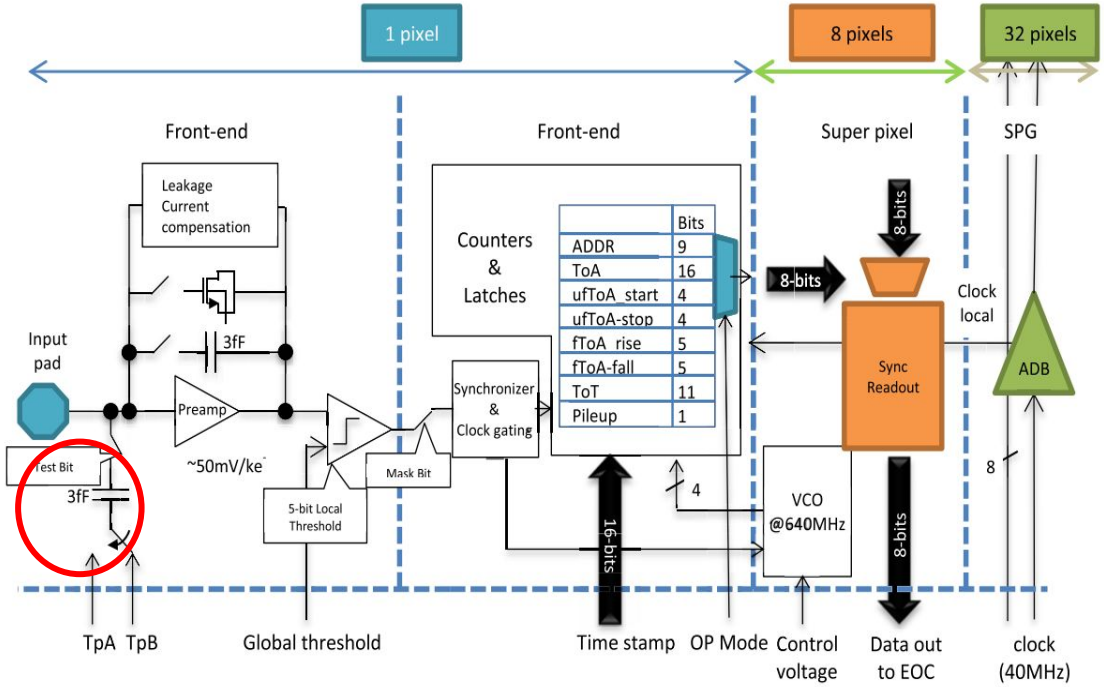

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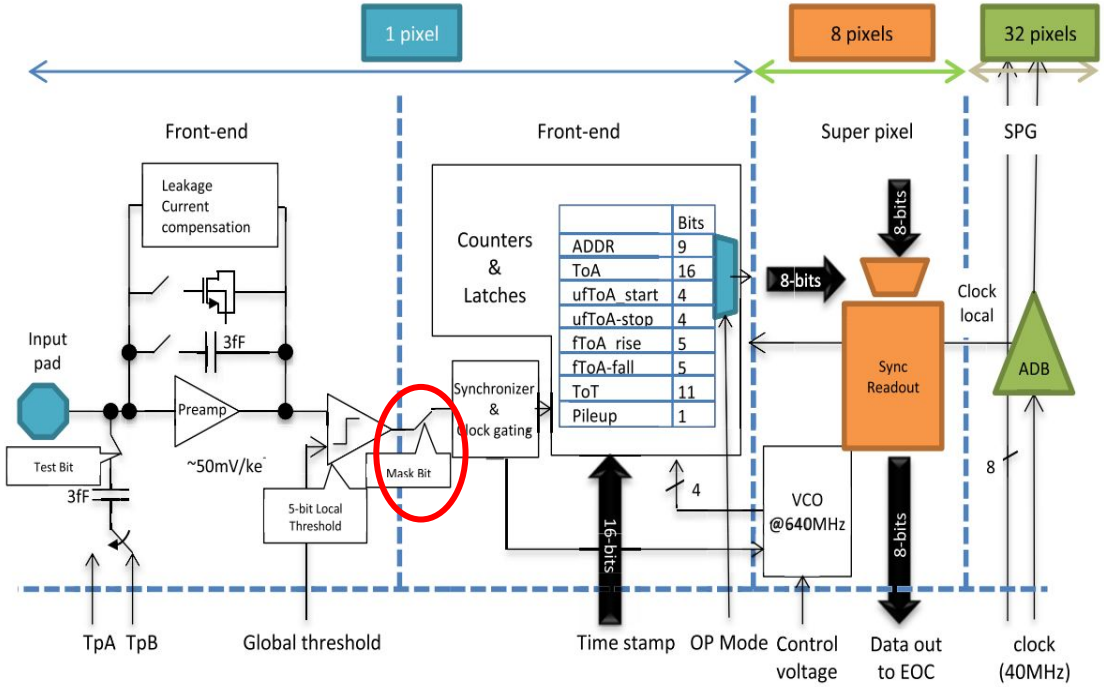

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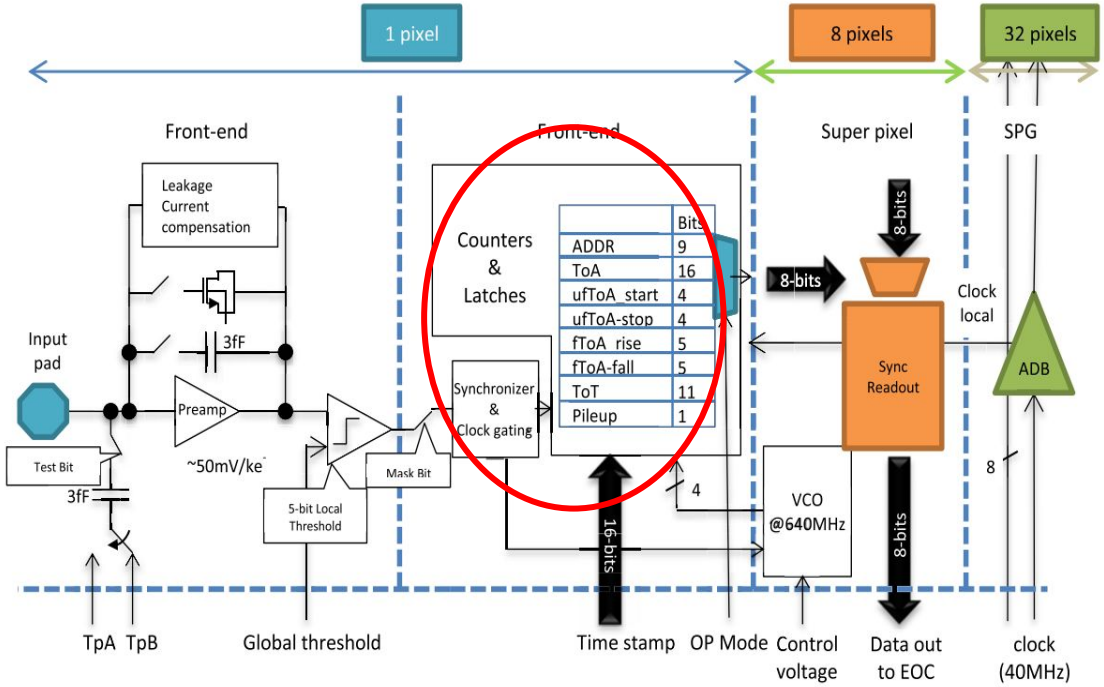

[X. Llopart *et al* 2022 *JINST* **17** C01044]

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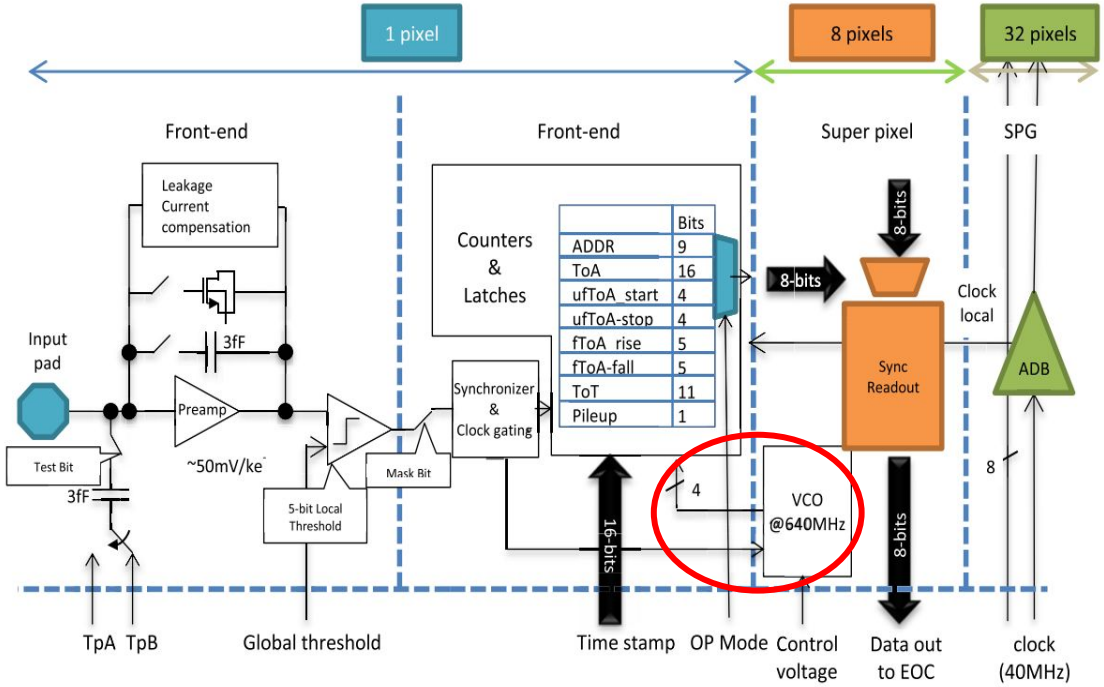
- Super Pixel level:
  - Voltage-Controlled Oscillator



[X. Llopart *et al* 2022 *JINST* **17** C01044]

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  - digital front-end:
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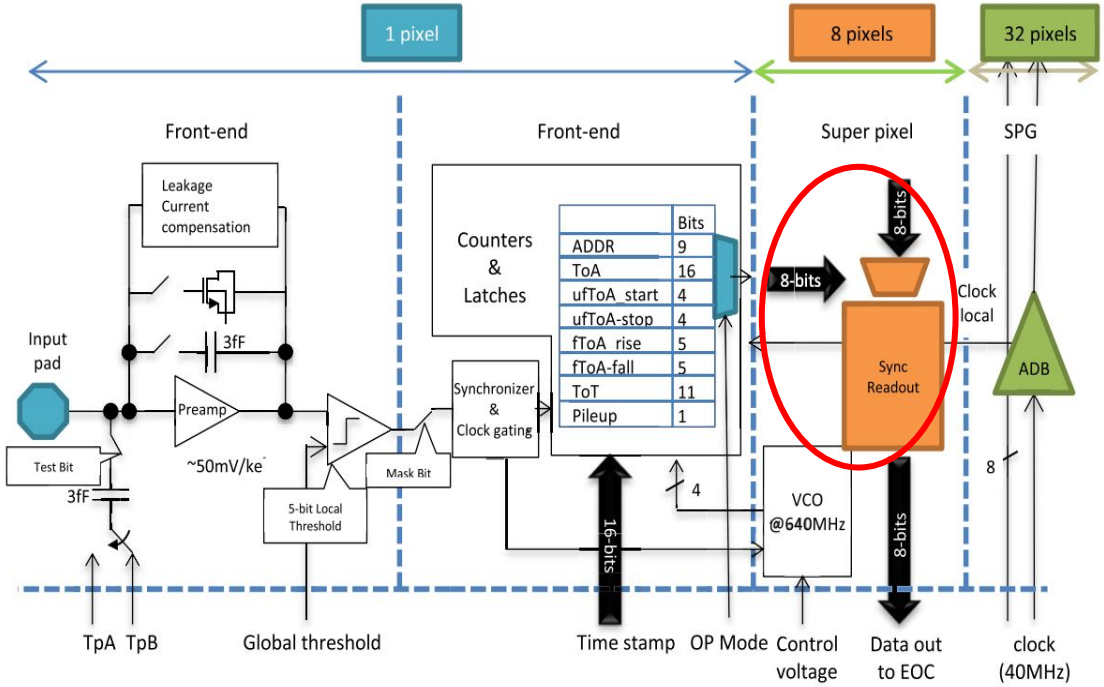
- Super Pixel level:
  - Voltage-Controlled Oscillator
  - pixels readout



[X. Llopart *et al* 2022 *JINST* **17** C01044]

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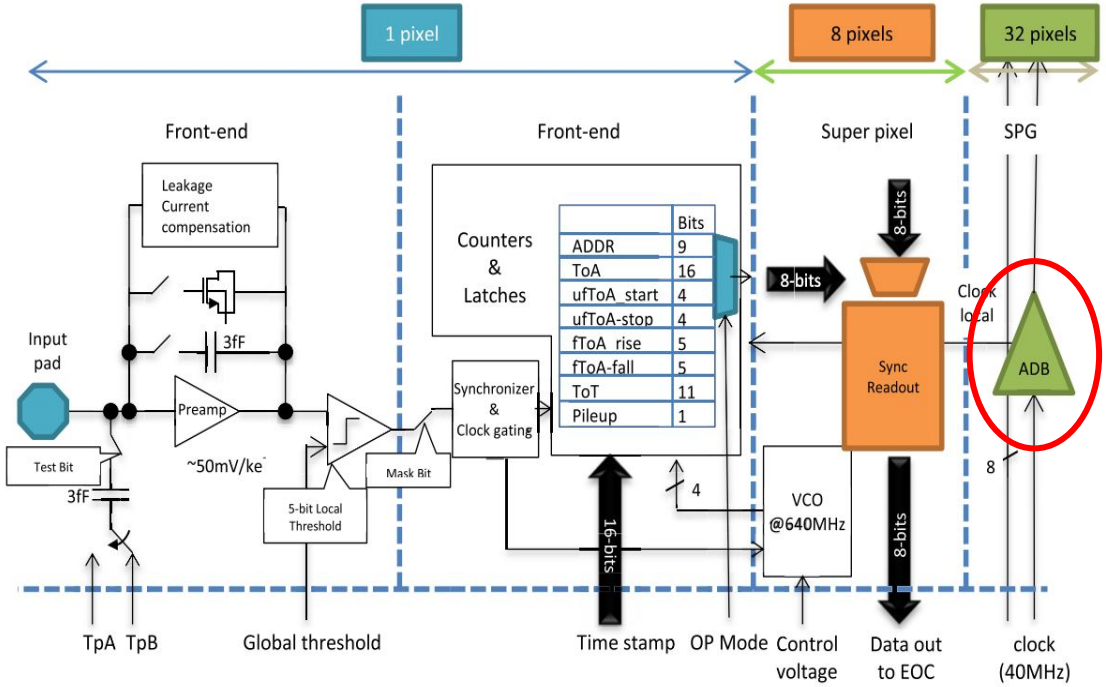
- Super Pixel level:
  - Voltage-Controlled Oscillator
  - pixels readout
- Super Pixel Group level:
  - Adjustable Delay Buffer, to correctly distribute the reference clock to the pixels across the double column



[X. Llopart *et al* 2022 *JINST* **17** C01044]

Readout modes: data driven

- Event-based readout
- Zero-suppressed
- ToA-ToT mode:
  - pixel coordinates
  - timestamp
  - charge

ToA/ToT mode packets specification

Name	Width	Bits used
Pixel address	18	[63:46]
ToA	16	[45:30]
ufToA_start	4	[29:26]
ufToA_stop	4	[25:22]
fToA_rise	5	[21:17]
fToA_fall	5	[16:12]
ToT	11	[11:1]
Pileup	1	[0:0]

Time: 29 bits

Charge: 21 bits

Readout modes: data driven

- Event-based readout
- Zero-suppressed
- ToA-ToT mode:
  - pixel coordinates
  - timestamp
  - charge
- 64-bit packets for each event, encoded with 64b/66b standard encoding communication protocol
- Output via:
  - slow control: 40 Mb/s (2.6 Hz/pixel)
  - high speed links: from 40 Mb/s to ≳ 160 Gb/s (10.8 kHz/pixel)

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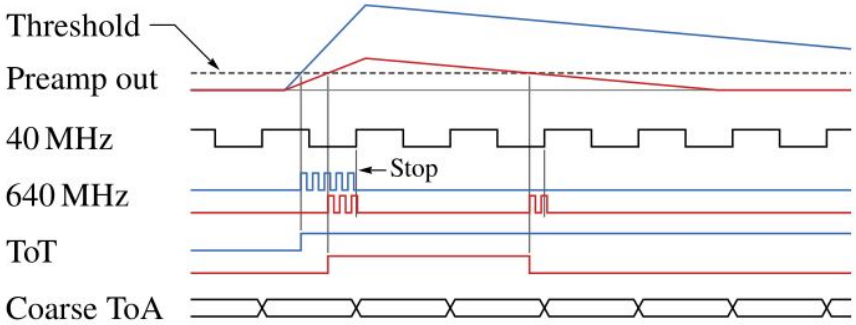
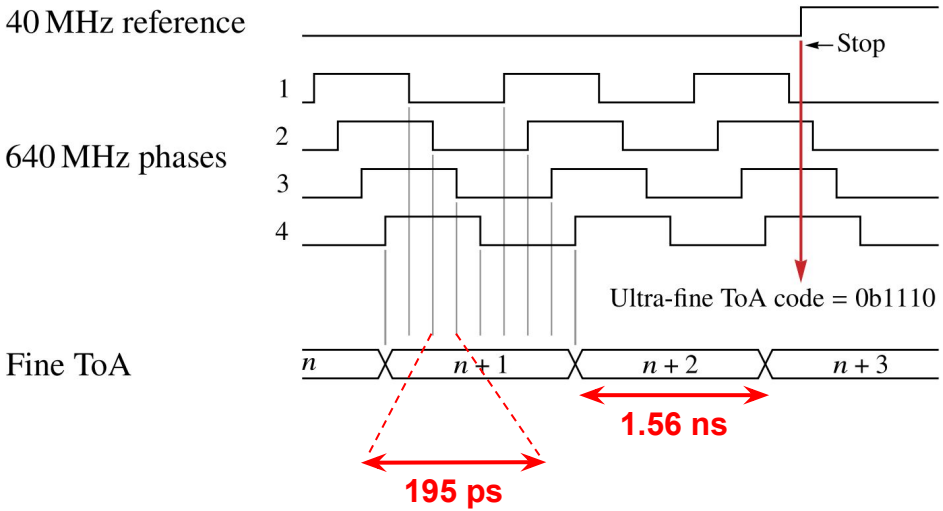
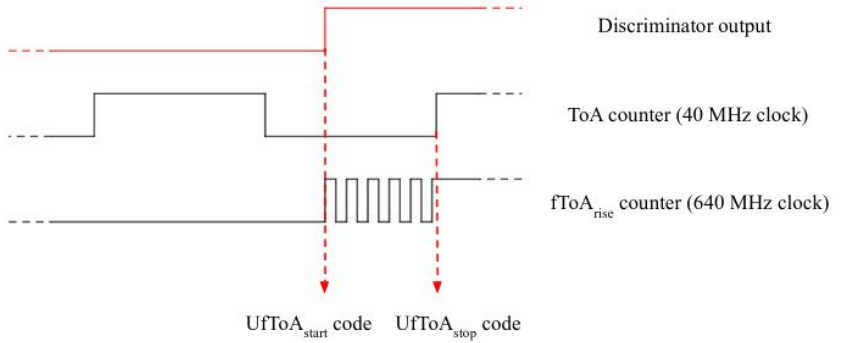
ToA and ToT measurements

- ToA measurement:
  - coarse Time-of-Arrival (ToA), **40 MHz clock** (25 ns bins width)
  - fine-ToA bins, **640 MHz clock**, generated by the VCO (**1.56 ns bins width**)
  - Ultrafine-ToA, by 4 copies of 640 MHz clock (**195 ps bins width**)
- ToT measurements: only coarse and fine



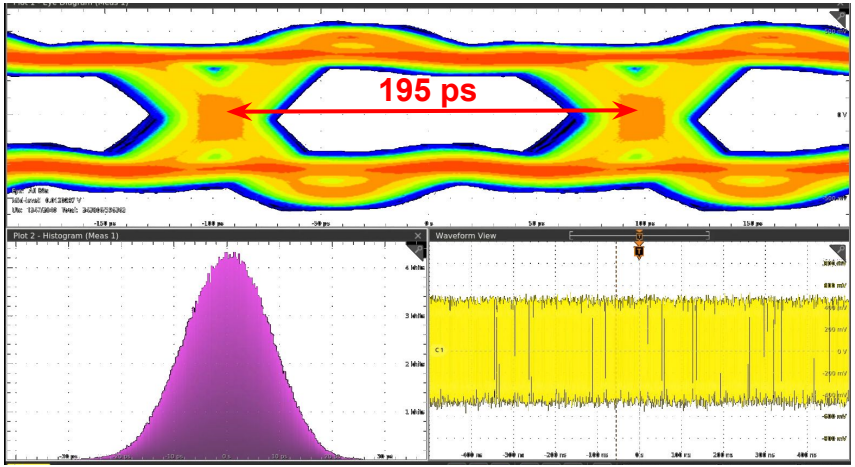




[K. Heijhoff *et al* 2022 *JINST* 17 P07006]

- Gigabit Wireline Transmitter with a Clock Cleaner (GWT-CC):
  - serializes data stream
  - transmits data to an off-chip receiver
- High configurability:
  - each link can be configured to operate at different speed, from 40 Mb/s to 10.24 Gb/s
  - possible to use from 1 to 8 links per half-matrix
- Max bandwidth of 160 Gb/s
- PRBS generator for links tests
- Tested up to 5.12 Gb/s, both with WB and TSV connection
- Timepix4 and control board links alignment and physics measurement performed only @ 2.56 Gb/s

Eye diagram of high-speed link @ 5.12 Gb/s

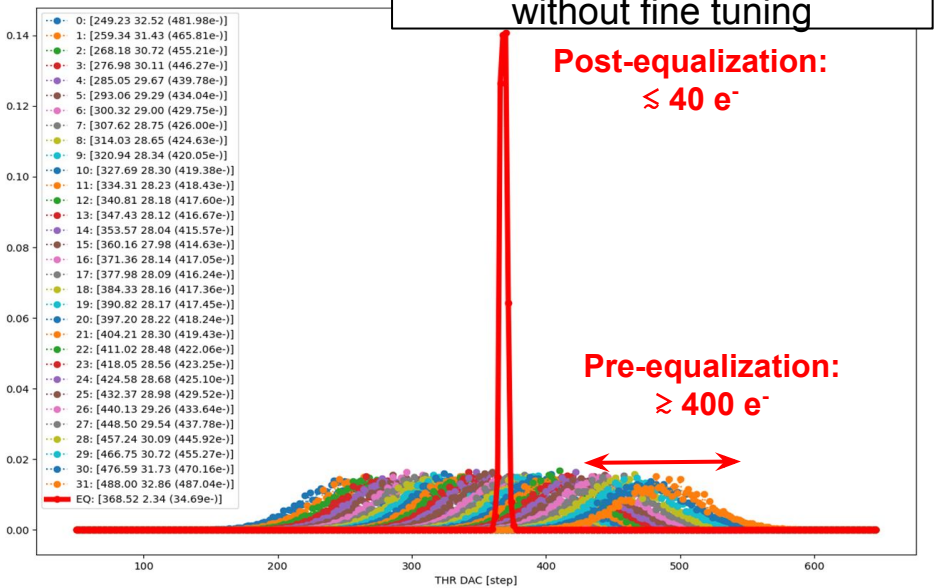


Preliminary calibrations

Preliminary calibrations - Threshold equalization and noise

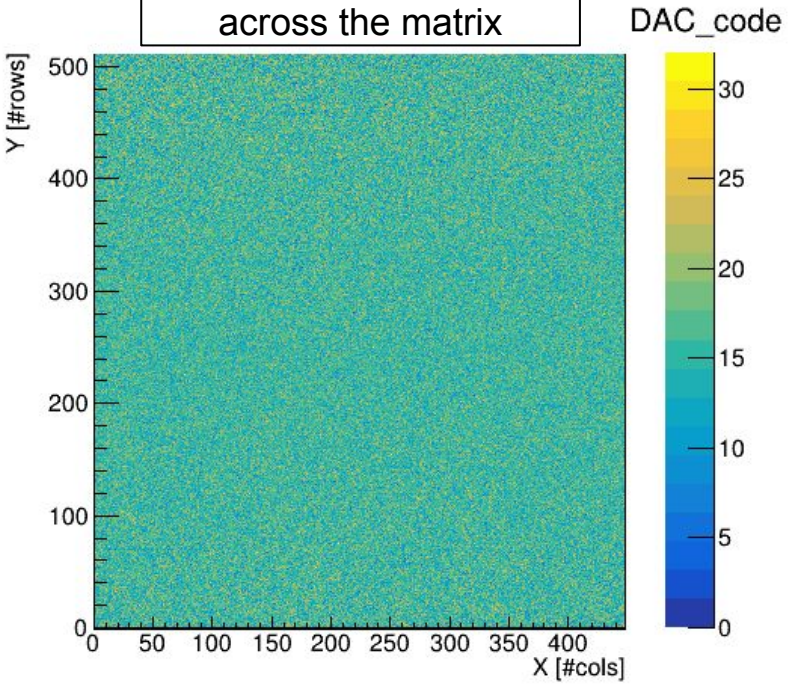
- **Threshold equalization**: threshold fine tuning at pixel level
- On-pixel 5-bits DAC to locally shift the threshold
- Method based on noise floor threshold scan
- Noisy pixel detection and masking

Threshold dispersion with or without fine tuning



[X. Llopart, XII Front-End Electronics Workshop]

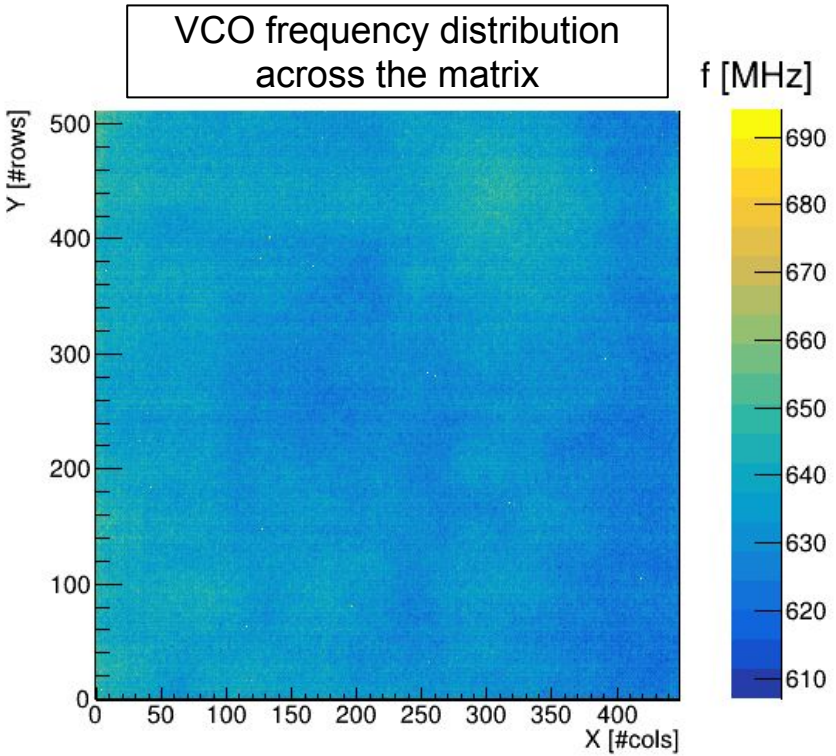
Local threshold tuning across the matrix



Typically less than 10 pixels masked out of ~230 thousand pixels

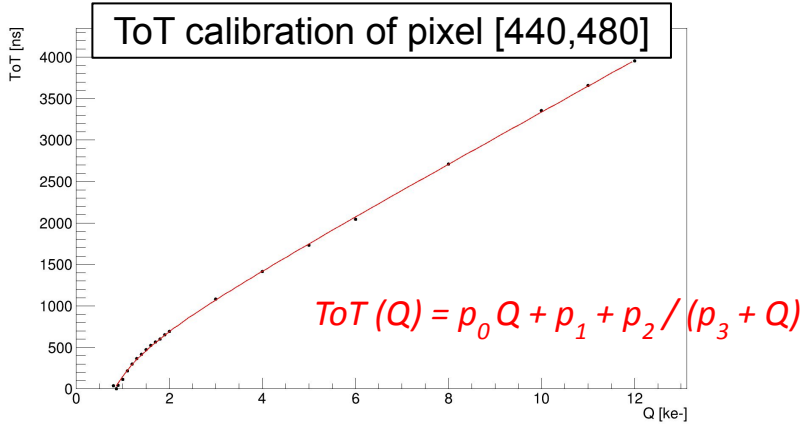
Preliminary calibrations - VCO frequency calibration

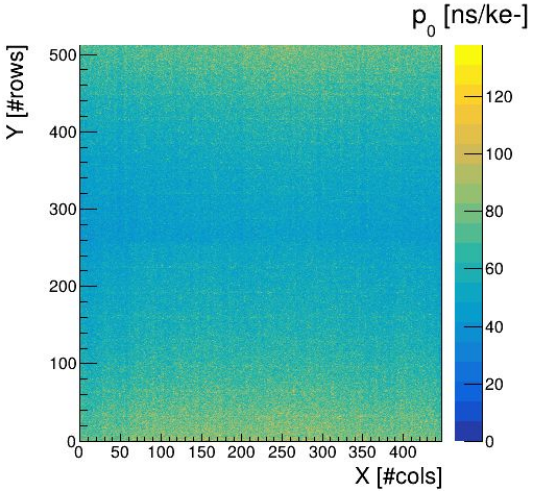
- **Voltage-Controlled Oscillators frequency** calibration:
  - On pixel VCO oscillation frequency controlled by a PLL at the center of the chip (@ 640 MHz nominal)
  - Spread caused by power supply dispersion due to large size and wire bonds
  - This spread would heavily affect the timing performance:
    - calibration and offline ToA correction allows to improve by 100-300 ps, depending on the particular measurement



Preliminary calibration - ToT vs charge calibration

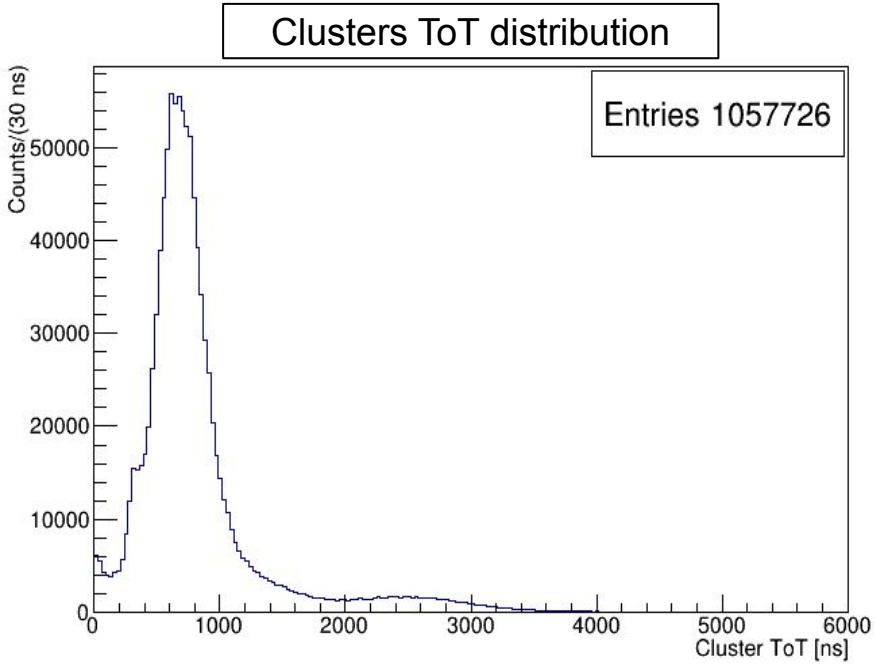
- **ToT vs Q calibration** with testpulse:
  - at fixed charge, large ToT spread across the matrix due to local gain differences
  - calibration required to correctly reconstruct the pixel charge and to correctly perform the clustering
  - non linear calibration performed with integrated testpulse tool
  - per-pixel calibration, exploiting high-speed links readout





Calibration slope distribution across the matrix

- **Validation with radioactive sources(^{137}Cs and ^{241}Am superimposed spectra)**



[R. Bolzonella *et al* 2024 *JINST* 19 P07021]

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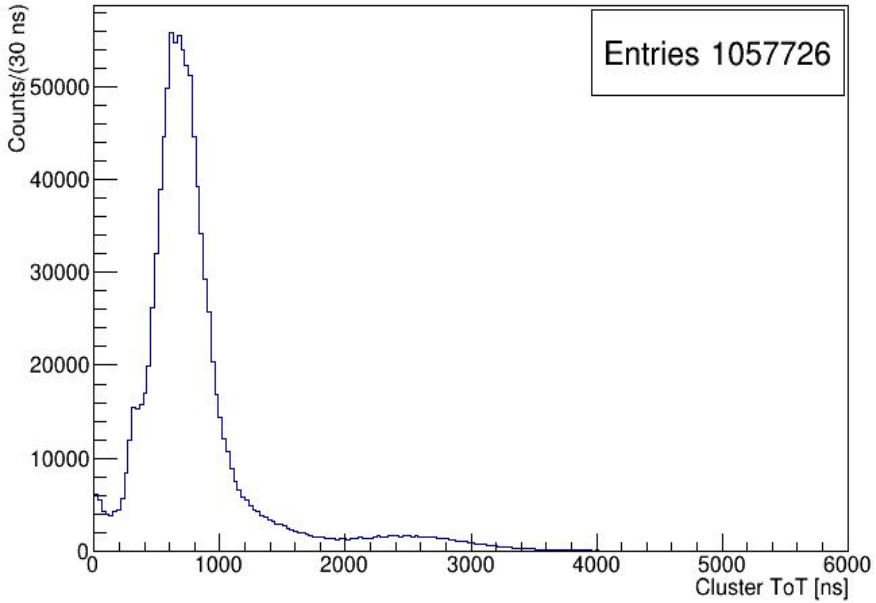
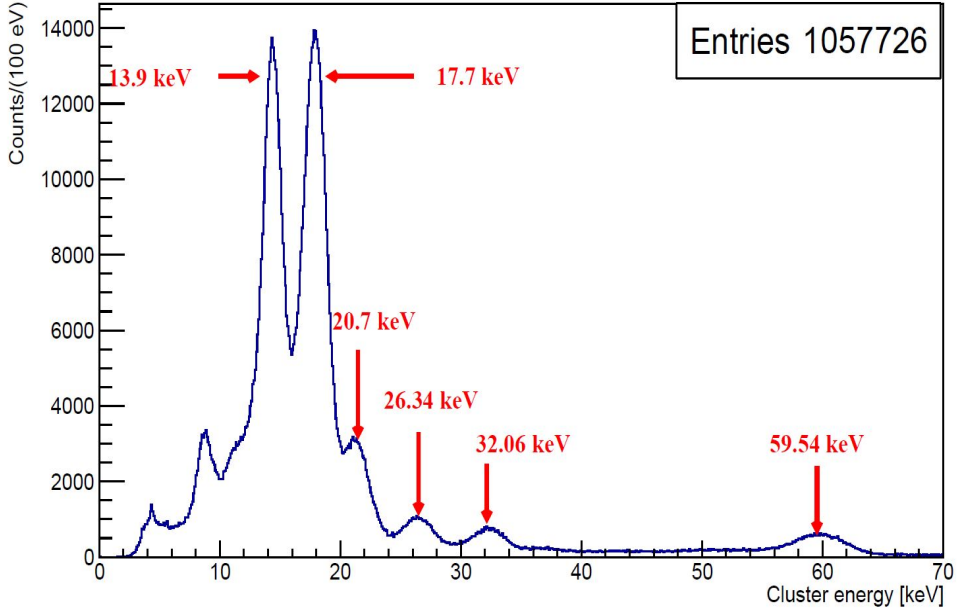
Clusters ToT distribution



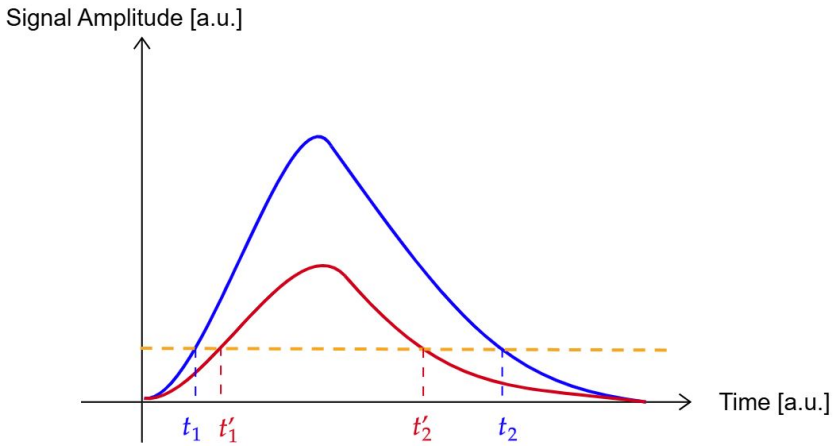
Clusters calibrated charge distribution



[R. Bolzonella *et al* 2024 *JINST* 19 P07021]

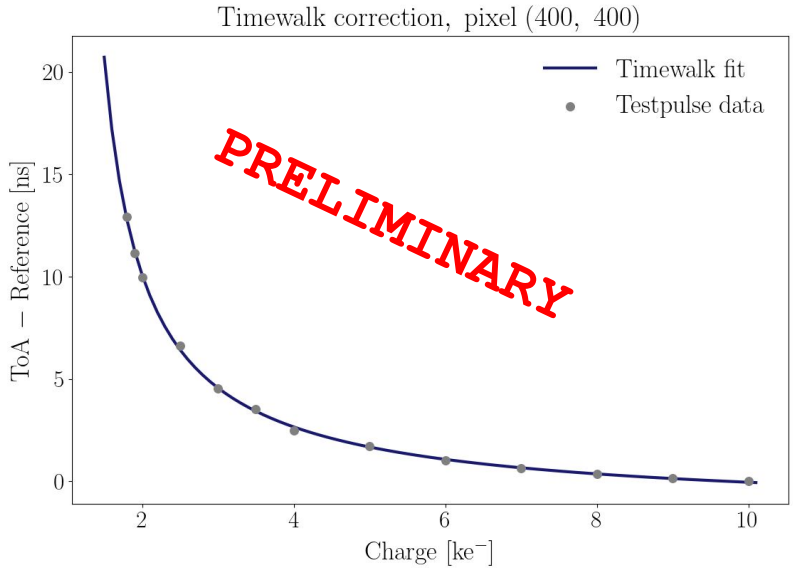
- ➢ Up to 1.6 keV FHWM (@ 14 keV)
- ➢ Resolution up to 8% (@60 keV)
- ➢ ASIC bonded to 100 µm n-on-p Si detector

➢ Lower amplitude signals rise above threshold later than higher amplitude signals starting at the same time ⇒ **Time-walk effect**



Preliminary calibration - Time walk calibration

- Lower amplitude signals rise above threshold later than higher amplitude signals starting at the same time ⇒ **Time-walk effect**
- Internal testpulse used to **calibrate the time-walk per pixel**
  - set a constant delay between the test-pulse and an external shutter
  - **shutter** time-stamp used as **reference**
  - ToA determined for several input charges



[N. Dimova, iWoRiD 2025]

Preliminary calibration - Time walk calibration

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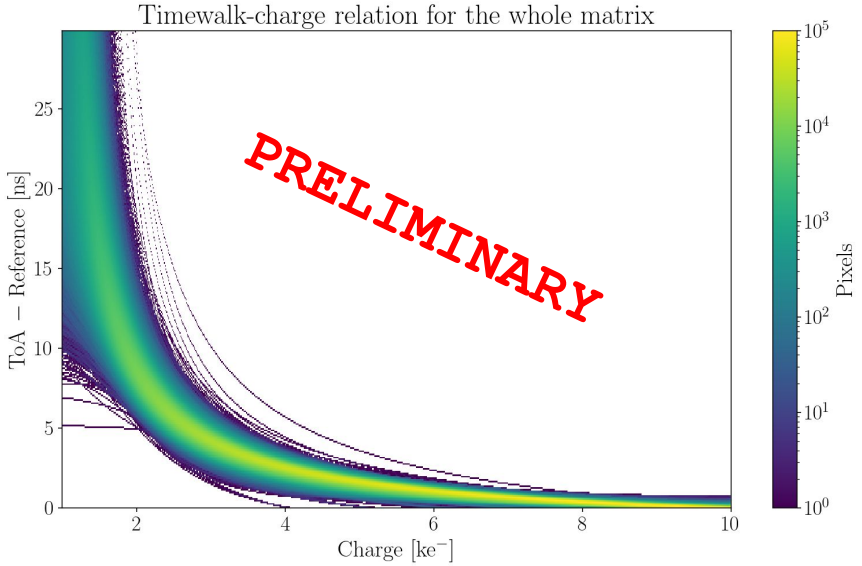
  - **shutter** time-stamp used as **reference**
  - ToA determined for several input charges
- Procedure repeated in every pixel to see the calibration variability

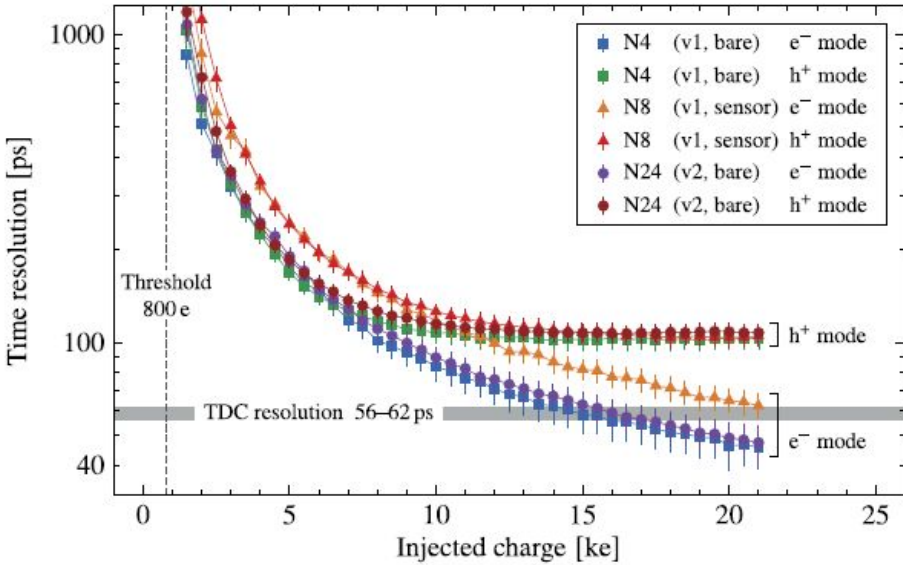


[N. Dimova, iWoRiD 2025]

Measured performance

- Analog internal test pulse used to measure the analog front-end jitter
- Hole-collecting mode:
  - jitter asymptotic to ~100 ps r.m.s., as expected due to slew rate limitations
  - bare Timepix4 and Timepix4 bonded to Si sensor show similar trends
  - at low charge, worst resolution with sensor bonded
- Electron-collecting mode:
  - no asymptotic trend
  - resolution lower than 50 ps r.m.s. both with bare and bonded chips

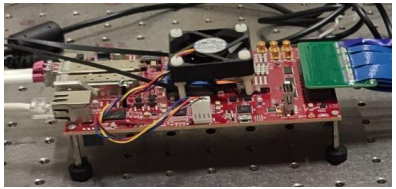
Analog front-end jitter against charge distribution



[K. Heijhoff *et al* 2022 *JINST* 17 P07006]

Timing resolution measurements - Laser measurements

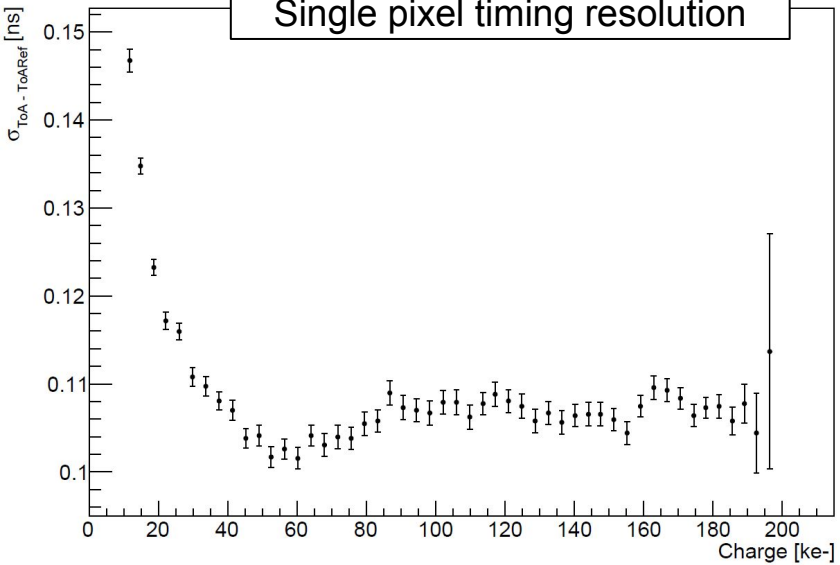
- **Spidr4** control board
- **Timepix4v2**:
  - bonded to a 100 µm n-on-p Si detector biased at -150 V
  - metalization with holes pattern
  - Courtesy of CERN and NIKHEF Medipix4/VELO groups
- **Waveform generator**
  - input signal to digital pixels
  - laser trigger
- **Laser**:
  - 1060 nm
  - variable attenuator



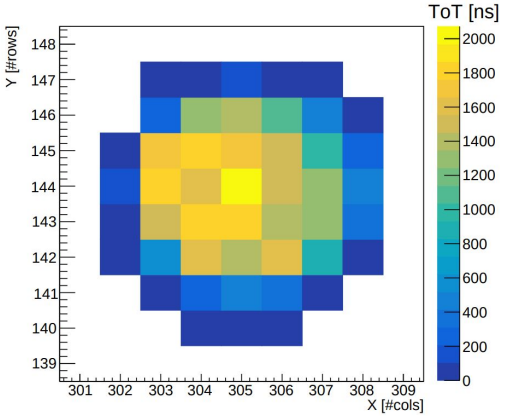
4DPHOTON project, grant agreement No. 819627, European Union's Horizon 2020 research and innovation programme - European Research Council (ERC)

Timing resolution measurements - Laser measurements

Single pixel timing resolution



Typical laser cluster



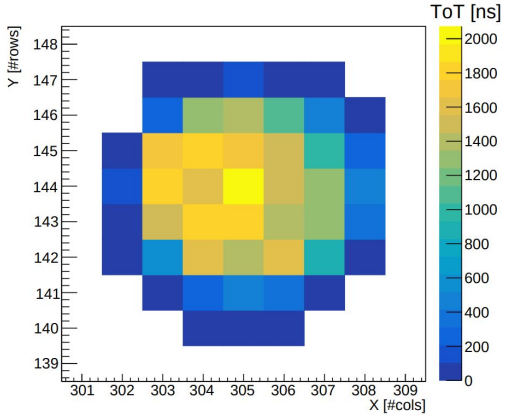
- Distribution of timing resolution as a function of injected charge in the most illuminated pixel
- Reference signal contribution estimated to be 72±3 ps rms
- After the contribution of the reference signal has been subtracted, a resolution of 107±3 ps rms is obtained

[R. Bolzonella *et al* 2024 *JINST* 19 P07021]

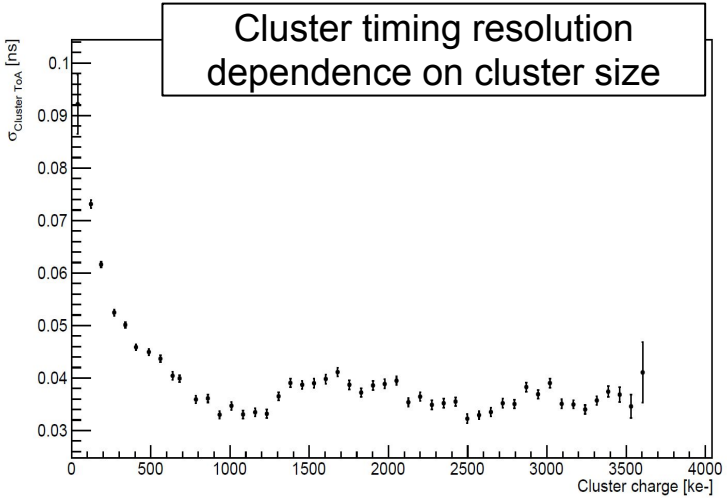
Timing resolution measurements - Laser measurements

- For each cluster (~30 pixels):
  - **weighted average** of ToA using charge as weights
  - cluster charge computed
- Timing resolution dependence on cluster charge:
  - best result: $\sigma_{ToADiffAvg}$ = 79 ± 1 ps rms
    - timing resolution after the reference signal contribution has been subtracted: σ_{ToAAvg} = 33 ± 3 ps rms

Typical laser cluster



Cluster timing resolution dependence on cluster size



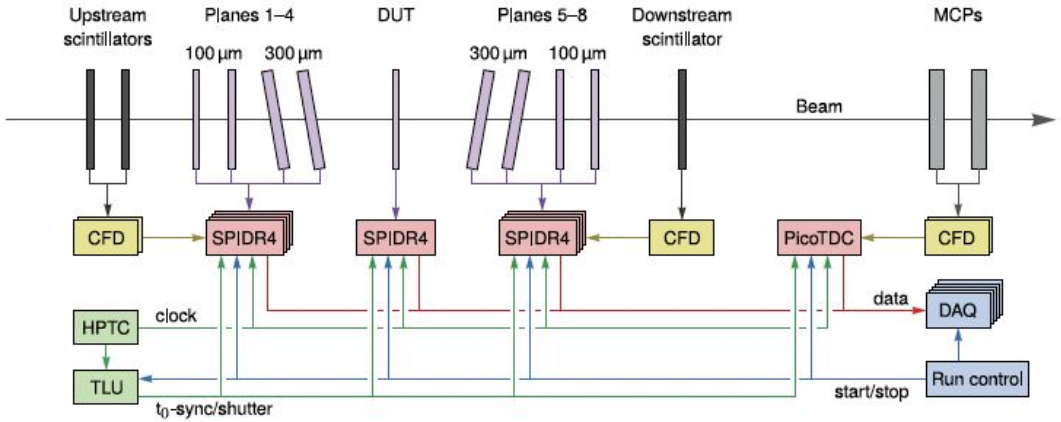
[R. Bolzonella *et al* 2024 *JINST* 19 P07021]

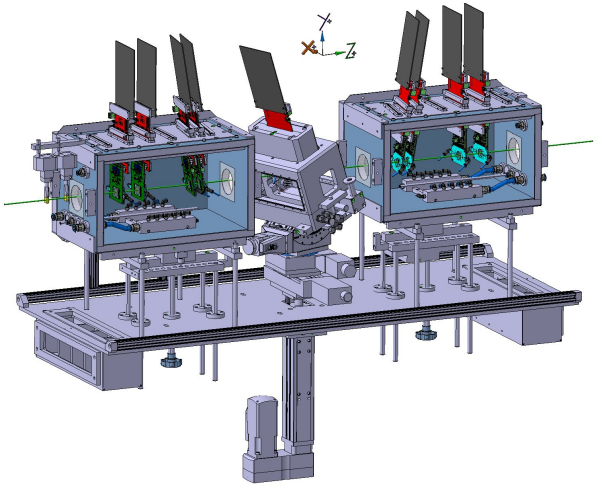
Timepix telescope

Timepix4 telescope goals:

- characterization of sensor + ASIC
- proof of concept of 4D tracker
- pointing resolution of ~2 μm @DUT
- < 50 ps track-time resolution at high rate

- Setup:
  - two arms of 4 planes each
  - DUT plane in the center, which can translate and rotate up to grazing angle
  - MCP-PMTs for timing reference
  - several DUT assemblies (planars and inverted LGAD sensors)

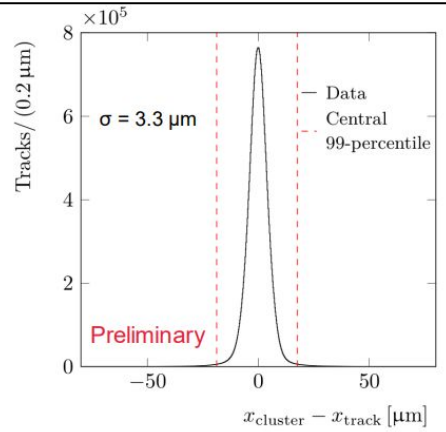


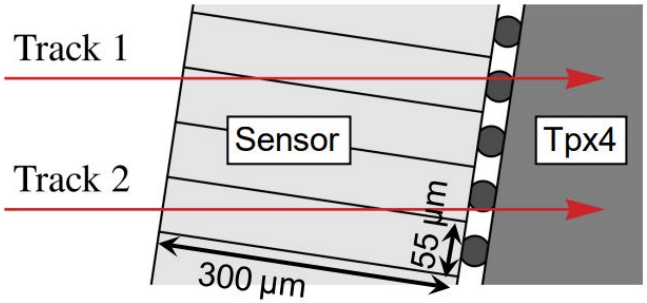


[K. Akiba et al. arXiv:2503.15207v1 [hep-ex] 19 Mar 2025]

- Spatial resolution:
  - four inner planes rotated to generate charge in multiple pixels and improve the resolution
  - single planes resolution: 3.3 µm

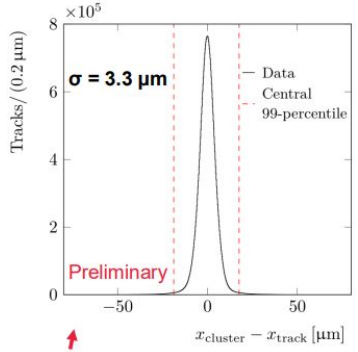
Single assembly spatial residuals





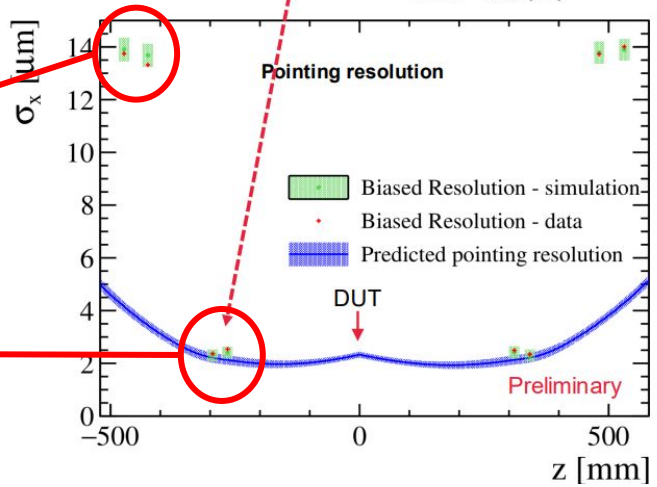
[T. Bischoff, VCI 2025]

- Spatial resolution:
  - four inner planes rotated to generate charge in multiple pixels and improve the resolution
  - single planes resolution: 3.3 µm
  - pointing resolution @DUT: 2.4 µm (Mixed hadron beam 180 GeV/c)



Planes perpendicular to the beam

Planes tilted with respect to the beam



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- Spatial resolution:
  - four inner planes rotated to generate charge in multiple pixels and improve the resolution
  - single planes resolution: 3.3 μm
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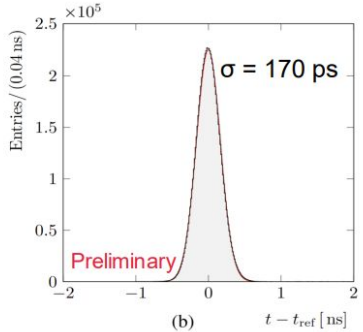
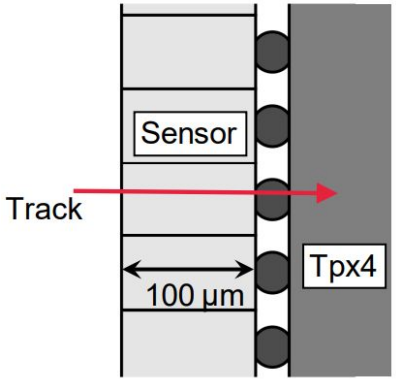
- Timing resolution:
  - thin sensor (100 μm) reduce charge sharing
  - perpendicular to the beam maximize signal charge
  - single plane resolution: 170-196 ps
    - timewalk correction: ~500 ps ⇒ ~220 ps
    - VCO calibration: ~220 ps ⇒ 170 ps

Single assembly time residuals





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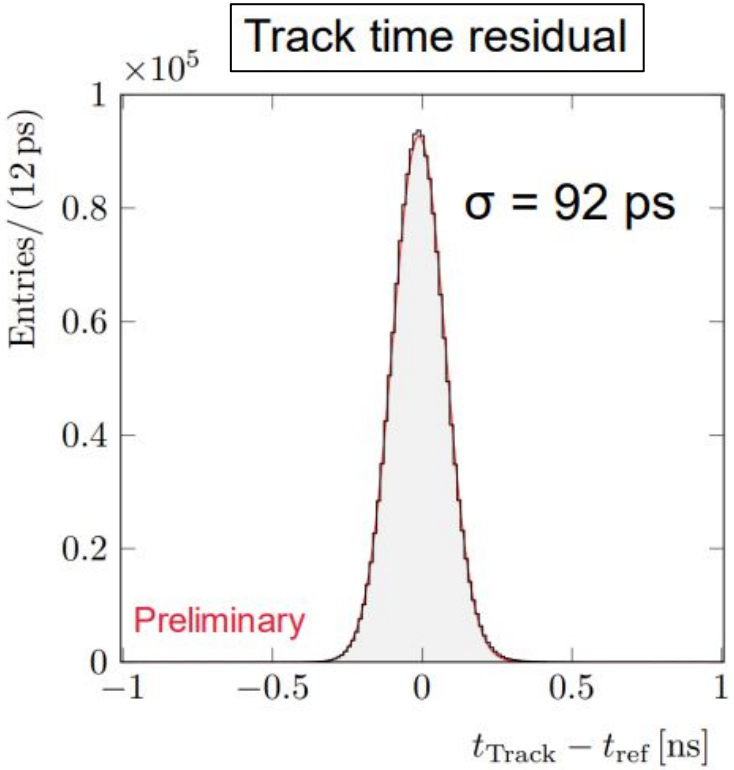
    - VCO calibration: ~220 ps ⇒ 170 ps
  - track time resolution: ~92 ps



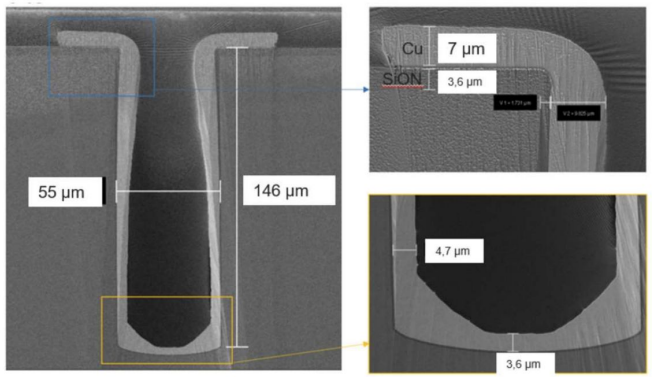
[T. Bischoff, VCI 2025]

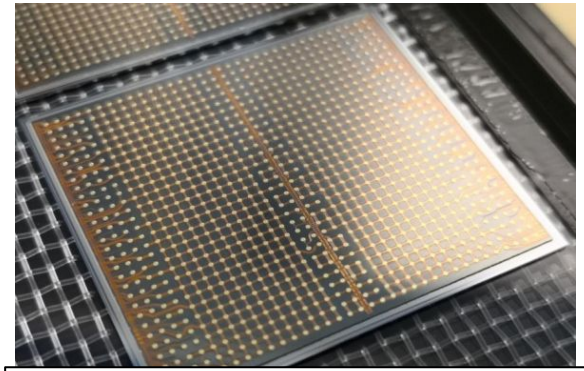
TSV assemblies status

Through-Silicon Vias status

- Redistribution layer and UBM designed at CERN
- **Multisite production** (2 European and 1 Asian)
- Devices mounted in **Nikhef chipboard** and **CERN finger board** to test
- Timepix4v0 and Timepix4v1 used as setup wafers
  - procedure validated with tests on these assemblies
- Timepix4v2 and Timepix4v3 used as “gold” wafers
- Received ~300 Timepix4v3 with TSV last week
  - quality tests ongoing

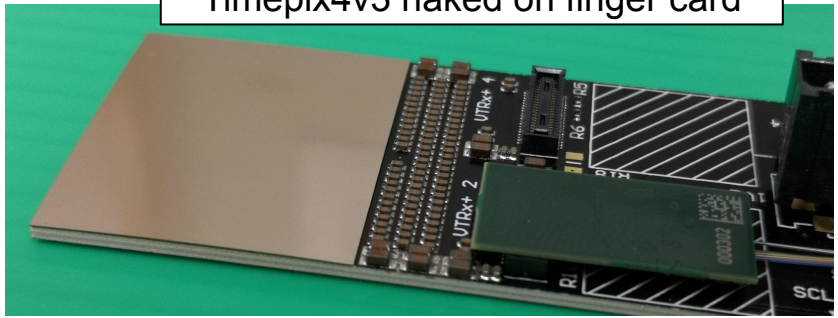
Through-Silicon Via section





Backside with redistribution layer of Timepix4v3 + N-P Si sensor

Timepix4v3 naked on finger card



Courtesy of F. Piernas, J. Alozy et al.

What’s next? The Picopix project

What's next? The Picopix project

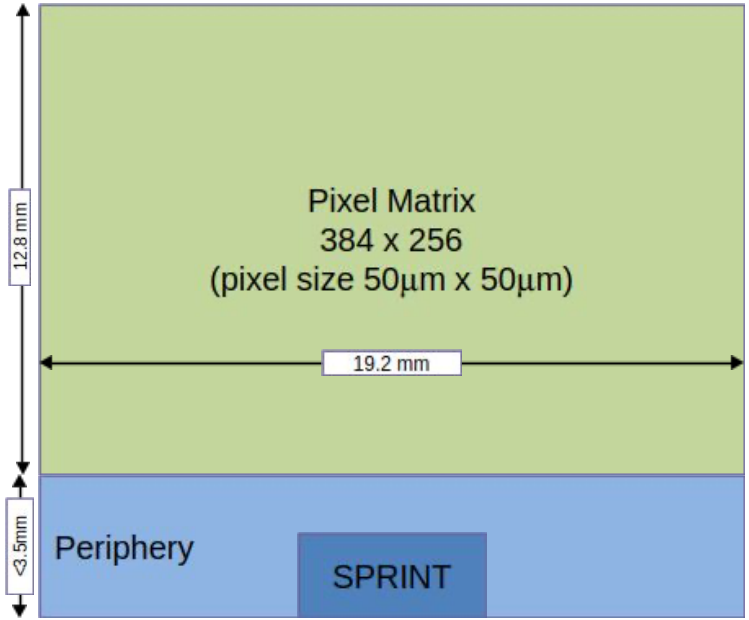
- Large-scale hybrid pixel tracking particle detector designed in 28 nm CMOS
- Promoted by different members, thus suitable to be used in different applications
  - **LHCb VELO Upgrade 2 & Fast-Sensor R&D**
    - High-precision tracking for HL-LHC
    - Timestamp bins size below 50 ps
    - Radiation-hard hybrid silicon sensors for extreme environments
  - **SY-BI Beam Loss Monitoring**
    - Bunch-by-bunch beam loss detection
    - Improved diagnostic for LHC and future e^+e^- colliders
  - **Medipix3 Collaboration** (Medical & Industrial Applications)
    - Hadron therapy beam monitoring in cancer treatment
    - X-ray diffraction and electron microscopy for material science
    - Single-layer Compton cameras for homeland security and SPECT imaging
    - Quantum sensing using entangled particle detection

Timepix4 vs Picopix

			Timepix4	Picopix
Tech. node (nm)			TSMC 65	TSMC 28
Year			2019	2026
Pixel sixe (µm)			55	50
# pixels (x x y)			448 x 512	384 x 256
Sensitive area			6.94 cm^2	2.45 cm^2
Number of sides for tiling using WB			2 (93.7% active area)	2 (78.5% active area)
Number of sides for tiling using TSV			4 (99.3% active area)	2 (78.5% active area)
Front-end		positive (h+)	High Gain (35mV/kh^+) Low Gain (20mV/kh^+) Logarithmic Gain	
		negative (e-)	High Gain (35mV/ke^-) Low Gain (20mV/ke^-)	High Gain (35mV/ke^-) Low Gain (20mV/ke^-)
Minimum detectable charge			~500 e^-	~500 e^-
Operation Modes	Tracking (Event arrival time and/or energy)	Readout	Data-driven (64-bit packet per pixel hit)	Data-driven (72-bit packet per pixel hit)
		Event Data	TOT & TOA	TOT & TOA & hitmap
		TOT energy resolution	~1KeV (FWHM Si)	~1KeV (FWHM Si)
		TOA bin size	195ps (On-pixel TDC @40MHz)	~35ps (On-pixel TDC @40MHz)
		TOA dynamic range	1.63ms (16b@40MHz)	107s (32b@40MHz)
		Max Rate	358x10^6 hits/cm^2/s	1.56x10^9 hits/cm^2/s (@ 24-bit mode)
		Max Pix Rate	10.8 KHz/pixel	39 KHz/pixel (24-bit Mode)
	Imaging (Event counting)	Readout	Full Frame-based (Continuous R/W)	Zero-suppressed (with pixel addr) (Sequential R/W)
		Counter depth	8-bits or 16-bits	12-bits
		Frame rate	89.2 kfps @8-bit 16x163Gbps 44.8 kfps @16-bit 16x163Gbps	52 kfps @102.8Gbps
		Max Count Rate	~800 x 10^9 hits/cm^2/s	~800 x 10^9 hits/cm^2/s
Maximum Readout bandwidth			≤163.84Gbps (16x @10.24 Gbps)	≤102.8Gbps (4x @25.6 Gbps)
Power consumption			700mW/cm^2 (nominal) 200mW/cm^2 (low power)	1W/cm^2 (nominal)
Other				On-pixel clustering On-chip time calibration On-chip packet sorting
Paper			https://iopscience.iop.org/article/10.1088/1748-0221/17/01/C01044	

Picopix main features

- Large-scale hybrid pixel tracking particle detector designed in 28 nm CMOS
- 3-side buttable, 384 x 256 square pixels with 50 µm pitch
- Time resolution <50 ps accounting ASIC + sensor:
  - expected σ^2_{sensor} ~ 40 ps and σ^2_{ASIC} ~ 35 ps (time bin size)



SPRINT: Silicon Photonics
Radiation-tolerant Integrated Transmitter

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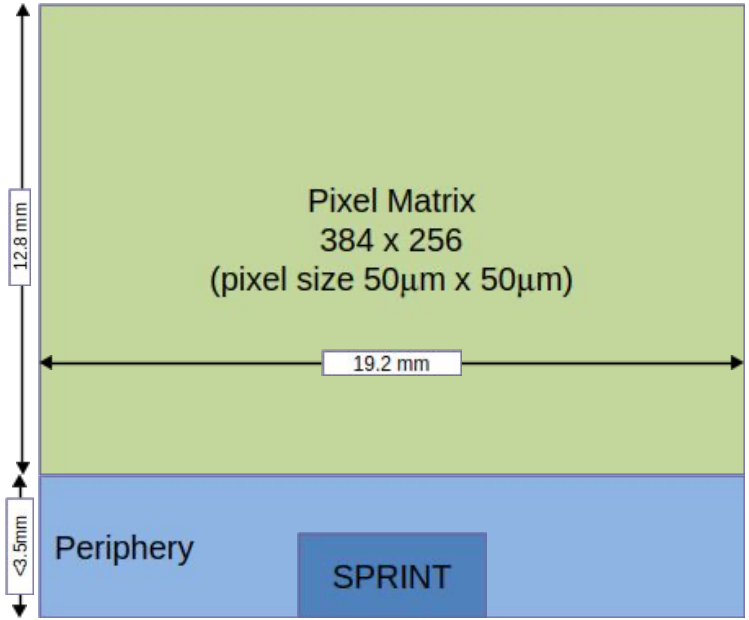
- Data reduction, on-chip programmable event clustering, veto, filtering and sorting
- Free running Digital Control Oscillators
  - ufToA: ~30-40 ps bin derived from state of VCO inner nodes
  - auto-calibrated TDC at each measurement



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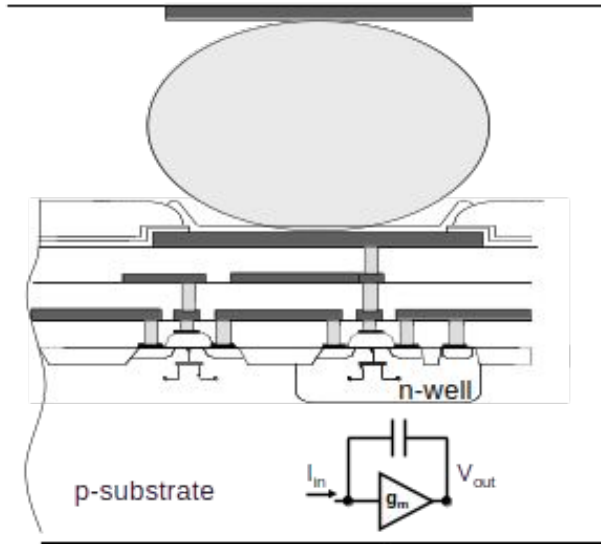
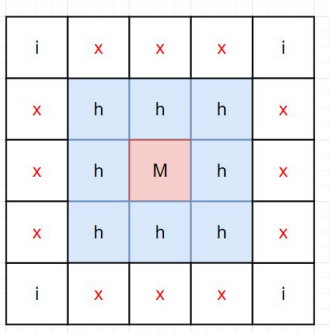


- Data driven readout with up to 4 x 25.6 Gbps fast links: up to ~3.84 x 10^9 events/chip
- Compatibility with different sensors:
  - Planar (Si, Ge, GaAs, CdTe), LGAD, 3D and naked MCP ⇒ Front-end: Charge Sensitive Amplifier
  - SPADs (anode readout at 2 V overvoltage) ⇒ Front-end: Quenching element, regeneration circuit

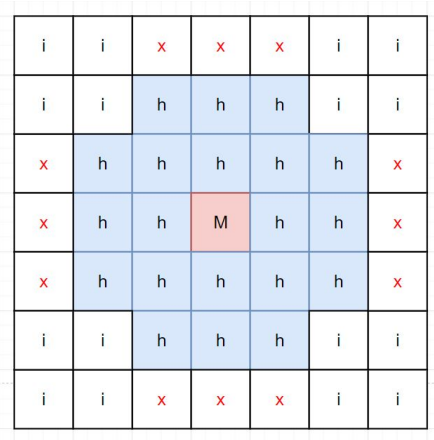
On-pixel clustering and filtering

- Data reduction and veto already at pixel level
  - Bandwidth reduction towards the periphery
  - Power and IR-drop reduction
  - Arbitration logic used in Medipix3/4
    - Transmit only master pixel packet
- Hit-map of pixels around the master
- More advanced on-pixel data filtering:
  - ToA and ToT range
  - hit-map shape (single pixel, 2, 2x2, 3x3, …)

Data filtering with 3x3 cluster veto



Data filtering with 5x5 cluster veto



On-pixel clustering and filtering

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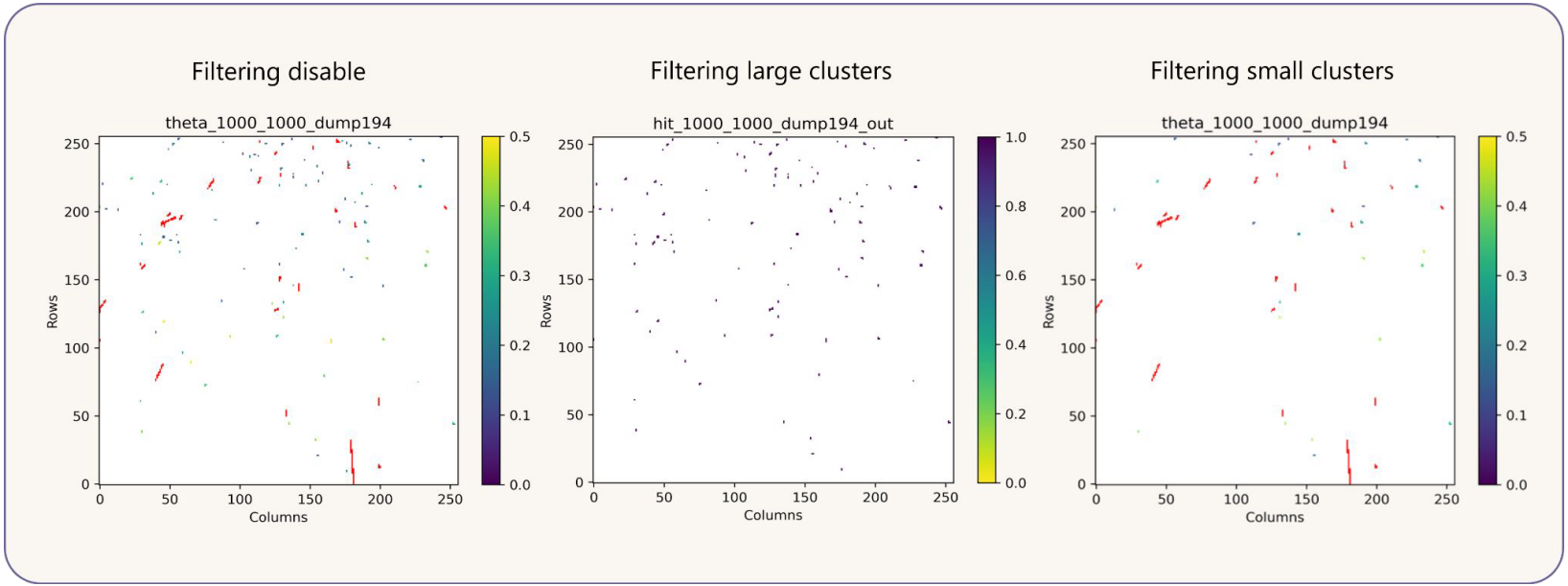
  - Bandwidth reduction towards the periphery
  - Power and IR-drop reduction
  - Arbitration logic used in Medipix3/4
    - Transmit only master pixel packet
- Hit-map of pixels around the master
- More advanced on-pixel data filtering:
  - ToA and ToT range
  - hit-map shape (single pixel, 2, 2x2, 3x3, …)
- Clustering and filtering architecture validated with simulations in a reduced matrix (256x256 pixels)



Conclusions

- Timepix4:
  - hybrid pixel detector for tracking and imaging developed by the Medipix4 collaboration
- Characteristics:
  - large active area: 6.94 cm^2
  - 4-side buttable architecture
  - ToA: 195 ps bin size
  - ToT: 1.56 ns bin size (~200 e^- rms charge resolution)
  - Readout: up to 160 Gb/s, encoded 64b/66b
- Several groups in the collaboration are using and characterizing the Timepix4
  - timing resolution, energy resolution and overall performance meeting the expectations
- Near future steps:
  - characterization with TSV processed wafers and TSV compatible chipboard (NIKHEF)
  - several DAQs being designed by members of the collaboration
- Picopix improves Timepix4 performance and simplify its use:
  - improved time binning: ~35 ps bin size
  - compatibility also with SPADs
  - allows to perform: on-pixel data filtering, on-chip time-walk and clock skew correction, on-chip packet sorting


THANK YOU
FOR YOUR ATTENTION
500
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