# XVI SuperB Workshop (LNF)

## Monday, 4 April 2011

**Parallel 1 - DCH - Room Calcolo, Bldg 14 (15:00 - 16:30)**

| time | [id] title | presenter |
|---|---|---|
| 15:00 | [56] FEA Analysis and optimization of a drift chamber structure in composite materials | ROSSETTI, Fabio |
| 15:20 | [57] Front-end, Read-out and Pre-processing electronics for a cluster timing drift chamber | CAPPELLI, Luigi<br>D'AMICO, Stefano |
| 15:40 | [128] FPGA implementation of a multi-channel, 1-ns time resolution, multi-hit TDC | IAFOLLA, Lorenzo |
| 16:00 | [129] Update on 28 chs DCH prototype FEE & DCH readout chain | FELICI, Giulietto |