Detector Status

F.Forti, INFN and University, Pisa

Overview

- Detector design is fairly advanced
  - Progress report: arxiv.org/abs/1007.4241
- R&D continuing in several areas
- Organization is in place and working well
- We are moving towards the Technical Design Report

… but …

- Significantly more physicists and engineers are needed
  - to finalize the design
  - to build and operate the detector
  - to do physics

Detector Organization

Detector Coordinators – B.Ratcliff, F. Forti
Technical Coordinator – W.Wisnieswki

- SVT – G. Rizzo
- DCH – G. Finocchiaro, M.Roney
- PID – N.Arnaud, J.Va'vra
- EMC – F.Porter, C.Cecchi
- IFR – R.Calabrese
- Magnet – W.Wisniewski
- Electronics, Trigger, DAQ – D. Breton, U. Marconi
- Online/DAQ – S.Luitz
- Offline SW –
  - Simulation coordinator – D.Brown
  - Fast simulation – M. Rama
  - Full Simulation – F. Bianchi
- Rad monitor –
- Lumi monitor –
- Polarimeter –
- Background simulation – M.Boscolo, E.Paoloni
- Machine Detector Interface –

Detector Geometry Working Group
Chairs M.Rama, A.Stocchi

Forward Task Force
Chair H.Jawahery

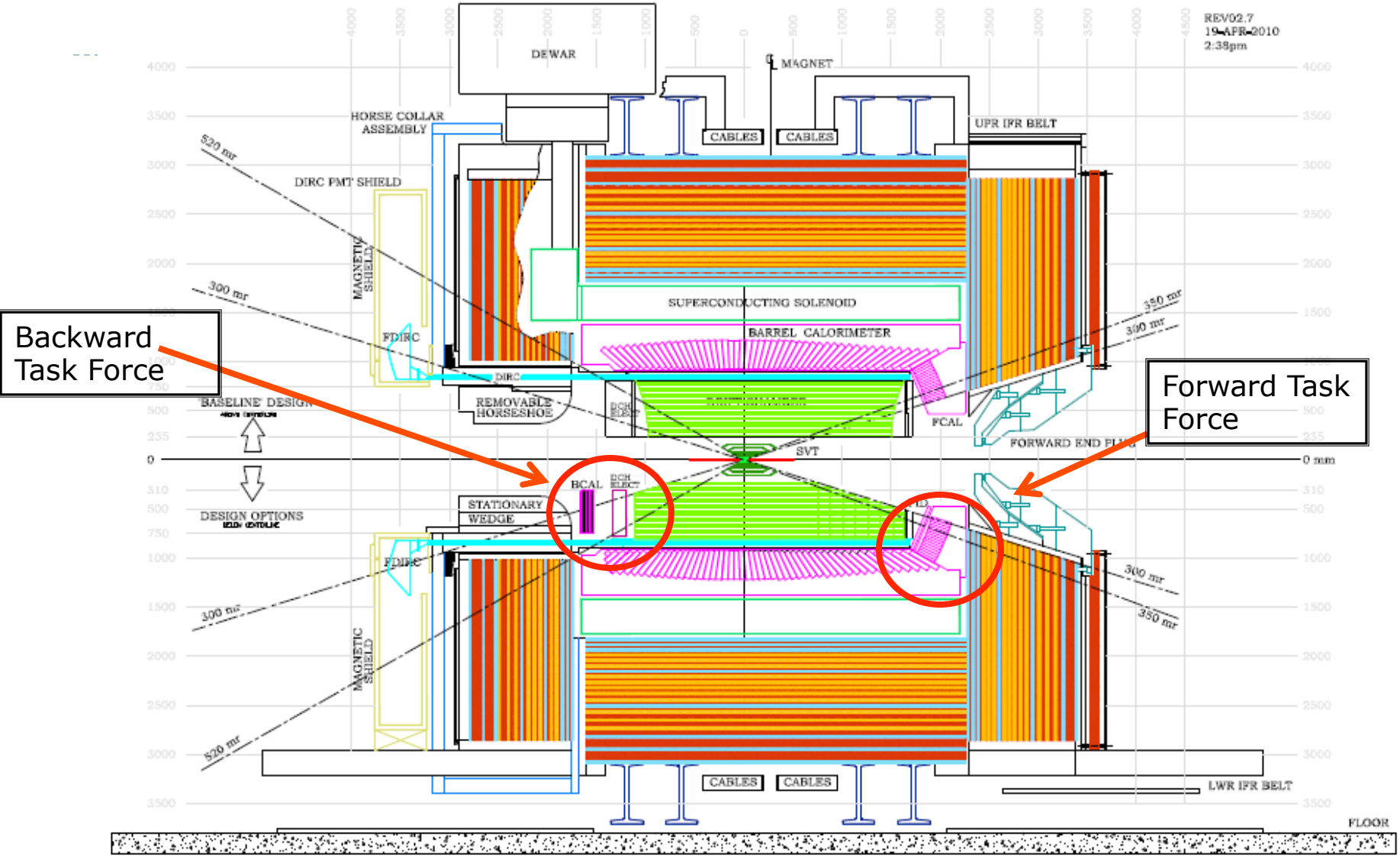
Backward Task Force
Chair W. Wisniewski

To be created:
Mechanical integration team
Central electronics team

Institutions

System	Institutions
SVT	Bologna, Milano, Pavia, Pisa, Rome3, Torino, Trieste, Trento, LBNL, Queen Mary, RAL
DCH	LNF, McGill, Montreal, TRIUMF, UBC, Victoria
PID	SLAC, BINP , Hawaii, Cincinnati, Bari, Padova, Maryland, LAL, LPNHE
EMC	Bergen, Caltech, Edinburgh, McGill, Perugia, Rome I
IFR	Ferrara, Padova
ETD	SLAC, Caltech, Napoli, Bologna, LAL, Padova, Roma3
Computing	Padova, Ferrara, Torino, Bologna, Rome2, Pisa, Perugia, LNF, LBNL, Napoli, SLAC
Magnet/ Integration	SLAC, LNF, Pisa
Backgrounds	Pisa, LNF
TBD	(Valencia, Barcelona, Annecy, Strasbourg, Tel Aviv, Ohio State, Liverpool, Kiev, Krakow,...)

Detector Design (with options)



Detector Design Issues

System	Baseline	Issues (technical OR manpower; R&D)
MDI	Initial IR designed	Magnetic elements and radiation masks. Design of tungsten shields. Background simulations: global map, detector occupancy
SVT	6-layer silicon	Technology for Layer 0: striplets or pixels. Thin pixels R&D. Readout chip for strips. Mechanical design.
DCH	Stereo-axial He-based	Dimensions (inner radius, length). Mechanical structure Cluster counting option.
EMC	Barrel: CsI(Tl) Forw: LYSO	Electronics and trigger. Mechanical structure Forward EMC technology: LYSO / LYSO+CsI(Tl); Pure CsI. Backward EMC: cost/benefit analysis
PID	DIRC w/ FBLOCK	FBLOCK design. Photon detection. Mechanical structure Forward PID: cost/benefit analysis. Different technologies.
IFR	Scintillator+ fibers	8 vs 9 layers. SiPM radiation damage and location. Extra 10cm iron. Mechanical design and yoke reuse.
ETD	Synchronous const. latency	Fast link rad hardness. L1Trigger (jitter and rate). ROM design. Link to computing for HLT.

TDR process and timeline

- The Technical Design Report is an essential step to get funding and get the detector built.
- Conflicting requirements
  - Essential to enlarge the collaboration, define institutional responsibilites and find resources for designing and building the detector
  - Essential that collaboration members, institutions and countries take ownership of the design and fabrication
  - Essential to move forward rapidly to finalizing the design and writing the TDR
- Timeline has to be adjusted to these requirements
  - Can be different for different systems

MDI

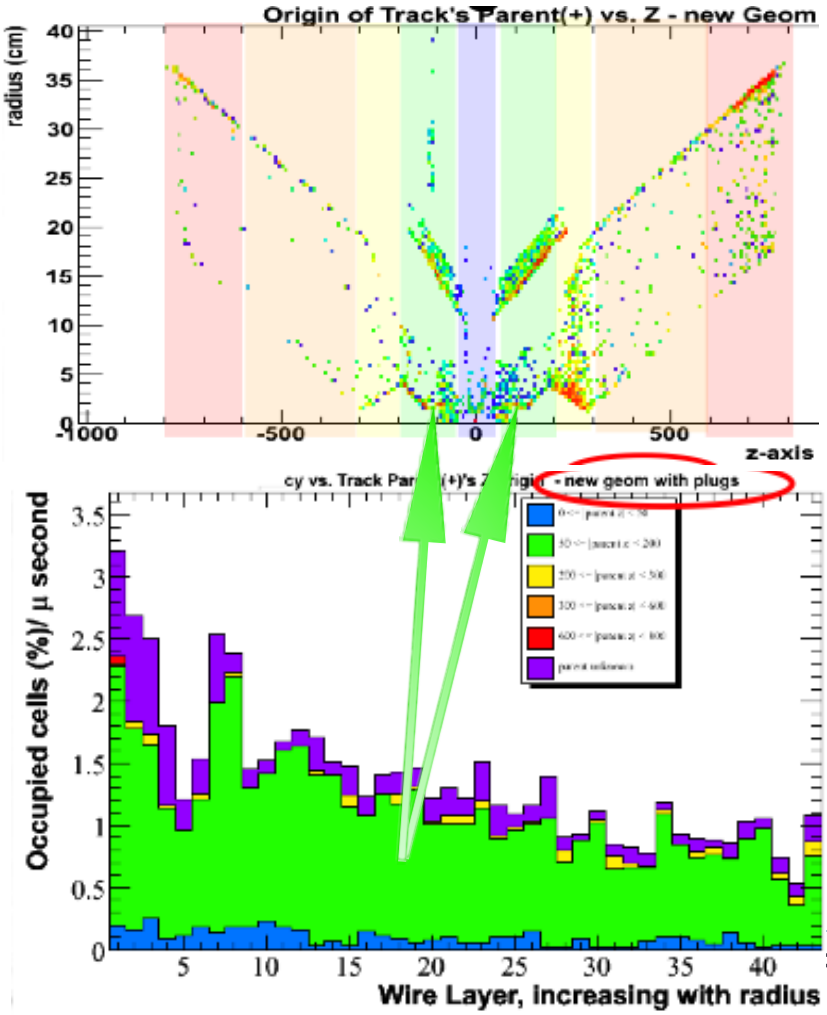
Eugenio Paoloni

Bkg simulation: progresses since Caltech

- DCH bkg. rate dependence on max G4 step length
  - The Geant4 default approximation made for slow particles traveling in low density material overestimates the multiple Coulomb scattering effect
  - Low p_t electrons caged in a single DCH cell by the magnetic field erroneously scattered over several cells giving rise to severe overestimates of the bkg. rate (R.Cenci).
- Correlation studies of loss position at the beam pipe and rate observed in the DCH, very useful for shield optimizations (D. Lindemann)
- Beam line + detector hall model (A.Perez)
- First look at the radiation map of the detector hall (R.Cenci)
- First look at the pair production rate on L0 in the 2 machine options (high/low boost @ charm threshold)
- Backward EMC scoring (S.Germani), fTOF (L.Burmistrov + R.Cenci)
- Bruno Optical photon simulation (A. Di Simone + D. Roberts)
- Please join the tomorrow afternoon Bkg parallel for further details

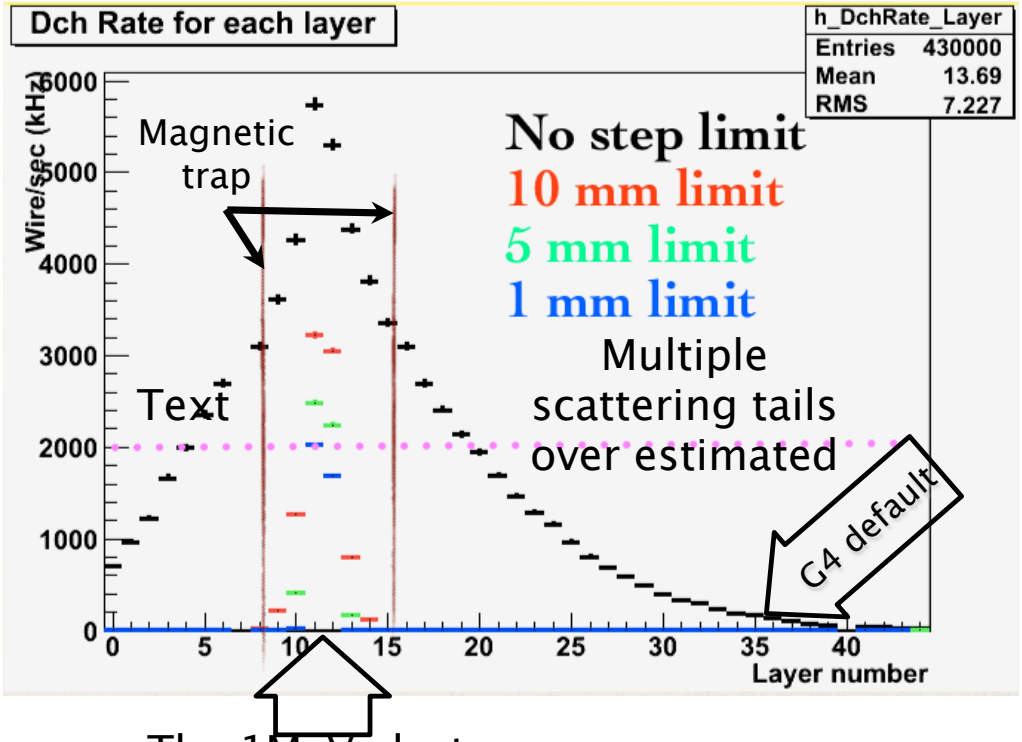
DCH Background studies

The source of DCH backgrounds are mainly concentrated in +/- 20 cm from IP (Dana)



The default Geant4 setting overestimate the moultiple Coulomb scattering (Riccardo)

Single electrons, 1 MeV



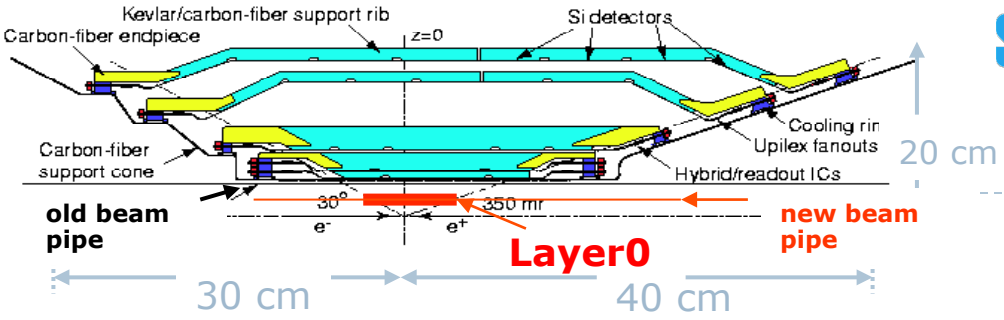
Focus of the meeting

- Definition a Quality Assurance policy for the next productions
  - Subsystem + machine reference plots
  - Definition of a before production "takeoff" checklist & sign off procedure
- Definition of a set of reference plot for background studies
  - Definition of a right after production "landing" checklist to validate the production output
- Write down the shopping list for the simulation of the poorly simulated/still not simulated background sources

SVT

Giuliana Rizzo

SVT



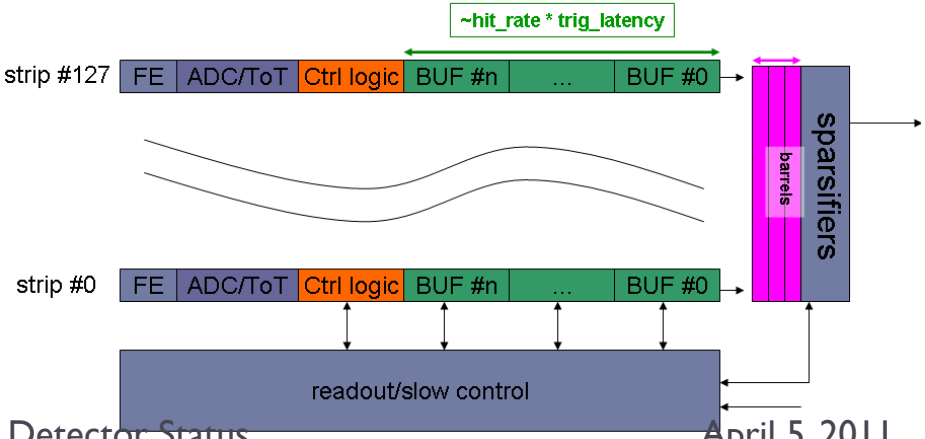
- SVT Baseline for TDR
  - Striplets in Layer0 @ R~1.5 cm
  - 5 layers of silicon strip modules (extended coverage w.r.t BaBar)
- Upgrade Layer0 to thin pixel for full luminosity run
  - more robust against background occupancy
- Since Caltech (approval!) more focused activities on the design of the SVT baseline option with regular biweekly SVT-TDR meetings
- Some progress also on pixel R&D
  - Slower than expected due to very long delays in delivery of first Vertical Integration (3D) MAPS → some results available from 2D wafers.
  - Preparation of new submissions for 3D pixels and INMAPS process.
- Testbeam in preparation for Sept. 2011

Main progress on SVT baseline (I)

- Requirement definitions for strip/striplets FE readout chips:
  - Very different among layers: striplets: ~2 MHit/strip → 25 ns shaping time & fast readout , Layer4-5 strip: long modules → 1 μs shaping
  - Existent FE chips do not match and we need to develop new chip(s)
  - Analog channels could be designed by Pavia group
  - Just started to evaluate if readout architecture we developed for pixel could be used for strip and striplets FE chips. Probably yes but need more thinking/simulation. Manpower is an issue.

The readout sees the 128 strips with N buffers each (to store hits during trigger latency) as a pixel matrix with 128xN pixels

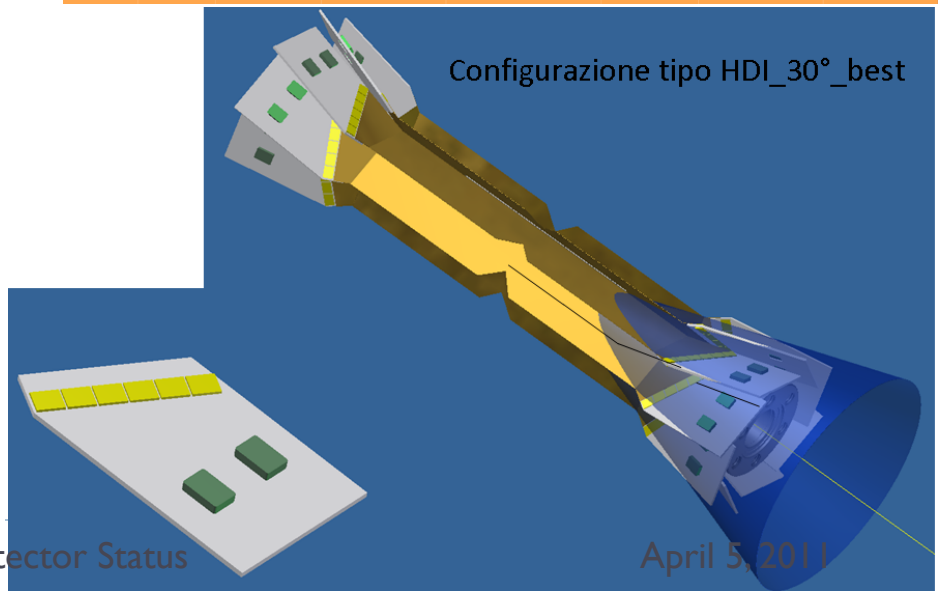
FE chip for strips from pixel architecture



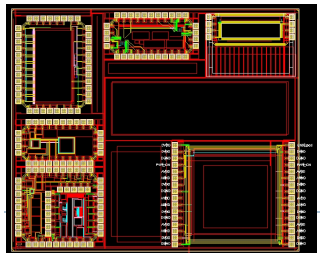
Main progress on SVT baseline (II)

- First estimate of noise performance for strip readout channel
  - realistic inputs for C, Rs, shaping time have been evaluated
- More realistic design of Layer0 striplets module:
  - Mechanical constraints quite tough
  - HDI design challenging
    - small, 6 chips, many output lines/chip
  - FE chip development needed
- Important to (re-)evaluate real cost/benefit of having striplets vs hybrid pixel installed at T_0.

Layer	C_D [pF]	available t_p [ns]	selected t_p [ns]	ENC from R_S [e rms]	ENC [e rms]	Hit rate/strip [kHz]	Efficiency 1/(1+N)
0	11.2	25, 50, 100, 200 (or 150)	25	220	**740**	2060	0.890
1	26.7		100	460	**940**	268	0.940
2	31.2		100	590	**1100**	179	0.959
3	45.8	400, 600, 800, 1000 (or 500 and 1000)	400	520	**980**	52.5	0.952
			500	470	**920**		0.940
4	52.6		500	490	**1000**	21.9	0.974
			600	440	**940**		0.969
5	67.5		800	560	**1090**	18.7	0.965
			1000	500	**1030**		0.957



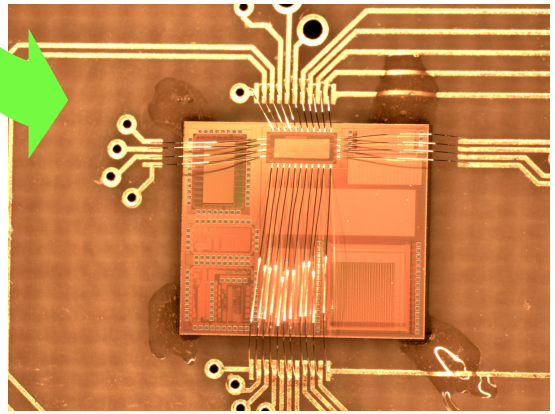
First results on MAPS from Chartered/Tezzaron process



Sensor + analog tier

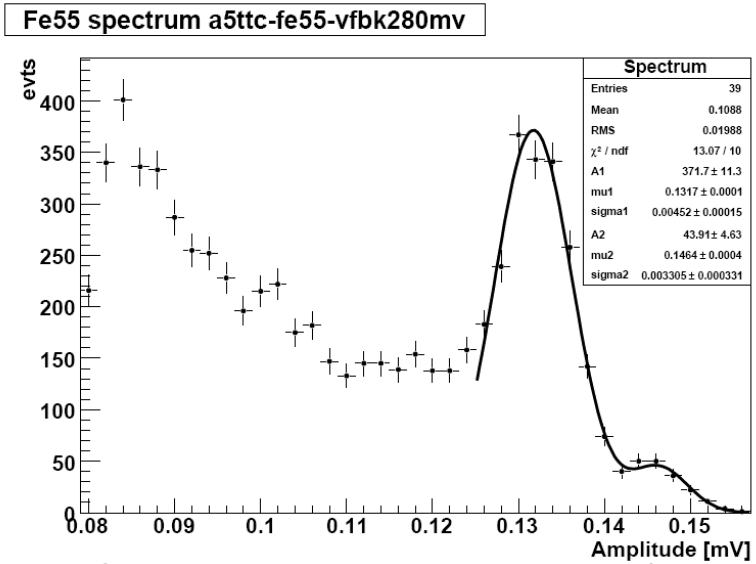
Digital tier

- 2D MAPS now available with the same CMOS process used for vertical integration of 3D MAPS
  - Now in test sensor+analog tier only!
  - First important results for the characterization of the process
- Still waiting for 3D wafers



Preliminary

- Noise ~ 4mV
  → ENC ~ 50 e-
- Calibration with Fe55
  - Gain ~ 500 mV/fC from 5.9 keV peek.
- First estimate of MIP signal from test with Sr90 ~ 800 e-



DCH

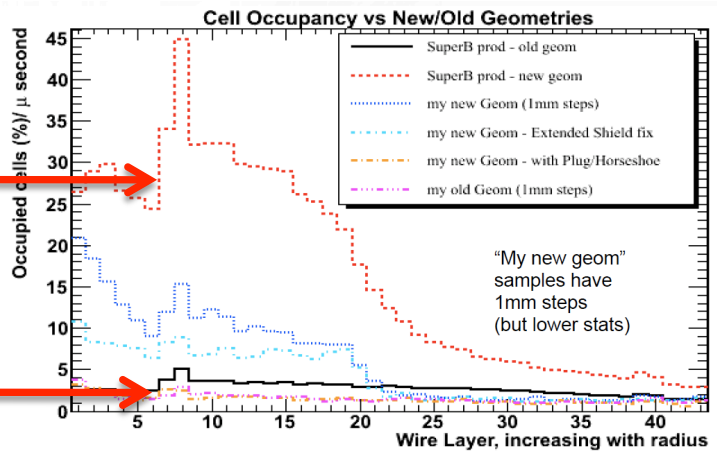
Giuseppe Finocchiaro and Mike Roney

Backgrounds

- Problem of very high DCH background rates in recent Bruno productions
  now solved!

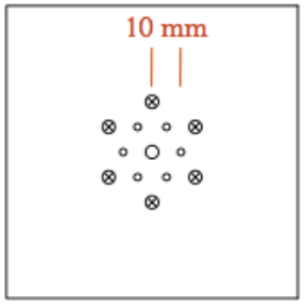
From here

To here



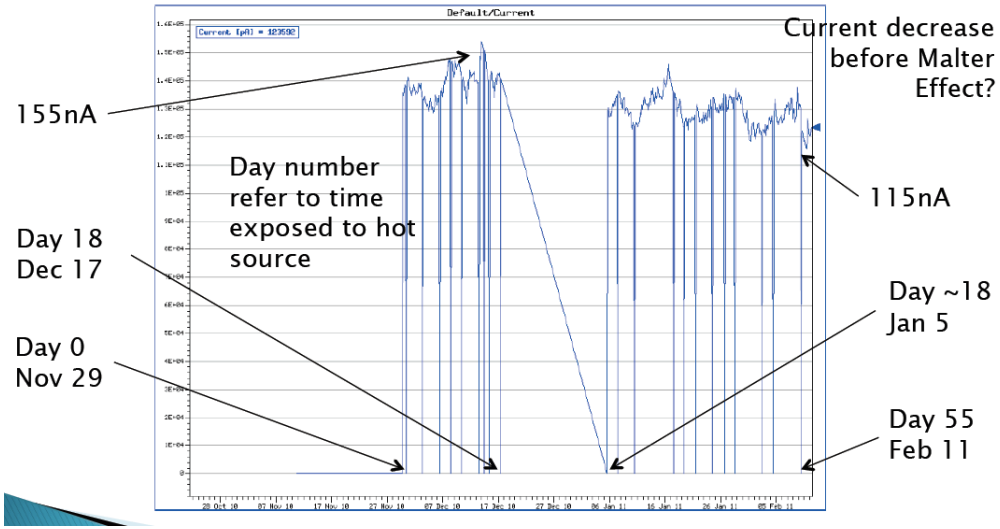
  - End plug +"horseshoe" included in the simulation, extended Tungsten shield
- Issues which still need to be addressed
  - *Safety factor?* Validation e.g. with KLOE background data?
  - Touschek contribution to be inserted in Bruno

Aging studies

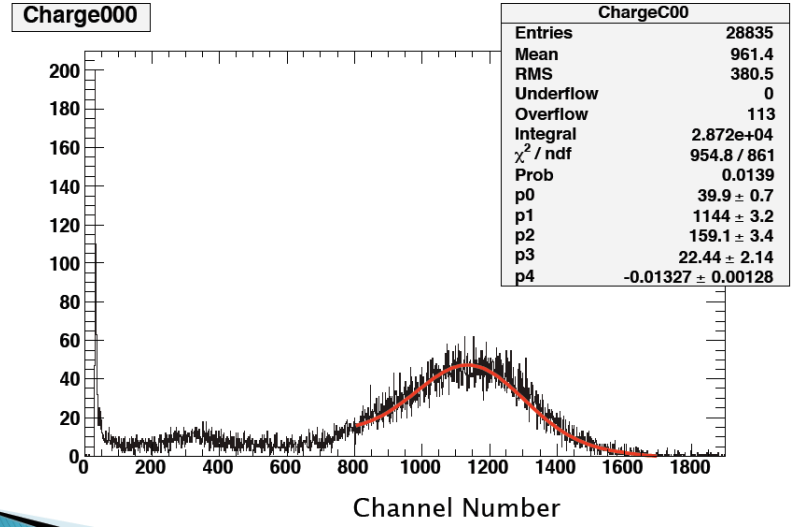


- Age chamber with a 100 mCi 55Fe source; measure 55Fe spectrum with a low-intensity source
- Monitor current, 55Fe peak location (gain), and ratio of small pulses to 55Fe interactions
  - Number of small pulses increase as Malter effect sets in.

Sense Wire Current with Hot Fe55

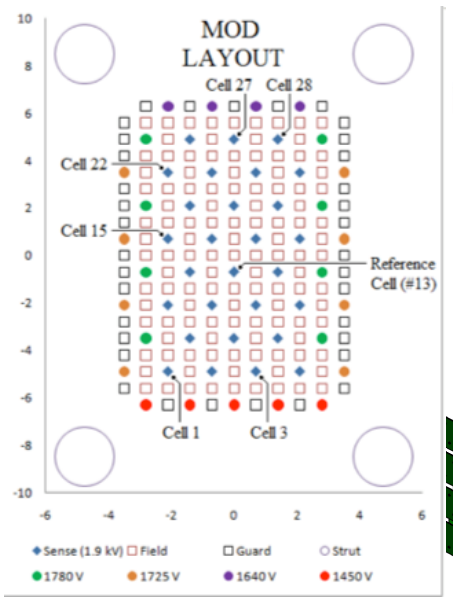


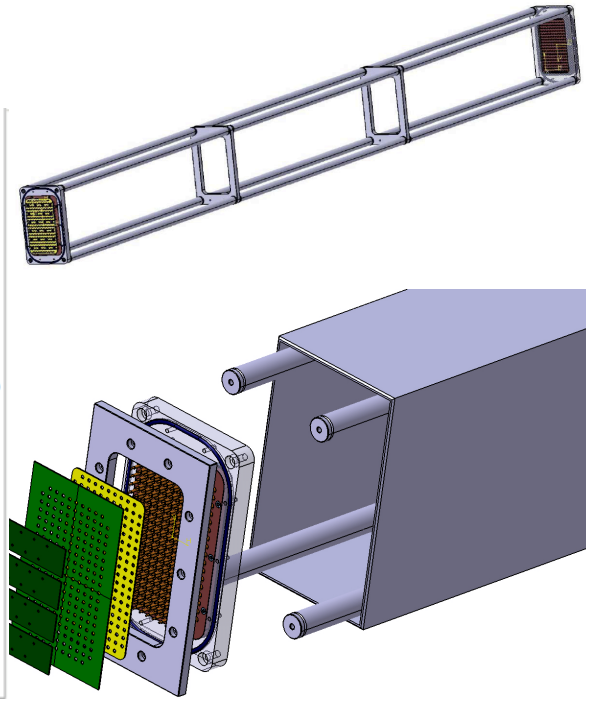
Fe55 Spectrum (Lower Activity)

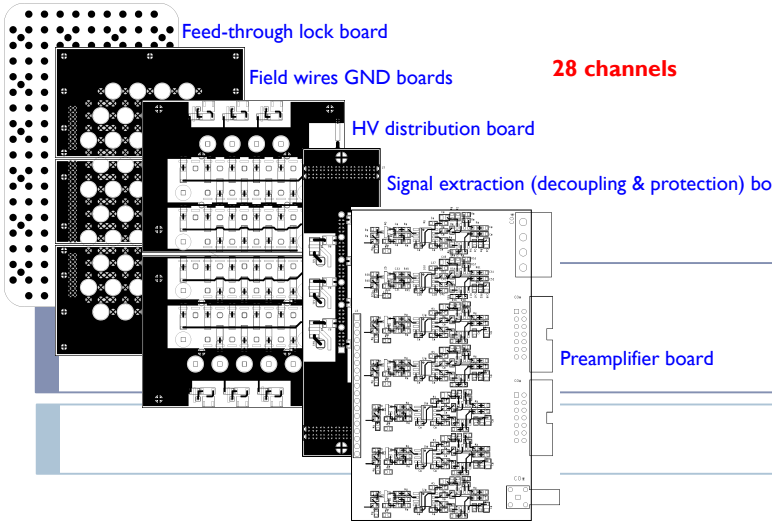


Prototype 2

- Building 2.5m long prototype with 28 sense wires arranged in 8 layers
  - study DCH response from single clusters in a realistic environment, and serve as a test bench for the final FEE

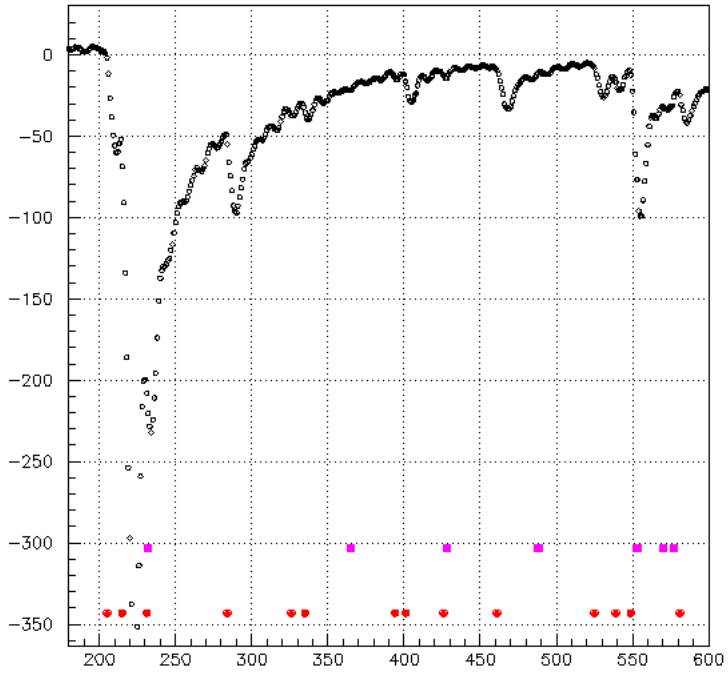


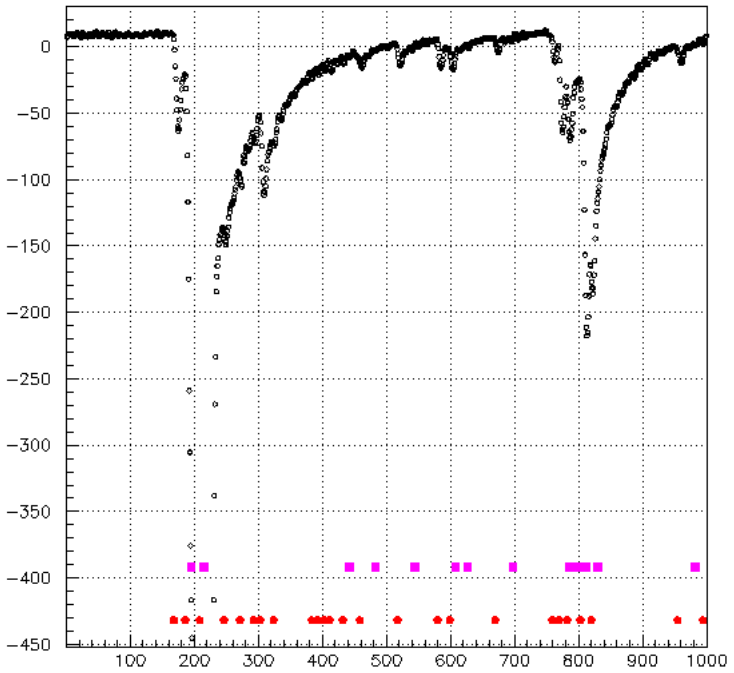




Cluster Counting in square drift tube

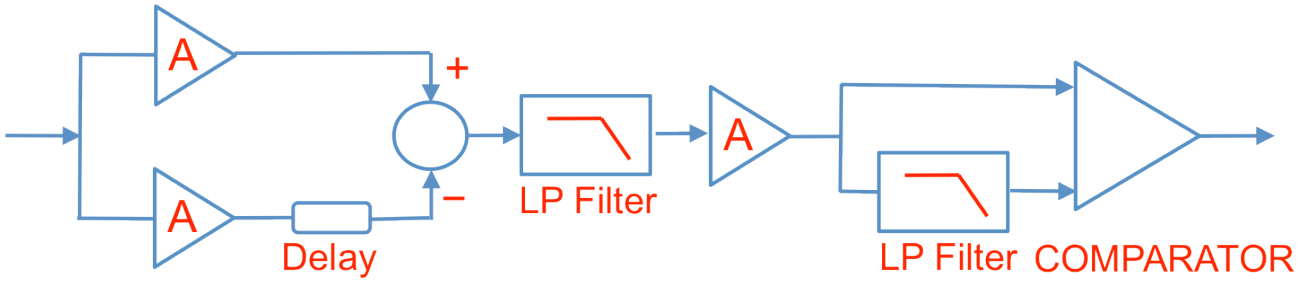
- Continuing studies of cluster counting in 30mm square drift tubes

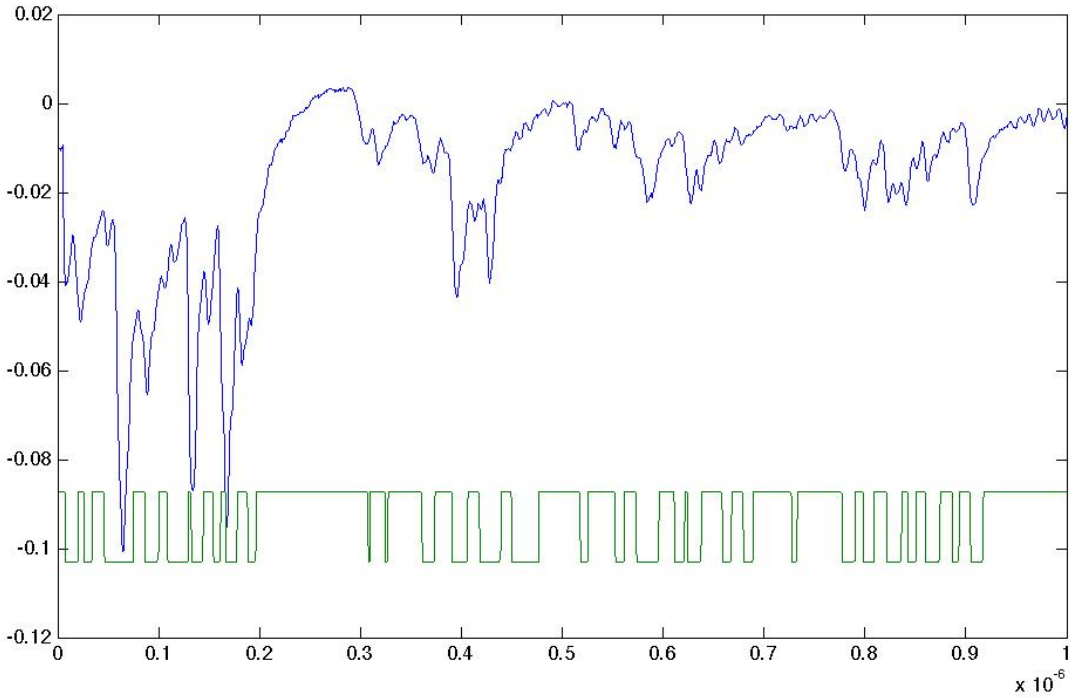




- Time of clusters from full waveform analysis
- Time of clusters from "analog derivative" method (delayed by ~50ns)

Improved Cluster Counting circuit





- Studies to verify Cluster Counting capability with analogic derivative circuit are going on.
- The method will be extensively tested on the 28 channel DCH prototype.

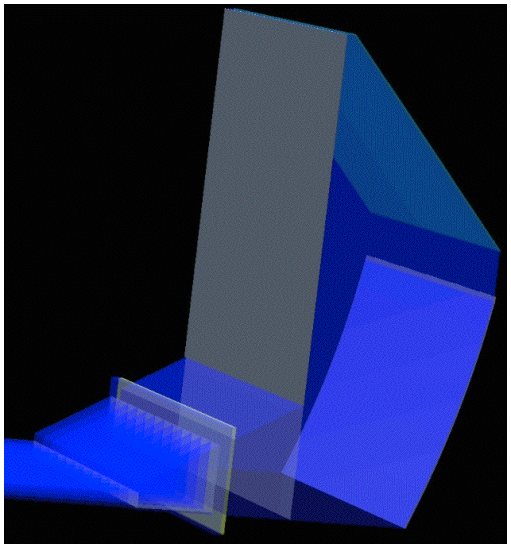
PID

Nicolas Arnaud and Jerry Va’vra

Barrel PID

- **FBLOCK & New Wedge** [SLAC]
  - Cosmo Co. has started to process of machining & polishing of the optical pieces.
  - New Wedge is expected to be finished by May.
  - FBLOCK is expected to be finished by June.
  - We are ~2 months late compared to original plans. More clear picture by Elba.

- **FDIRC optical coupling studies** [SLAC]
  - Developed a procedure to make a large optical couplings.
  - Measured transmission of all glue candidates.
  - Measuring yelowing under a large dose of photons and radiation damage effects.
  - This part seems to be under control and within the original schedule.



- **FDIRC Mechanics** [Padova + Bari + SLAC]
  - Dummy FBLOCK & New Wedge is being produced (Bari).
  - Detailed mechanical drawings almost ready to start cutting metal (Padova, Bari).
  - Detector holder concept defined. It will be produced at SLAC.
  - Method to generate the laser calibration defined (SLAC, Maryland, Padova).
  - We hope to freeze mechanical drawings by the end of this meeting and start cutting.
  - We are ~2 months late compared to original plans.

Barrel PID

- **H-8500 Detectors** [SLAC + Hawaii + Maryland + Bari]
  - SLAC scanning setup re-started. It uses old LeCroy Disc/TDC electronics presently.
  - It is going to be used to qualify 14 H-8500 detectors for CRT tests.
  - The scanning setup will be upgraded later on for the BLAB3 electronics.
  - Similar scanning setups are being prepared in Maryland and Bari.
  - Should be able to finish the detector qualification by summer.

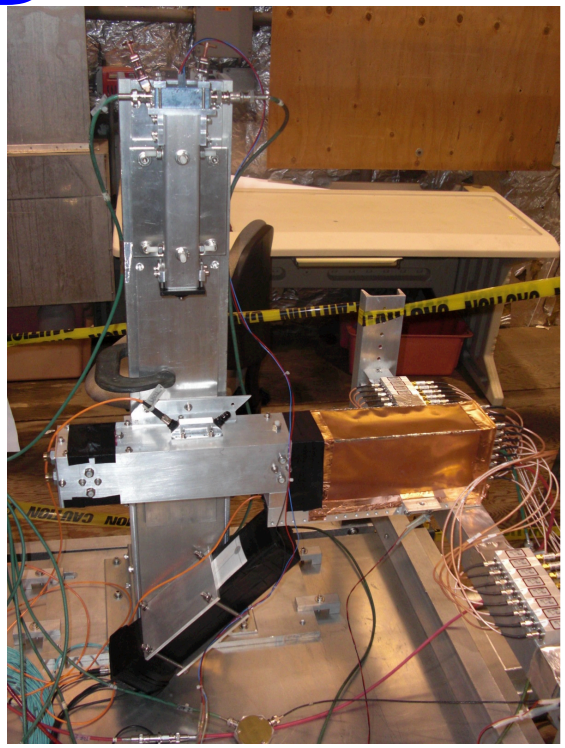
- **Electronics** [Hawaii + LAL-Orsay + LPNHE-Paris]
  - Will start the prototype with BLAB3 electronics. Gary has promissed 7 double-units.
  - LAL-Orsay electronics will be available in 2012:
    - Front-end chip and SCAT (100 ps TDC) status: work has started and they applied for a 450 kEuros grant to fund the development of the boards -- decision to be known by the Elba meeting probably

- **Definition of tasks/schedule**
  - Detailed schedule for building of the FDIRC prototype exists.
  - Search for participating institutions to take full responsibility continues.

- **New collaborators**
  - Continue to work on this issue.

Forward PID

- **FARICH** [Novosibirsk]
  - Test beam in progress.



- **DIRC-like TOF (FTOF)** [LAL-Orsay + SLAC]
  - Large data sample collected in CRT telescope.
  - Leonid will present results of his analysis in this meeting
  - Detailed MC simulation has been developed to understand the CRT data

- **A simple pixilated TOF using a LYSO crystal + G-APD** [SLAC]
  - CRT tests yielded a poor timing resolution with a full size LYSO crystal (σ~220ps).
  - There will be one more CRT test at SLAC, but it seem unlikely that one can achieve σ~100ps.

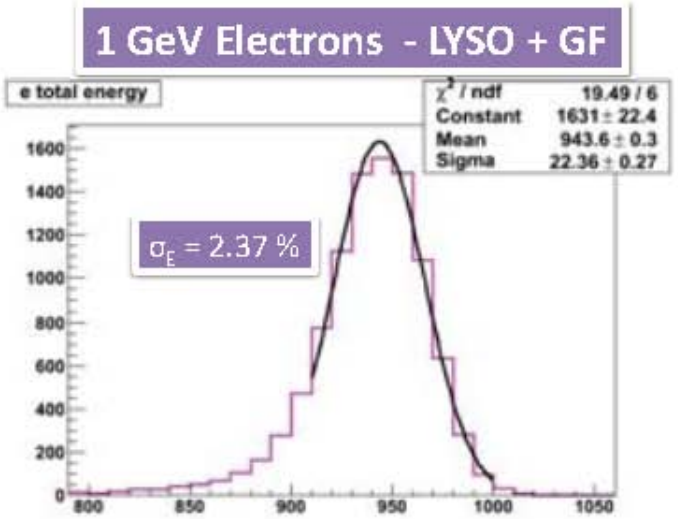
EMC

Claudia Cecchi and Frank Porter

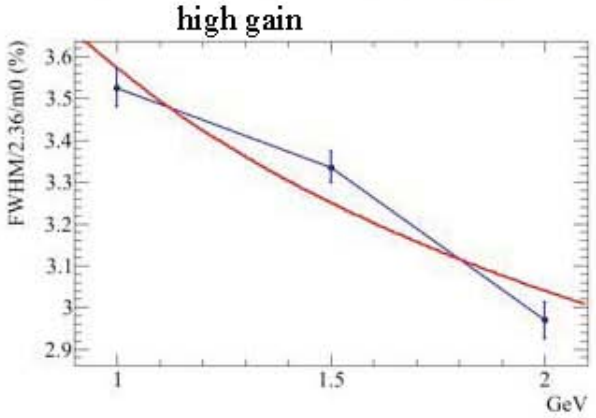
CERN test beam status

Analysis ongoing
Resolution poorer than expected from simulation
Ruled out various possible sources
Remaining ideas:

- CERN T10 beam spread larger than advertised
- Crystal uniformity not good enough



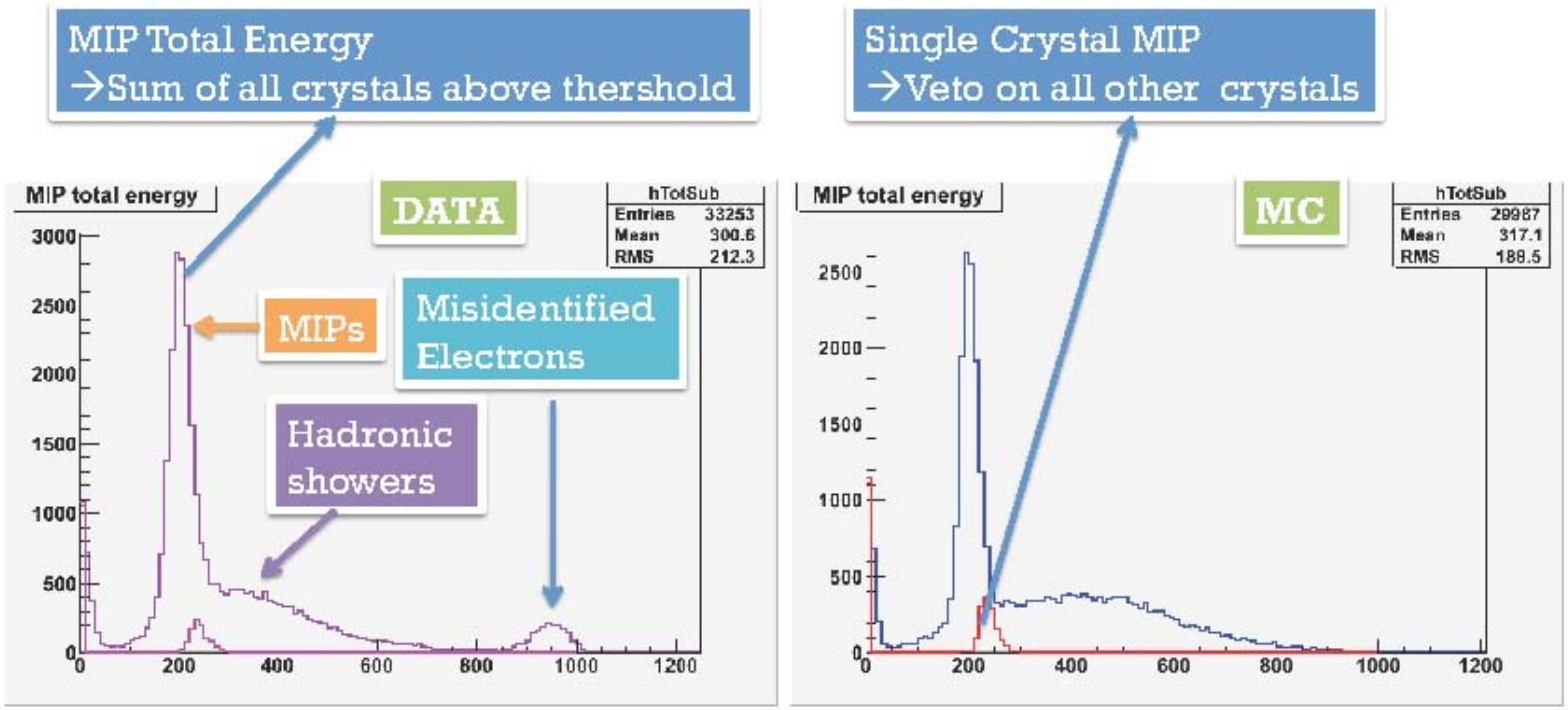
MC



data

CERN test beam status - pions

Pi : All X vs 1 X



DATA have smaller fraction of MIPs with only one crystal
Hadronic shower energy is different between DATA and MC

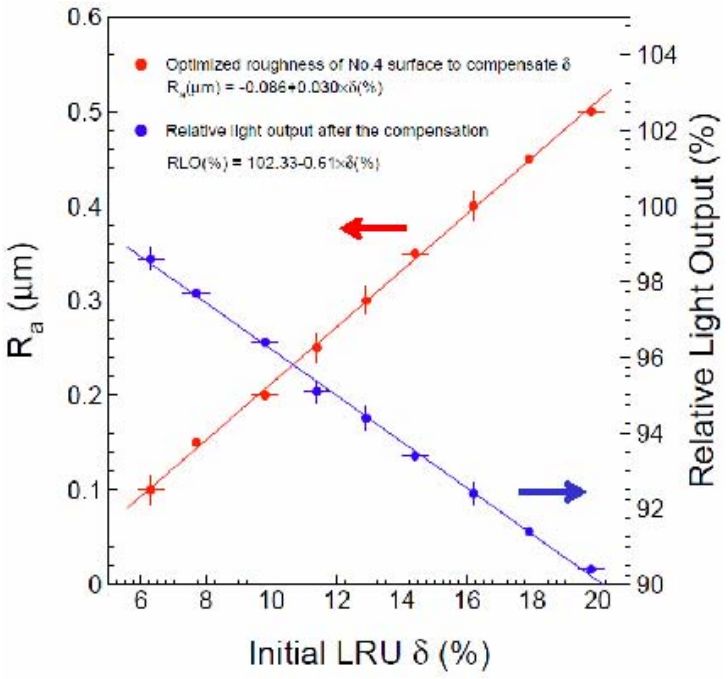
Plan for future LYSO test beams

- Test beam at Frascati in May with CERN configuration
- Test beam with further optimized array at Frascati, probably September
  - 2 APDs per crystal (this is proposed design)
  - Crystal uniformity by roughening a face
  - Source calibration of crystals
  - Electronics, APD gain optimized
- Discussions with Carsten Hast about possible tagged-photon test beam at SLAC

LYSO Crystals

- Three vendors make large LYSO(Ce) crystals, SIC, SIPAT, Saint-Gobain
- Developing improved method for uniformization of tapered crystals:

- Test beam uniformization was with black ink band on crystal, costs $\sim$ 40% in light for $\sim$ 5% uniformity
- Investigating uniformization by roughening a crystal face
- Simulation very promising, can correct to better than 5% with few % light loss
- Trying on a real crystal



Simulations

- Fastsim did not include energy smearing for neutrals in September production
  - May affect results for backward EMC studies
- Developed algorithm for applying smearing to ntuples without redoing production (Elisa Manoni)
- Preliminary result shows ~40% decrease in $\delta(S/\sqrt{B})$ in $B^0 \to K^{*0}(K\pi)\nu\bar{\nu}$ compared with non-smeared analysis

NO SMEARING

$$\delta\left(\frac{S}{\sqrt{B}}\right) = \frac{\left(\frac{S}{\sqrt{B}}\right)_{bwd} - \left(\frac{S}{\sqrt{B}}\right)_{nobwd}}{\left(\frac{S}{\sqrt{B}}\right)_{nobwd}}$$

$$= (10.9 \pm 3.1)\% \quad (K\pi)$$
$$= (5.9 \pm 2.3)\% \quad (K_s\pi)$$
$$= (7.8 \pm 4.2)\% \quad (K\pi^0)$$

SMEARING

$$\delta\left(\frac{S}{\sqrt{B}}\right) - \frac{\left(\frac{S}{\sqrt{B}}\right)_{bwd} - \left(\frac{S}{\sqrt{B}}\right)_{nobwd}}{\left(\frac{S}{\sqrt{B}}\right)_{nobwd}}$$

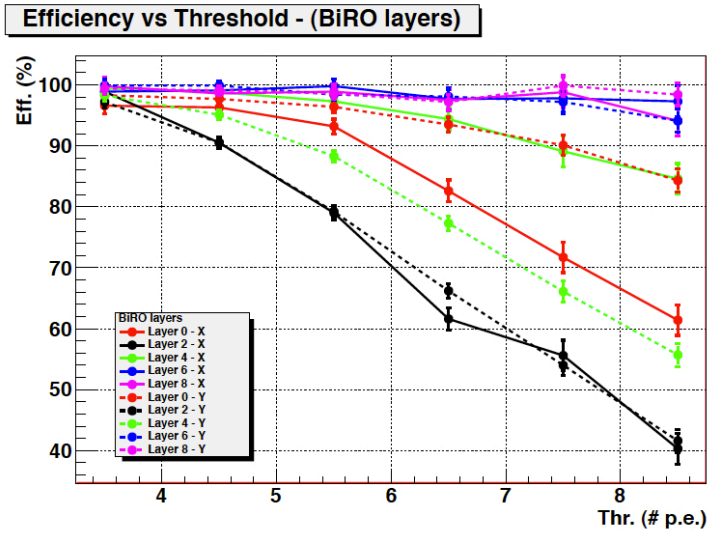
$$- (6.5 \pm 2.2)\% \quad (K\pi)$$
$$- (3.2 \pm 1.5)\% \quad (K_s\pi)$$
$$= (4.5 \pm 3.2)\% \quad (K\pi^0)$$

IFR

Roberto Calabrese

Advancements since Caltech:

- Prototype tested (1-7 Dec 2010) at the Fermi Test Beam Facility (Meson Area)
- **9 layer configuration tested with different readout schemes (5 BiRO layers and 4 TDC lay**
- Beam Test Data analysis ongoing
- Prototype shipped back and reassembled in Ferrara (no Iron) to continue the test with cosmics
- New Beam Test foreseen next summer



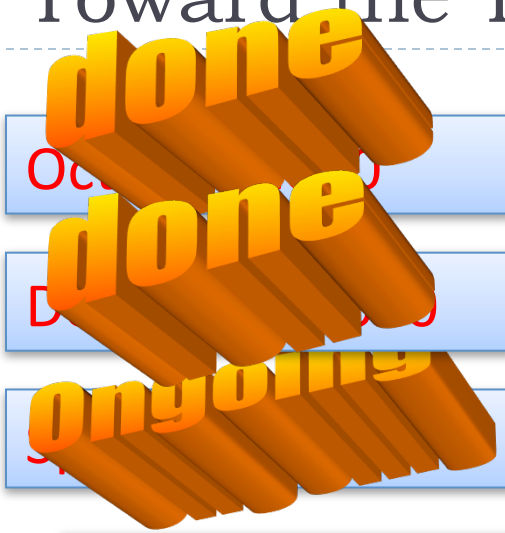
Goals for this meeting:

- ***Review advancements and achievements*** in all the development areas

- ***Particular focus on beam tests:*** analysis of the December data and preparation for the new summer beam test

- ***Analyze the TDR preparation*** process and prioritize the short and medium term activities

Toward the TDR



- ***test prototype with cosmics***
- ***first beam test @ FNAL***
- ***analyze/review test results***
- ***new beam test @ FNAL***
- ***analyze/review new test results***
- ***write TDR***

Summer 2011

Fall 2011

Winter 2011

ETD/Online

Dominique Breton, Umberto Marconi, Steffen Luitz

ETD (1)

- Since Caltech, we had a two-day ETD workshop at CERN end of February
  - All groups were represented => discussions were very effective
  - Good progress was done on putting numbers in dataflow and refining the trigger strategy on the front-end

  ⇒ Guidelines for next milestones were defined

  ⇒ Trigger studies really got started

- We will have 3 sessions during this workshop:
  - one concerning front-end electronics
  - one concerning common items
  - one dedicated to hardware trigger

- During the two last sessions, we would like to discuss the following points:

- Clock and control links:
  - Irradiation of the event data SERDES chipset was performed => results will be presented by Raffaele
  - We have to define plans to start qualifying components of the optical layer
  - The use of mezzanines vs firmware blocks has to be discussed again for the FCTS and ROM sides

ETD (2)

- ROM: new steps were made in understanding the solution to be described in the TDR.
  - We have to refine the ratio price/performance/flexibility of the different solutions.
  - A few presentations on these subjects will take place this week.

- Common Front-End Electronics: first simulations of the front-end derandomizer in order to be able to estimate its adequate depth will be presented

- Trigger:
  - Separate front-end parameters for trigger and event readout (e.g. in the EMC, different shaping times for trigger and event readout) were studied

    => What is the achievable time precision for the trigger primitives?
  - New solutions were presented to extract the trigger primitives from the front-end
    - We would like to standardize the philosophy of the primitives between DCH and EMC
    - EMC primitives could be transmitted on LVDS copper pairs (DCH?)

    All these subjects will be analysed in view of the TDR writing.

Agenda

SuperB Workshop

Frascati (Italy)
April 4 - 7, 2011

All Plenary Sessions will be held in Sala Touschek

Meeting Registration Desk: Monday, April 4, 10:00

Standing Cocktail Reception and guided visit to Villa Grazioli: Tuesday, April 5, 19:30

	Monday, April 4		Tuesday, April 5		Wednesday, April 6th		Thursday, April 7th
	PO Meeting	9:00	PLENARY	9:00	PARALLEL 5	9:00	PLENARY
		10 20 30 60	Welcome Project Status Physics Theory Seminar (Ali)	Tou Seminari	Det Geometry Task Force (open) Computing: Planning		MDI SVT DCH PID EMC IFR ETD
10:00	*Registration*	11:00	*Coffee Break*	11:00	*Coffee Break*	11:00	*Coffee Break*
11:30	PO Meeting	11:30	PLENARY	11:30	PARALLEL 6	11:30	PLENARY
Seminari	TechBoard	30 30 30	Accelerator Detector Computing	Tou B-1 Seminari	Det+Comp: BG + FullSim DG Task Force (closed) Physics: Other Experiments		Forward PID TF Backward EMC TF Comp Collaborative Tools Physics
13:30	*Lunch*	13:30	*Lunch*	13:30	*Lunch*	13:30	*Lunch*
15:00	PARALLEL 1	15:00	PARALLEL 3	15:00	PARALLEL 7	15:00	
Tou Calcolo B-1 A-1 Seminari Conversi	SVT DCH PID EMC IFR Comp R&D + TDR	Tou Seminari B-1 A-1	Det: ETD 1 Physics: Charm Comp: Collab Tools Det: Background	B-1 Tou Seminari	Det: Integration + MDI Det: ETD 3 Physics: TDR Organization	Direzione	Detector Tech Board
16:30	*Coffee Break*	16:30	*Coffee Break*	16:30	*Coffee Break*	16:30	*Coffee Break*
17:00	PARALLEL 2	17:00	PARALLEL 4	17:00	PARALLEL 8	17:00	
Tou Calcolo B-1 A-1 Seminari Conversi	SVT DCH PID EMC IFR Distributed Comp Tools	Tou Seminari	Det: ETD 2 Det+Comp+Physics: FastSim	Tou Calcolo B-1 A-1 Seminari	SVT DCH PID EMC IFR	Direzione Direzione	Steering Committee Project Board
18:30		18:30		18:30		18:30	
		19:30	*Standing Cocktail Reception and guided visit to Villa Grazioli*				

Room Codes		*Conf. #*		*Room Codes*		*Conf. #*	Telephone numbers for all calls at:
Tou	*Touschek - bldg 36*	1550		*B-1*	*Aula B-1 - bldg 36*	1553	*http://server10.infn.it/video/index.php?page=telephone_numbers*
Seminari	*Aula Seminari - bldg 36*	1551	*Aula Direzione - bldg 1*	*Calcolo*	*Aula Calcolo - bldg 14*	1554	
A-1	*Aula A-1 - bldg 36*	1552		*Conversi*	*Aula Conversi - bldg 57*	1555	

Workshop focus

- Review ongoing R&D and detector design
  - Increase mechanical integration effort
- Focus on issues to be resolved for TDR
  - Forward and backward geometry – tentative plan to take a decision in Elba.
  - Many more issues in the subsystems
- Advance understanding of backgrounds
  - Dominate detector design in many areas
- Recruit new collaborators
  - Prepare for the First SuperB Collaboration Meeting in Elba

The SuperB Pisa group is happy to announce that the **1st SuperB Collaboration Meeting** will take place in La Biodola, Isola d'Elba, May 28th to June 2nd.

Lying only 10 km from the mainland, Elba is the largest island in the Tuscan Archipelago and has become an internationally famous tourist resort. It offers a large number of attractions, hiking and climbing itineraries, bike trails and wonderful beaches. The excellent accommodation structures make it an ideal place to merge together, work, study and relax.

Click here for a Google map of the meeting site with information

The Registration will open on Thursday, April 7th and the deadline is **Sunday, May 15th**. Registration form and logistic information are linked from the left menu.

Meeting sessions will start in the morning of **Sunday, May 29th** and finish in the evening of **Wednesday, June 1st**.

Participants are expected to arrive on Saturday, May 28th and to leave on Thursday, June 2nd.

Technical Board, Accelerator Board, Project Board and Steering Committee will take place on Thursday, June 2nd, and the attenders are expected to leave on Friday, June 3rd.

http://agenda.infn.it/conferenceDisplay.py?confId=3352

Backup

SVT - Next R&D on pixel for Layer0

- Improvements in MAPS performance being pursued with:
  - **INMAPS CMOS process** with quadruple well + high resistivity substrate: higher charge collection efficiency & rad hardness → **design of first prototypes ongoing**
  - **3D MAPS** with 2 CMOS tiers interconnected:: higher cce efficiency, more complex in-pixel logic, reduce cross-talk → **first chips under test, testbeam in Sep. 2011**
- Improved readout architecture developed for pixel with Vertical Integration
  - TimeStamp is latched in each pixel when fired & readout is time ordered.
    - Timestamp granularity 100 ns
  - Readout could work in data push mode & triggered mode
    - VHDL results for 100MHz/cm2 hit rate: Effi_triggered=98.2%, Effi_data_push=99.9%
  - **New submission of large 3D MAPS and FE chip for Hybrid pixel (2-tiers), with the improved readout architecture, in preparation for mid 2011**
- Vertical interconnection of FE chip (2-tiers) with high resistivity pixel matrix (best technology under investigation) will give the best performance: high S/N and radiation hardness, low power and material budget