Update on new prototype(s) @ LNF

DCH-III parallel session

LNF 6 Apr 2011

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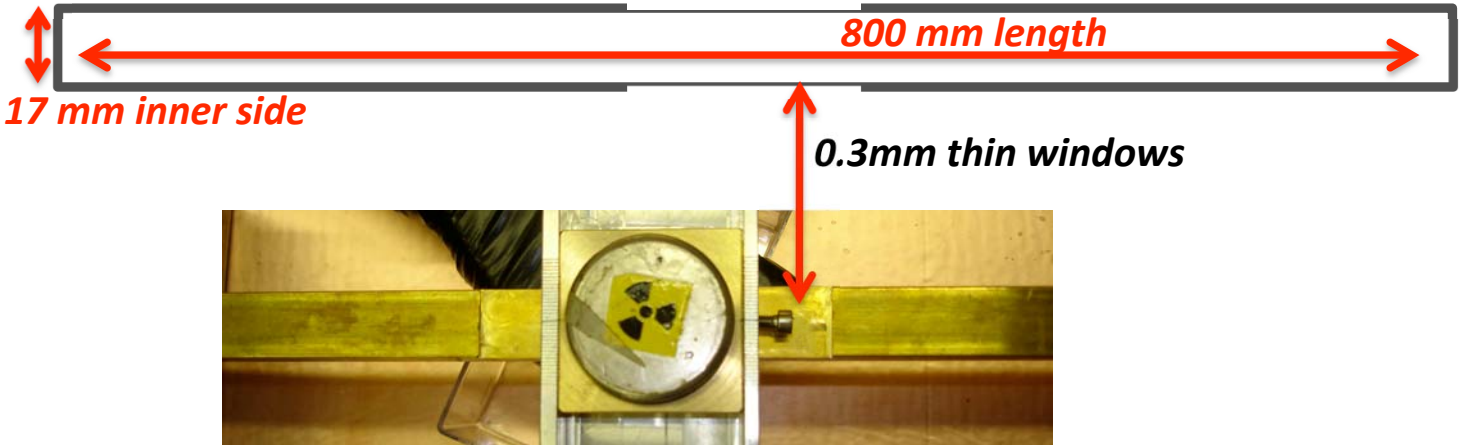
A new, smaller drift tube

- Motivations:
  - maximum time window of our DRS4 digitizer evaluation board is 1μs @1Gs sampling frequency
    - marginal with 30mm-side tube and medium-speed mixtures
    - now using a brass square tube with inner side of 17mm
  - Al-Mylar windows of previous tubes not 100% gas tight after some time
    - "transparent window" on 1.5mm thick tube now obtained milling two opposite sides down to 300μm thickness



A new, smaller drift tube (cont.)

- Using 25 μm Au-plated Mo wire in this tube for the first time
- Molybdenum has lower resistivity (less signal losses), possibly beneficial for cluster counting
  - Measured $R_{80cm}=94\Omega$ consistent with specs from Luma Metall

Properties of tungsten wire alloyed with 3% Rhenium

Purity of tungsten before rhenium addition	99.95% W
Melting point	3380 °C
Density	19.22 g/cm³
Specific electrical resistance at 20 °C	0.092 Ohm x mm²/m
Modulus of elasticity at 20 °C	430 kN/mm²

Properties of bare Molybdenum wire

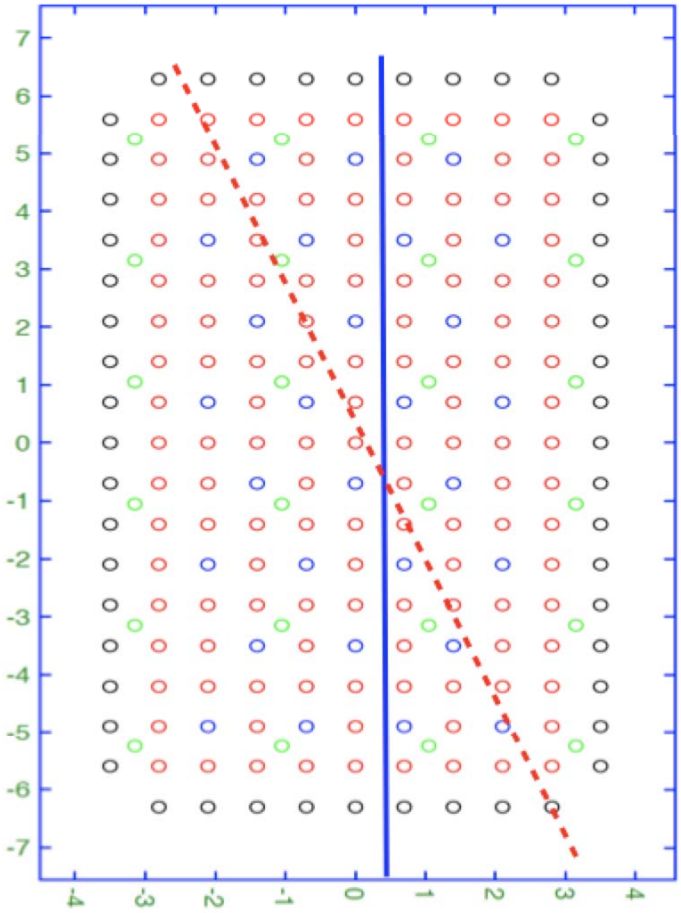
Purity	99.9% Mo
Melting point	2620 °C
Density	10.14 g/cm³
Specific electrical resistance at 20 °C	0.052 Ohm x mm²/m
Modulus of elasticity at 20 °C	320 kN/mm²

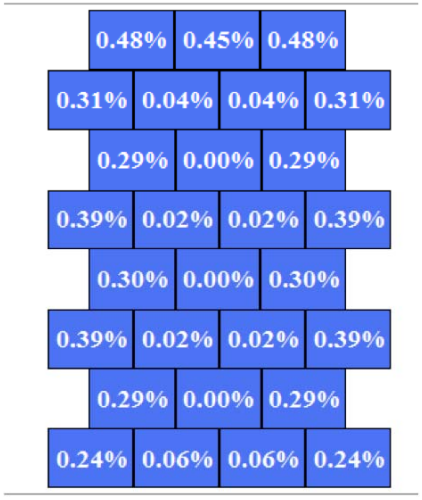
- Lower wire density:
  - 160Kg less tension on DCH endplates for 8,000 sense wires
  - Substantial decrease of material budget
  - e.g., X_0**(gas+wires)=570m for Mo** sense wires vs. **510m for W-Rh** sense wires

Status of Proto 2

REMINDER:

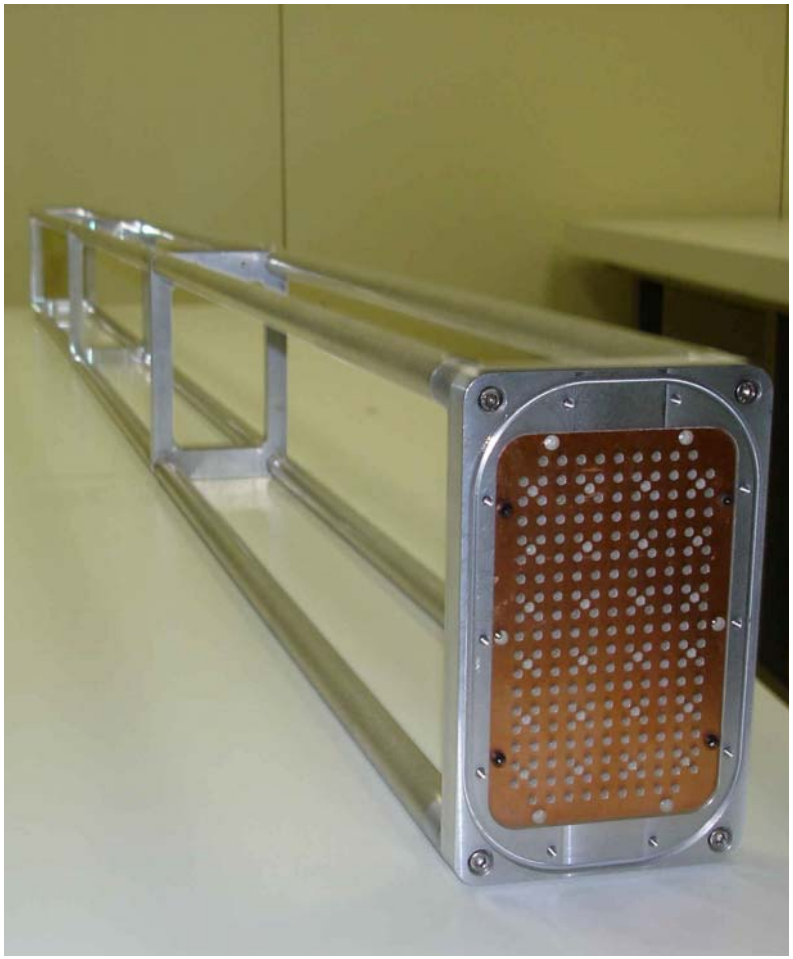
- Blue circles: 28 sense wires arranged in 8 layers (3-4-3-4-3-4-3-4)
  - Tracks with $\vartheta \in [-20,+20]^{o}$ cross all layers
- Red circles: field wires
- Black circles: External layer of guard wires to make cell response homogeneous
  - Optimization of wire positions and HV By Philip Lu
- Green circles: blind threaded holes for support of FEE boards





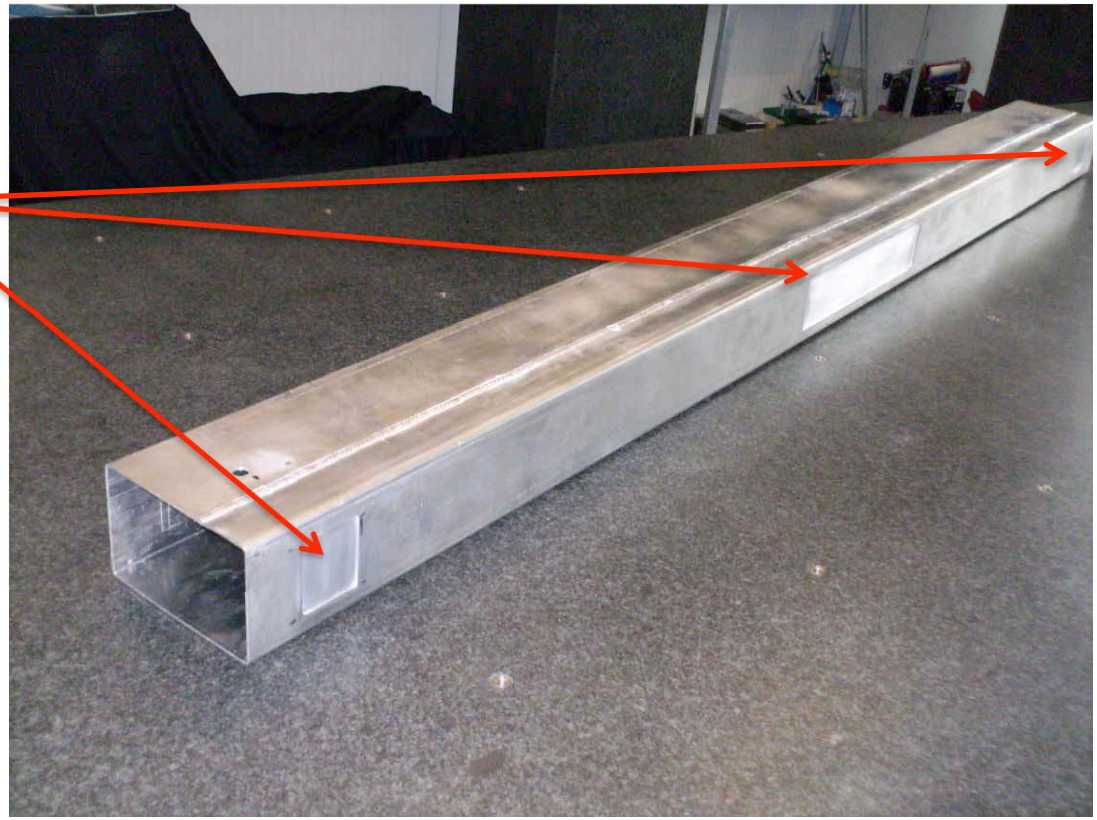
Status of Proto 2

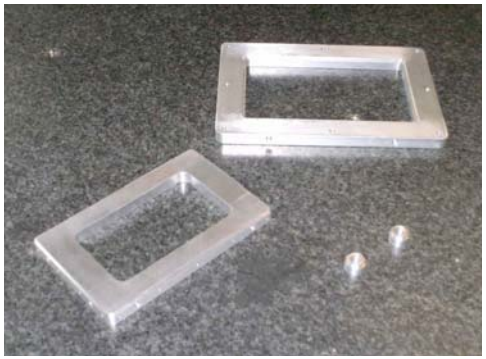
- Mechanical structure now complete
- Clean room is operational
- All material for stringing is in place
  - Idea is to use Mo wire for most of the sense wires (21?), W-Rh for a few others for comparison
    - this would entail different termination resistors
  - It should take O(1 week) to string 200 wires.
  - It would be desirable to perform a gas tightness test before stringing, but the schedule for getting all the pieces in place might not let us do that (see next slide)



Status of Proto 2

- External tube is built
  - 3mm thick Al, 3 pairs of 0.3mm thick windows milled in the middles, near and far from readout electronics
  - 2 flanges to be welded on the tube ends later this week





1 additional flange for gas tightness still to be machined

VTX1742 Digitizer

- 32+2 channels, 12 bit
- Selectable 5, 2.5, 1 GS/s Switched Capacitor ADC
- 1 Vpp input dynamics
- Based on DRS4 chip (Paul Scherrer Institute design)
- 1024 storage cells per channels (200 ns recorded time per event @ 5GSample/s)
- Memory buffer: 128 events/ch
- Dead Time: 110µs Analog inputs only, 181µs Analog inputs + TR0, TR1 inputs
- Possibility of FPGA for real-time data processing (for example Zero Suppression and Data Reduction algorithms)

- Delivery from CAEN due by Apr 15

Summary

- Progress was steady, but not as fast as expected
- Beam test scheduled on May 22-28 still possible, but time is tight
- Aim to schedule a new test beam period in September 2011