SVT - Pixels
Upgrade

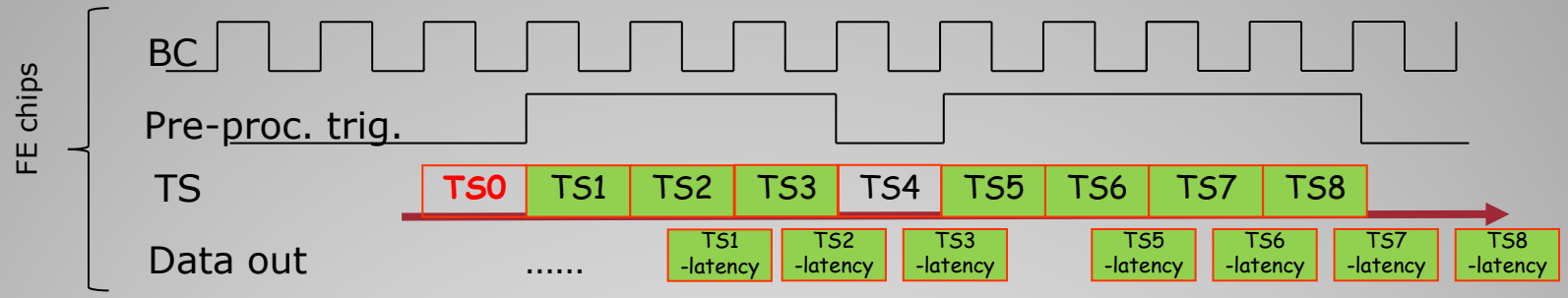
Filippo Maria Giorgi - INFN Bologna

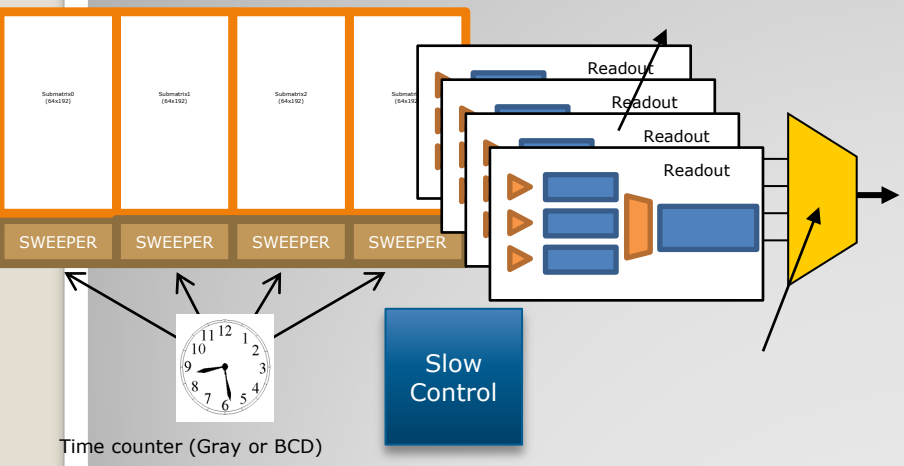
SuperB Workshop
Frascati, Apr. 4th-7th 2011

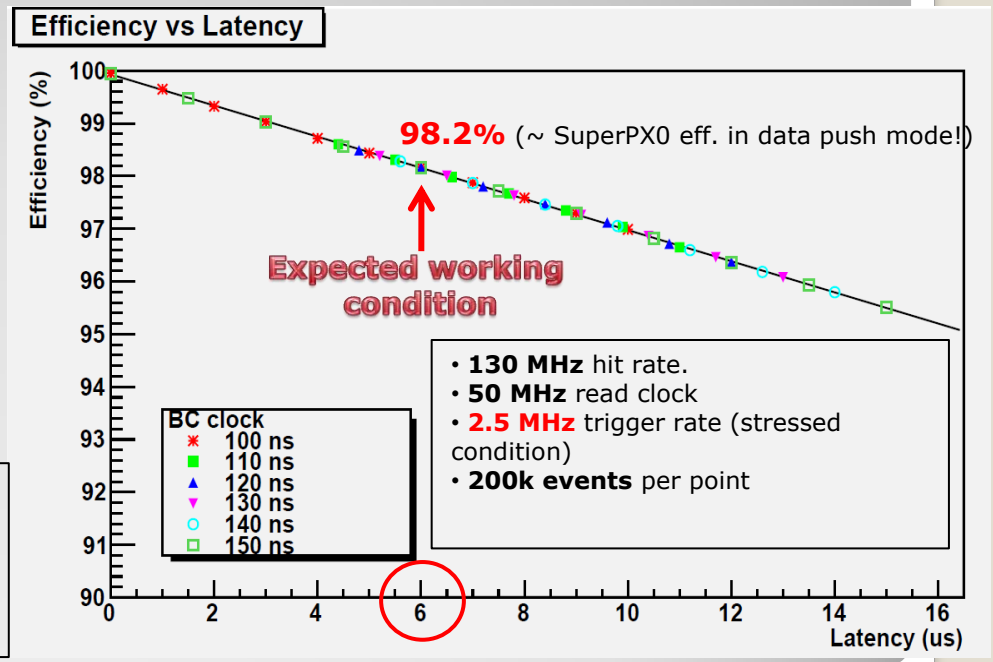
- Architecture State
- Submission Update
  - Tezzaron Chartered
  - INMAPS
- Sept. 2011 Test Beam Update
  - Firmware/software Upgrade

Summary

- Triggered/Data-push selectable working mode.

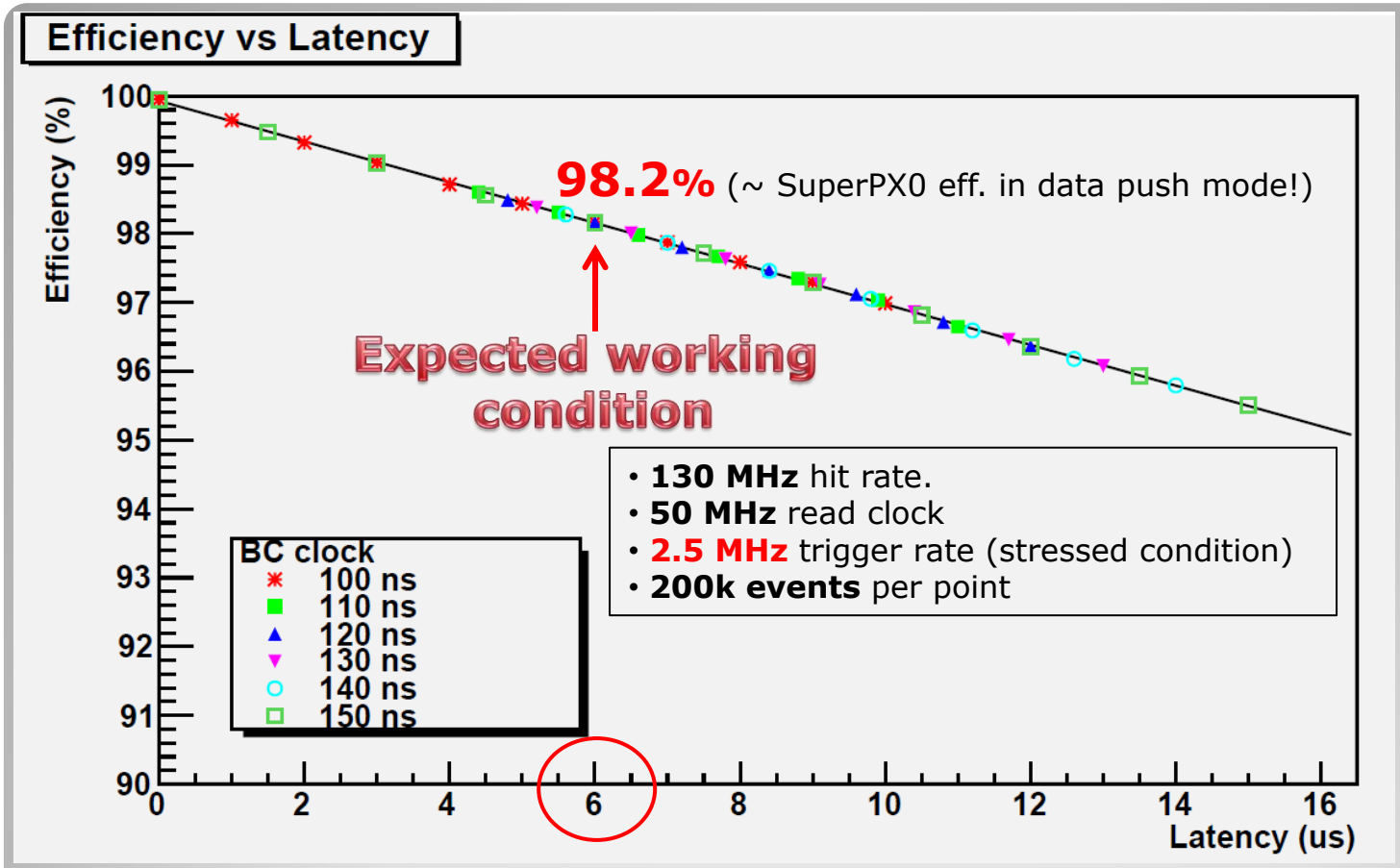






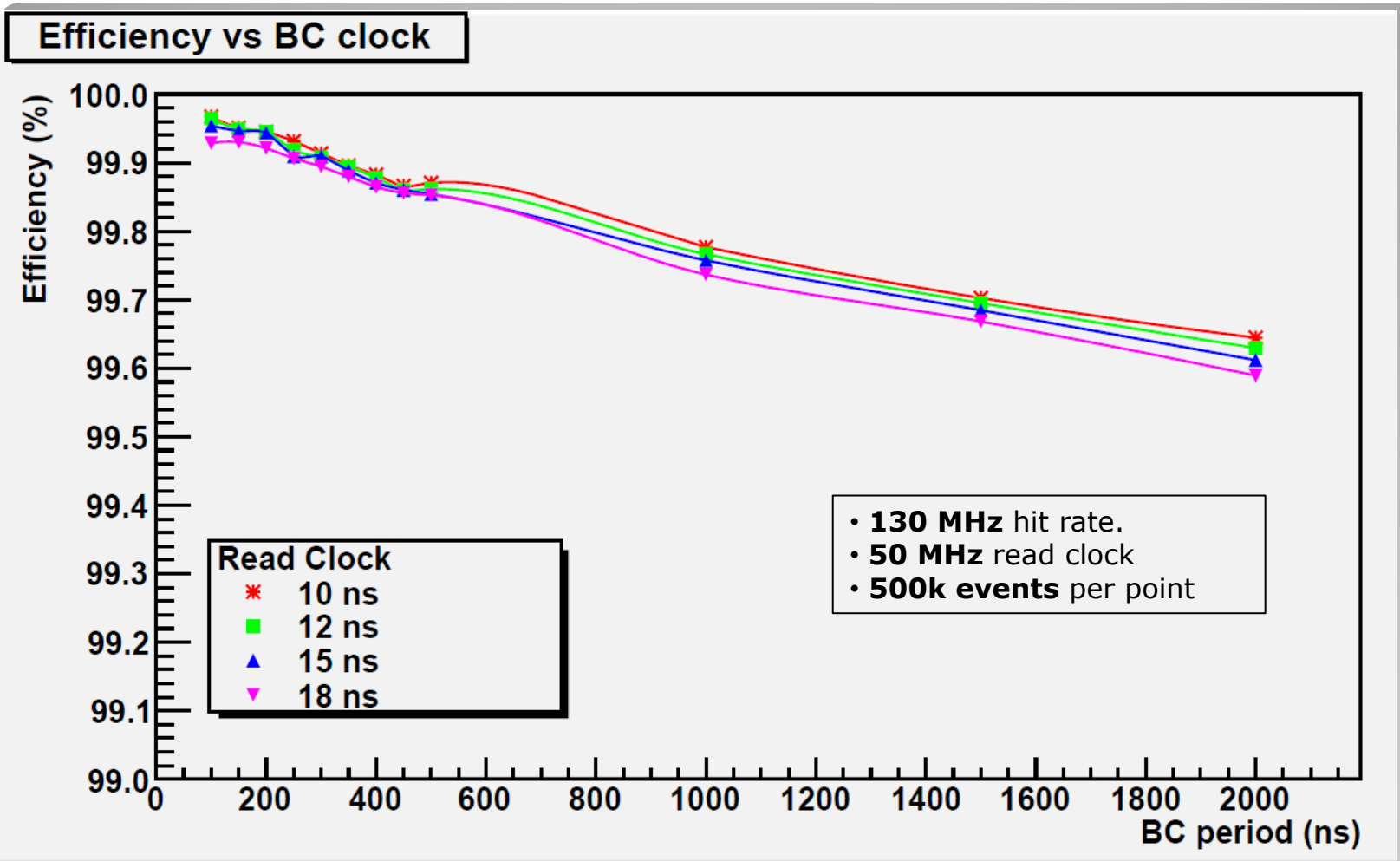
Still few functionalities to be defined and integrated (DAC bits loading into matrix)

Architecture state



- Smooth decrease of efficiency in function of trigger latency.
- Almost **no dependency** of efficiency **on BC period** (in this region)
- Linear fit slope: **-0.3 %/us**.

Simulation results, TRIGGERED



NOT taken into account:

- sensor efficiency (assumed 100%)
- pixel reset dead time (assumed few ns)

Simulation results DATA PUSH

Submissions update

Tezzaron Chartered submissions

- Architecture code has been branched:
  - APSELVI 96x96 (3D MAPS)
  - APSELVI 96x128 (3D MAPS)
  - SuperPix1 32x128 (3D Hybrid)
- Synthesis with ARM standard cells
- Synthesis exploration phase completed, timing closed @ RDclk=50MHz / fastClk=200MHz (a major revision required on Barrel1, functional integrity checked)
- Next to come:
  - Close architecture specifications/functionality.
  - Chose one APSELVI matrix size (see next slide)
  - Final synthesis → Post synth. simulations with real matrices models → Layout → post-layout simulations → sign-off.

Tezzaron Chartered AREA estimate

CHIP	N. Cells	Cells area (mm2)	RO area (mm2)
APSELVI96x96	78k	0.89	**8.71**
APSELVI96x128	102k	1.12	**11.31**
SuerPX1	68k	0.77	**7.57**

APSEL_VI (BOTH):
B1 length = 64 words
B2 length = 32 words
calibration 4 columns at a time (24 column steps = whole matrix step)

SPX1:
B1 length = 64 words
B2 length = 16 words
Calibration 2 columns at a time (16 columns steps = whole matrix step)

Submissions update

INMAPS submission

- NDA signed.
- Obtained access to the foundry cell libraries at the end of last week.
- Need to set-up the CAD tools and try to estimates the cell density/readout area with this new design-kit.

Submissions update

TEST BEAM UPGRADE

- Pixel chips supposed to be tested in September
  - **APSEL4D/4D_1**
  - **APSEL3D_TC**
  - **SuperPix0**

Few beam time, many chips → Different kinds of chip acquired simultaneously (and only one FE-side FPGA available)

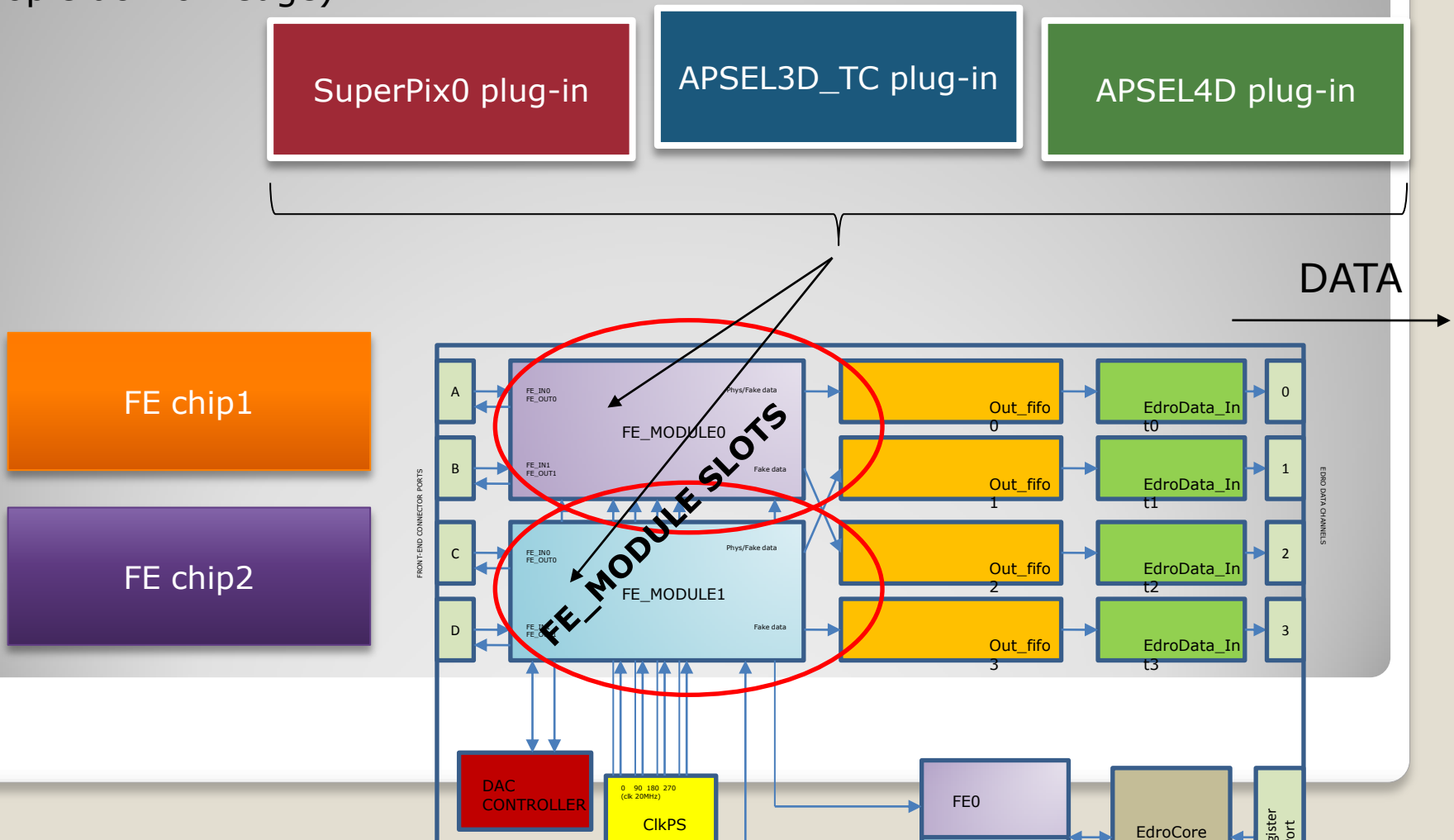
Need for a **modular project** both in **firmware** and **software** to provide the required flexibility. (Software = TDAQ & Configuration GUI)

- Re-organization of Front End control firmware to a flexible modular structure
- Software updates
  - Migration to newer TDAQ version and SLC5 almost completed.
  - New concept of FE module must be integrated.

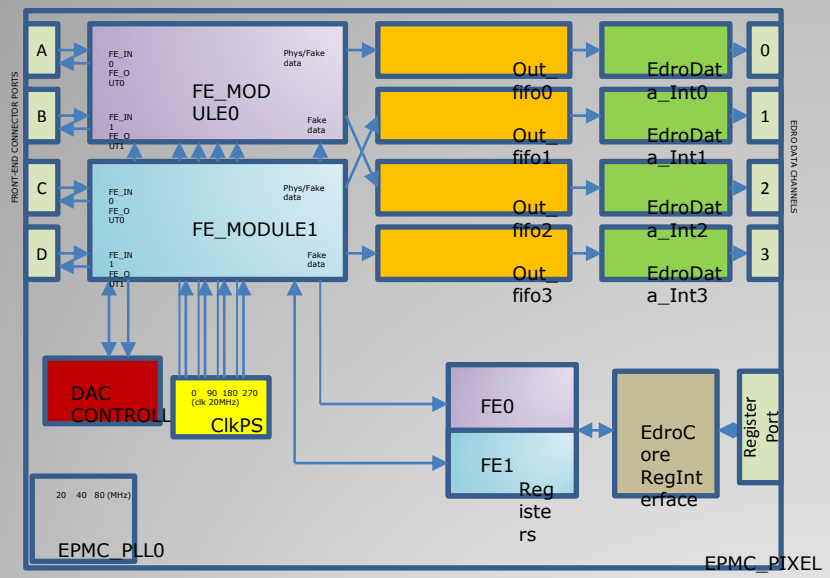
Test Beam Update

Front End Control Modules

• **Modular structure**. Shared features (DAC settings…) realized in on a common platform with **2 FE module "slots"**.
• 1 **FE module plug-in** for each FE chip. Common slot interface to platform.
• **Any mix** of pixel flavor allowed.
• Provided a simple **common hit format** outside: **xyt** bit-fields (offline people acknowledge)



DAQ UPGRADES



EDRO/VME

TDAQ

Configuration Software

Configuration file

DATA

Still to be updated for Test Beam

- Submissions
  - Tezzaron Chartered chips
    - → Synthesis exploration terminated. Timing closed and optimizations tested.
    - → Need to choose a matrix size for APSELVI
  - Functional specifications also must be closed as soon as possible.
  - INMAPS → Design-kit exploration phase.
- Test beam
  - Updating Front End control firmware.
  - More flexible solution for different FE chips simultaneous acquisition.
  - TDAQ / SlimGUI re-organizatio about to start.

Conclusions

BACK-UP slides

PIXEL TEST CHIP SUBMISSIONS

- Architecture tailored on (code branch):
  - APSELVI 96x96
  - APSELVI 96x128
  - SuperPix1 32x128

Area **estimate** with ARM cell library for **TC submission**

Which one? →

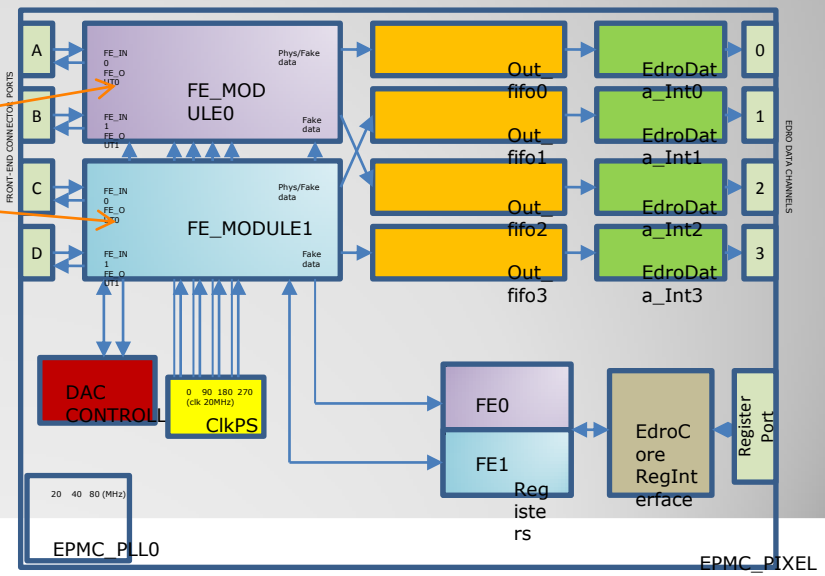
CHIP	N. Cells	Cells area (mm2)	RO area (mm2)
APSELVI96x96	78k	0.89	**8.71**
APSELVI96x128	102k	1.12	**11.31**
SuerPX1	68k	0.77	**7.57**

- NB: architecture functionality specifications still need to be closed!
- INMAPS submission: starting to evaluate the Design kit.

Summary 1

- Test beam 2011 DAQ update in progress
  - Different pixel FE chips have to be tested together. (control by the same Edro Programmable Mezzanine Card)
    - **APSEL4D / 4D_1**
    - **APSEL3D_TC**
    - **SuperPX0**
  - EPMC Firmware upgrade for the required flexibility 70% completed. (must be tested)
  - TDAQ and Configuration software must be updated as well. (process about to start).

EPMC new firmware
- 2 FE module slots
- Specific FE module plug-ins developed for each FE chip to be tested



Summary 2

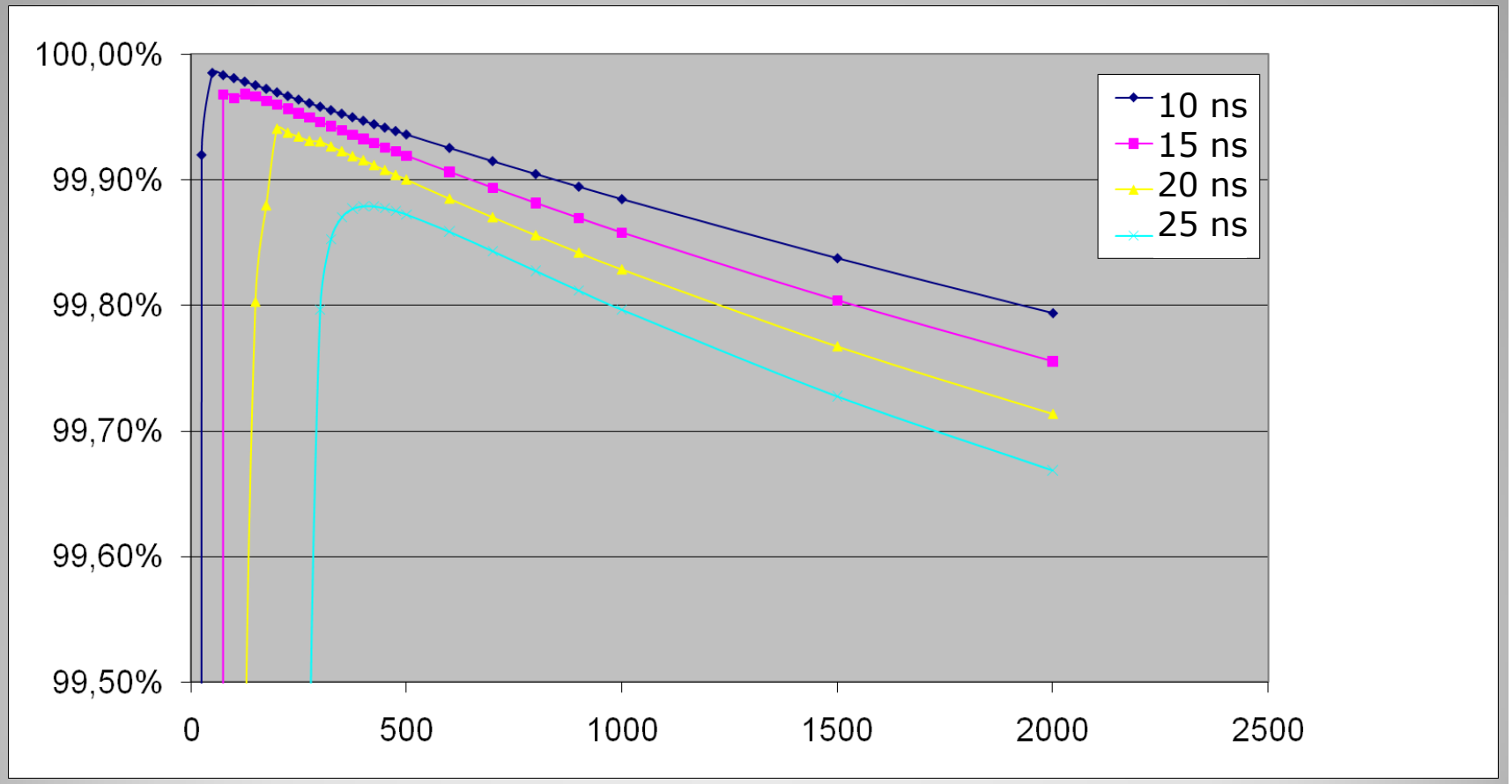
Bandwidth usage estimated by simulations

- ***Triggered mode***
  - **BC ~ 100 ns** (10 MHz)
  - Rate = **100 MHz/cm^2**
  - Trigger Rate = **150 KHz**

mean bandwidth usage of **40 Mbps**

Simulation results: BANDWIDTH

Expected efficiency combinatorial evaluations



NOT taken into account:

- sensor efficiency (assumed 100%)
- pixel reset dead time (assumed few ns)

Analitic expectation DATA PUSH

Data push Efficiency results:

SuperPX1 DATA PUSH arch.

RD (MHz) \ BC (ns)	200	250	300
%			
66.7	99.93	99.92	99.92
55.6	99.93	99.92	99.91
50	**99.92**	99.92	99.90

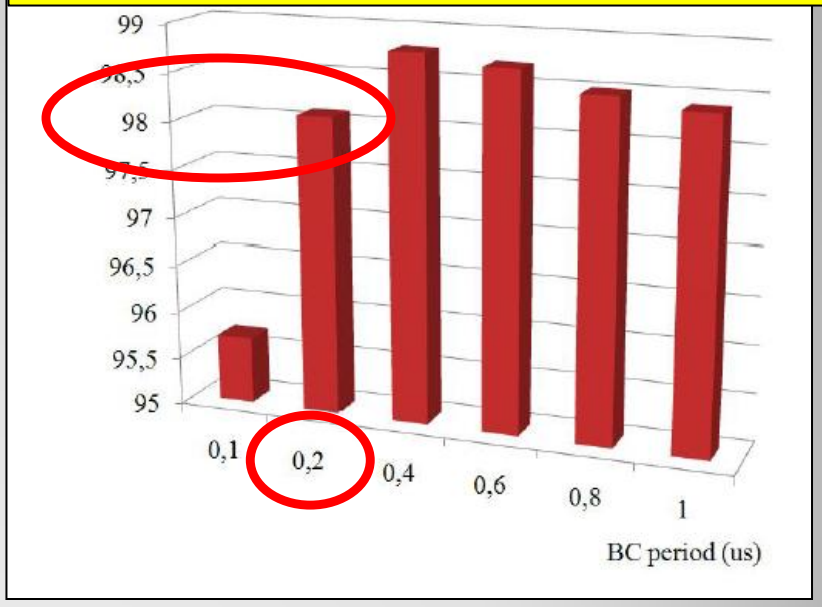
NOT taken into account:
- sensor efficiency (assumed 100%)
- pixel reset dead time (assumed few ns)

Readout de-queuing efficiency 100% (no barrel overflows)

- **Hit check** results: **100 % match**.
- Fast_clock **4 x** RDclk (output bus frequency)

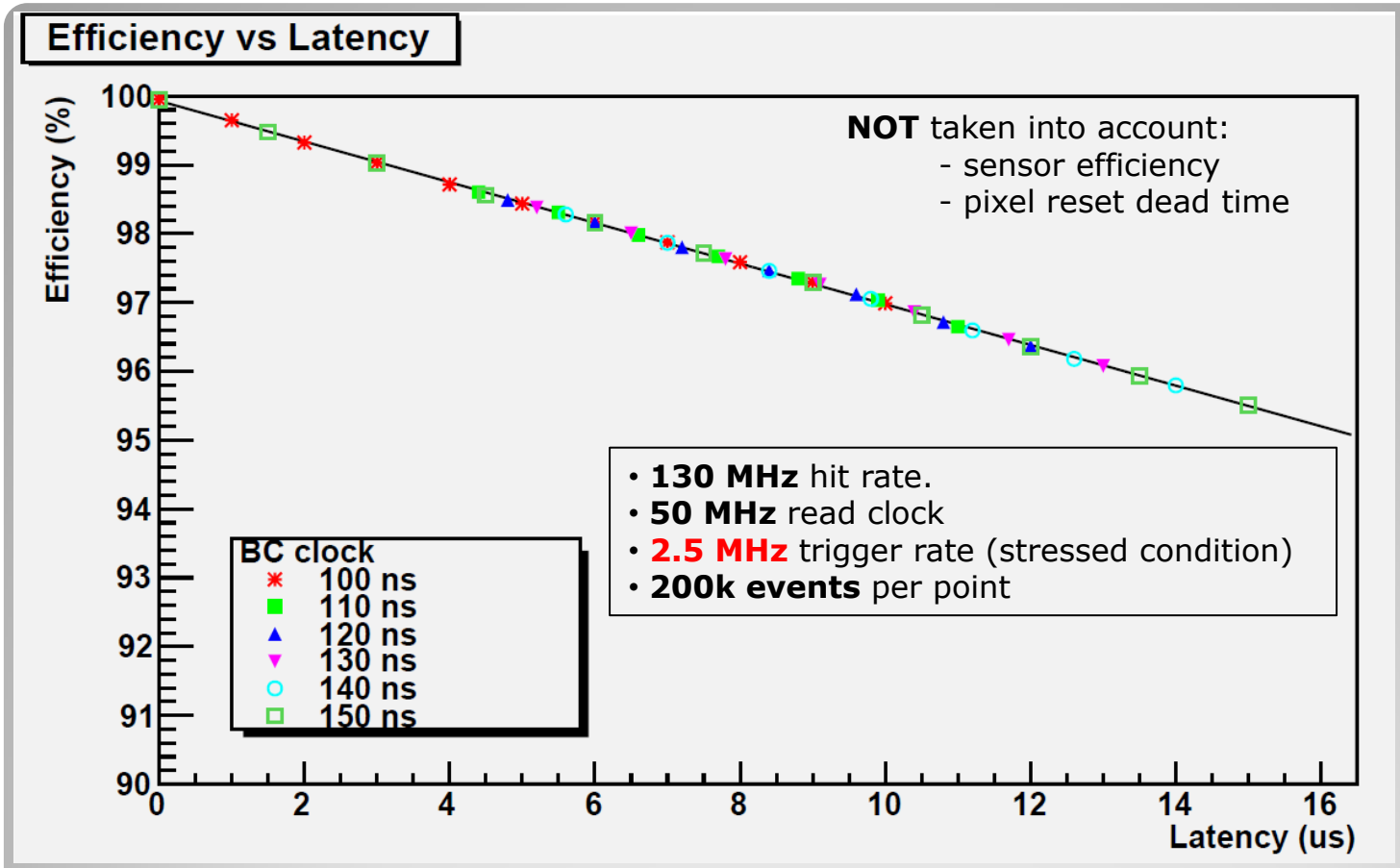
Compare with *SuperPX0* data push arch.

SUPERPX0 - RDclk **66.67 MHz** – Fast_clk **200 MHz (3x)**



efficiency results from similar simulations of *SuperPX0* readout

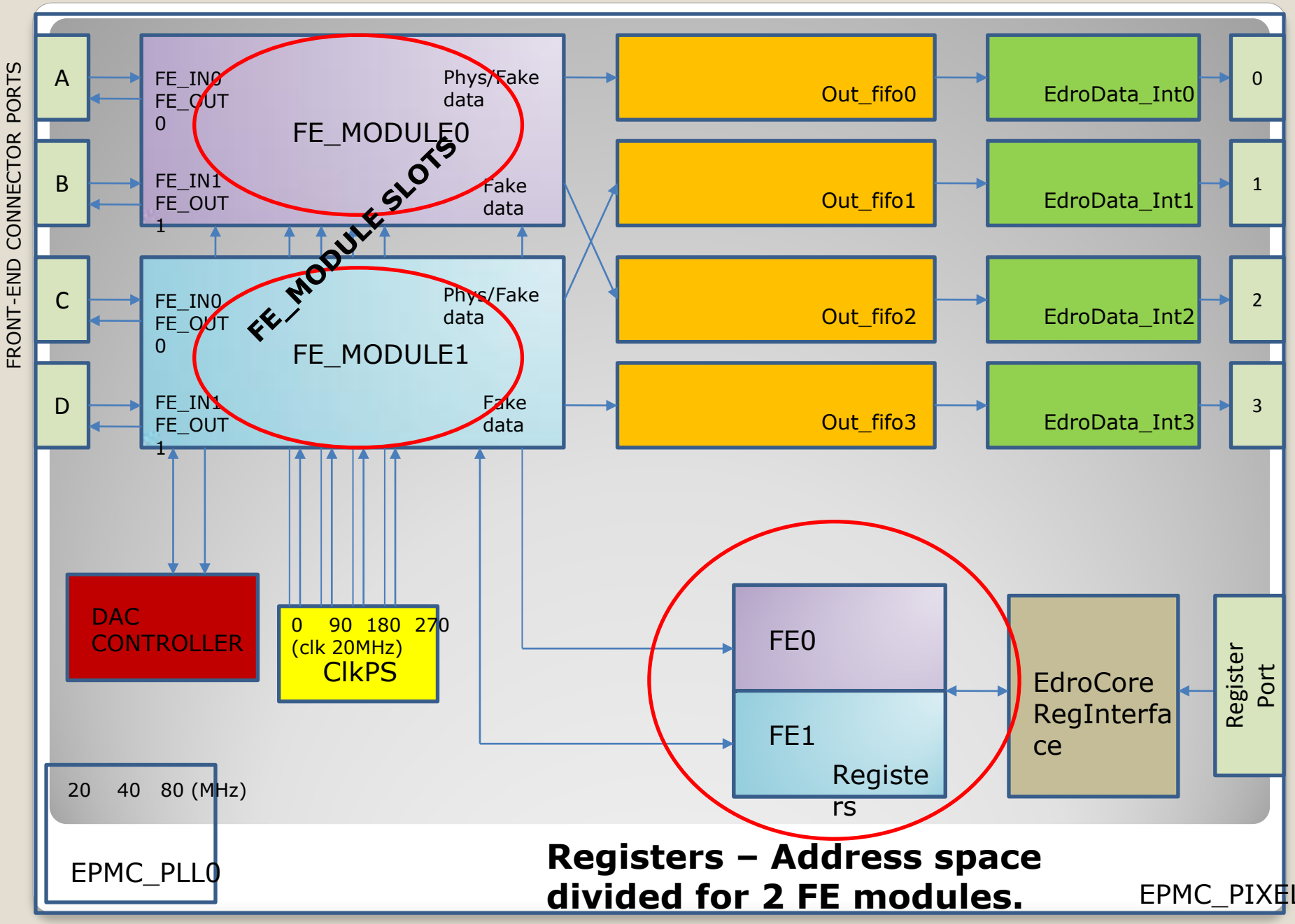
SuperPX0 comparison



- Smooth decrease of efficiency in function of trigger latency.
- Almost **no dependency** of efficiency **on BC period** (in this region)
- Linear fit slope: **-0.3 %/us**.

Simulation results, TRIGGERED

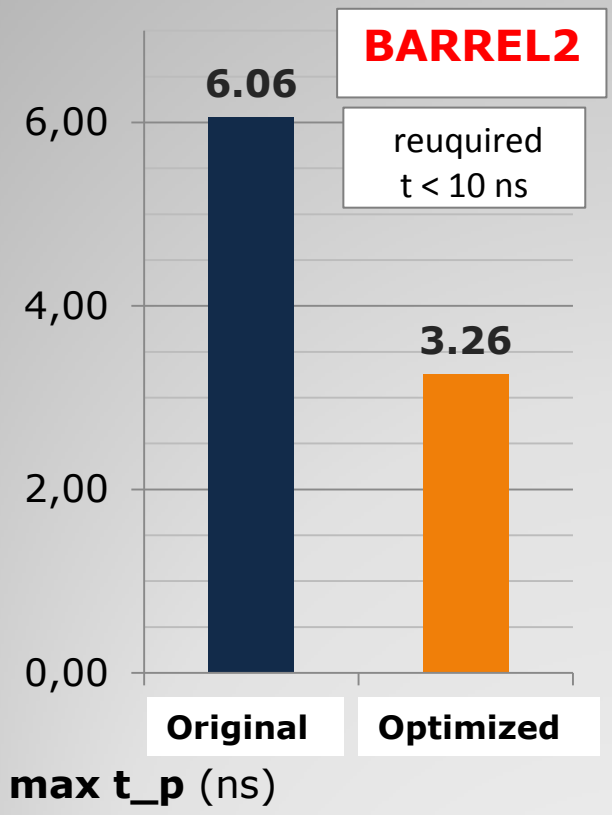
Front End Control Firmware Schematic

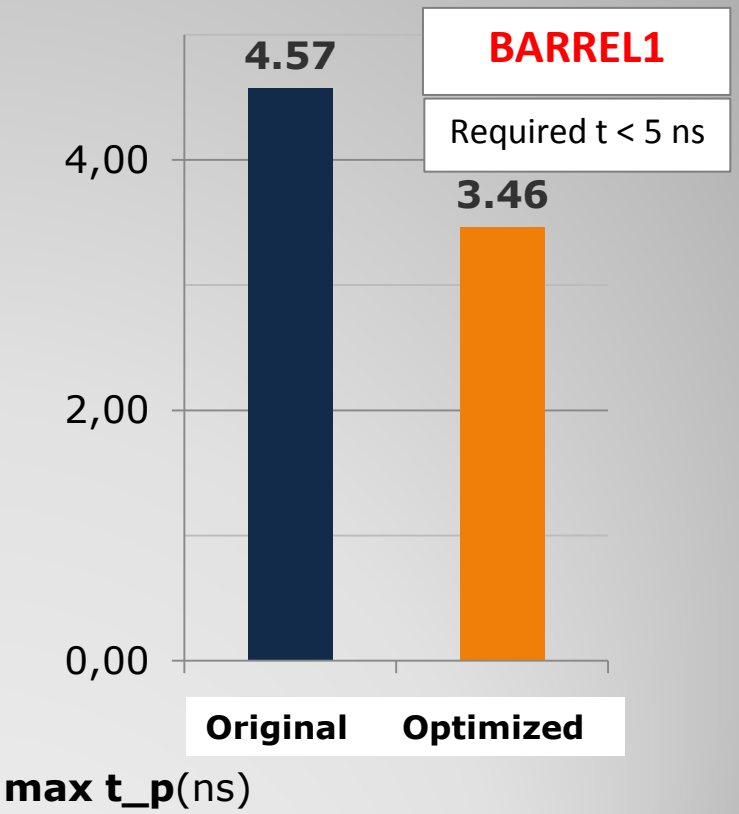


Registers – Address space divided for 2 FE modules.

Barrels speed optimization

Worse reg. to reg. signal propagation time



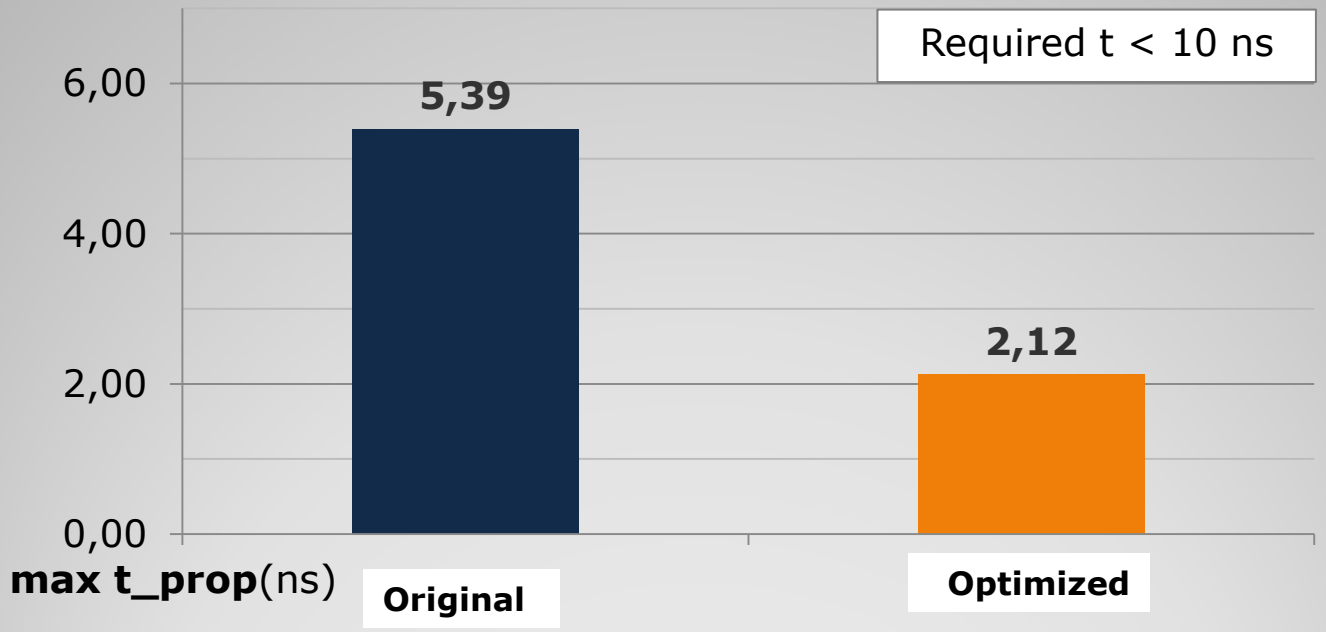


Optimizations

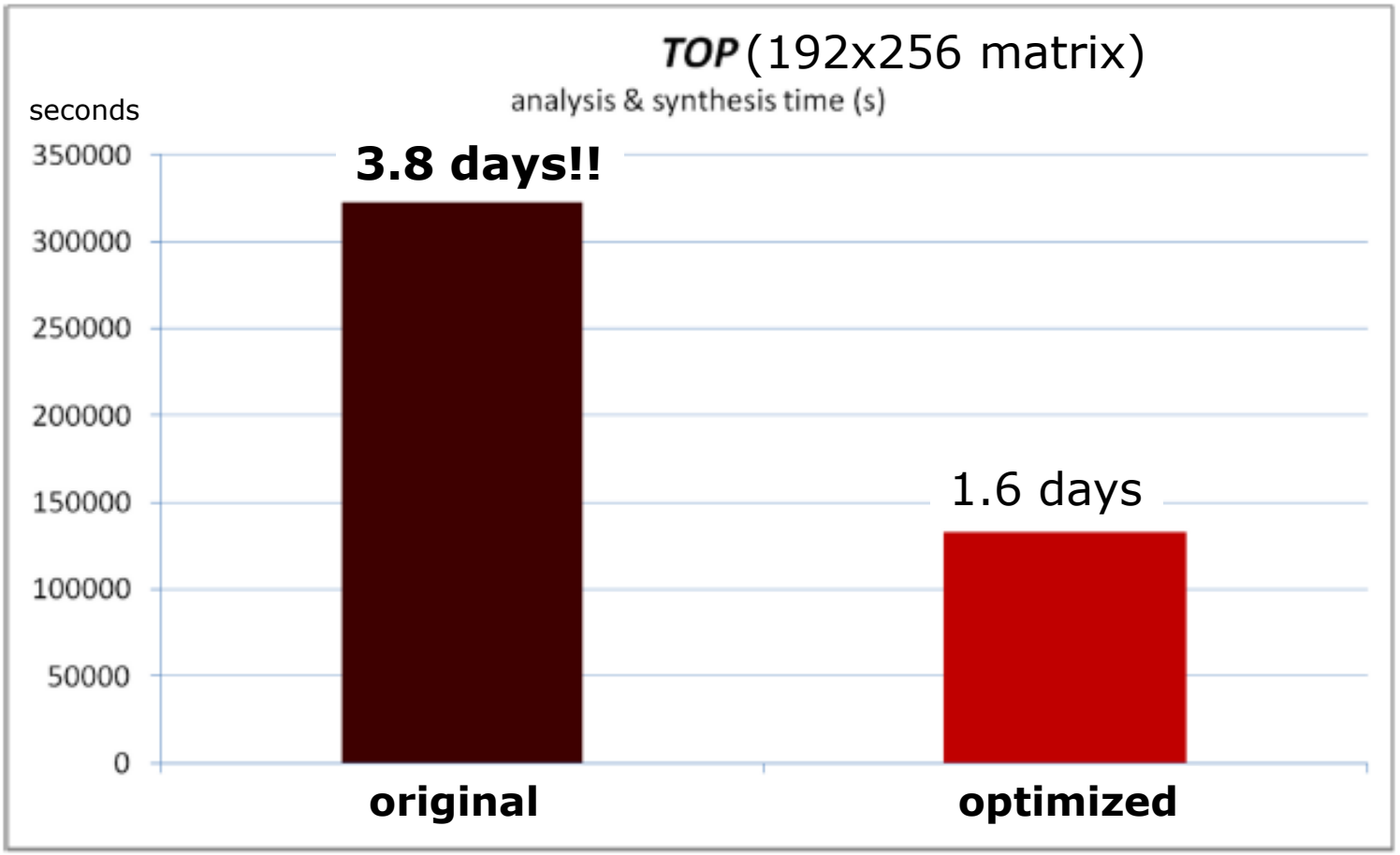
Optimizations

Sweeper speed optimization

Worse reg. to reg. signal propagation time

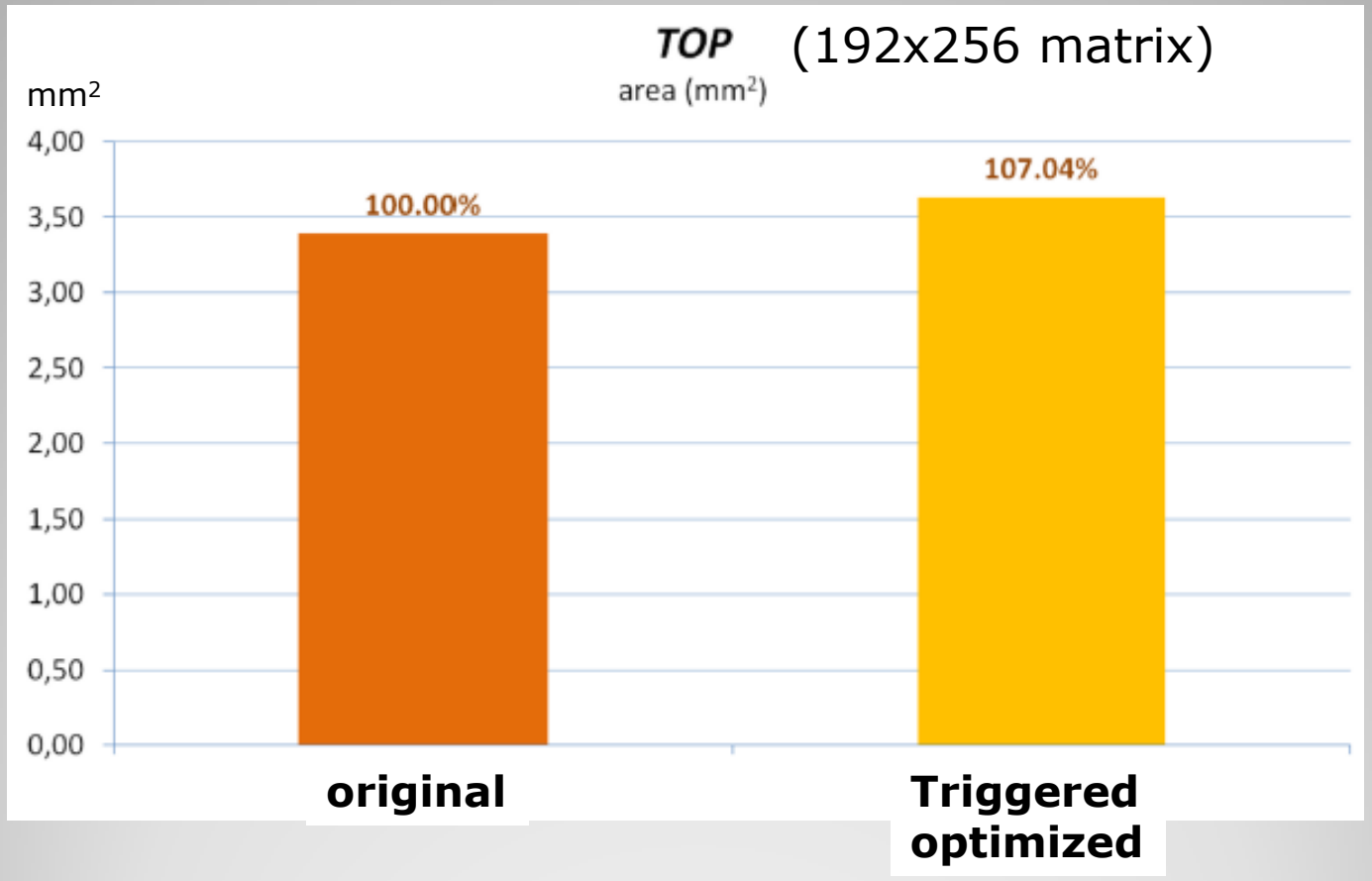


Full chip synthesis time optimization



Optimizations

Full chip cells area



Total cells area comparison

- **SuperPX1** hybrid 3D
  - Matrix 32x128
  - 2 sub-matrices 16x128
  - 4 sparsifiers
  - 8 zones for each sparsifier
  - zone width: 4 pixels

- **APSEL-VI** MAPS 3D
  - Matrix 96x128 (96x96)
  - 2 sub-matrices 48x128 (48x96)
  - 4 (3) sparsifiers
  - 8 zones for each sparsifier
  - zone width: 4 pixels

Submissions 2011

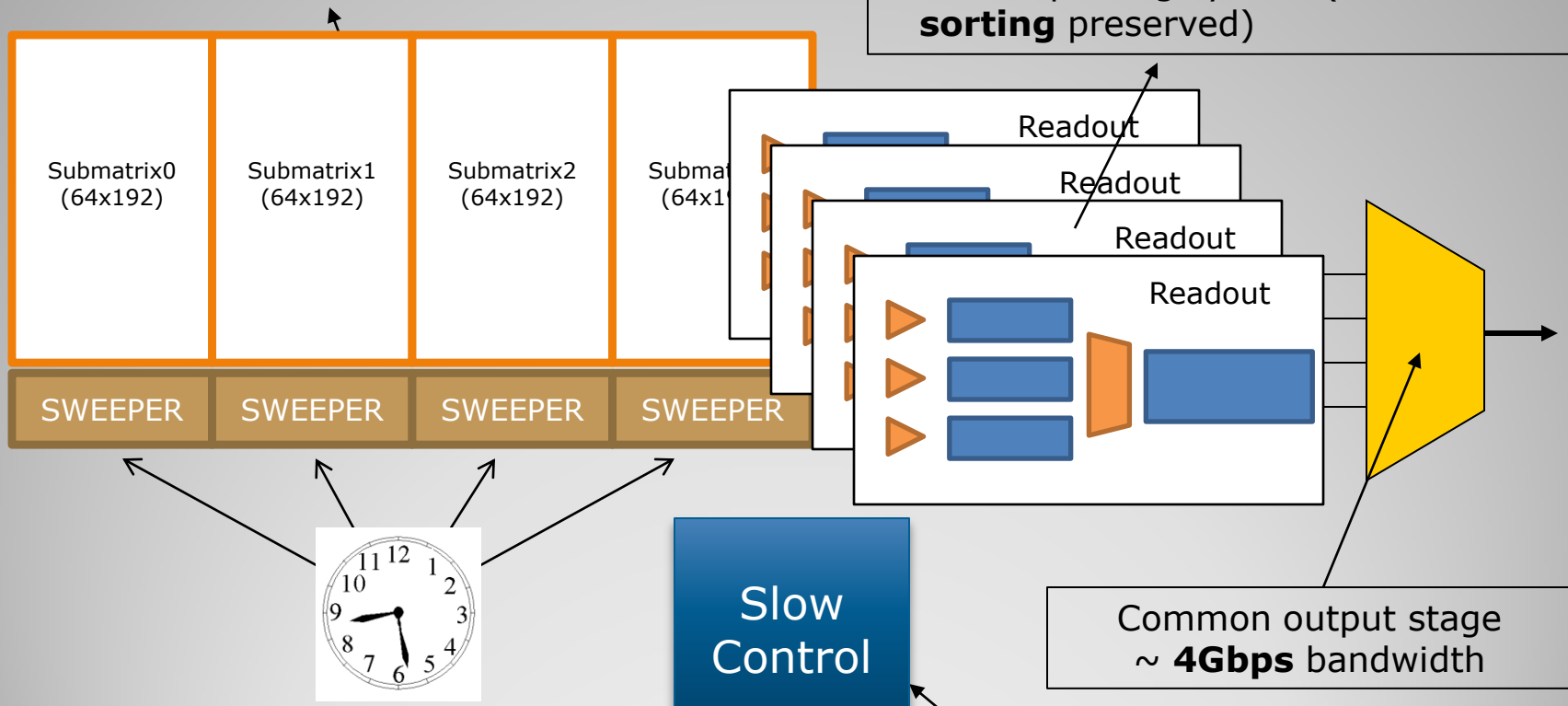
Readout Scheme

- Pixel organized into **4 sub-matrices**
- **Each** sub-matrix has an **independent** scan logic

→Increase horizontal parallelization

→The shorter the scans the greater the effi.

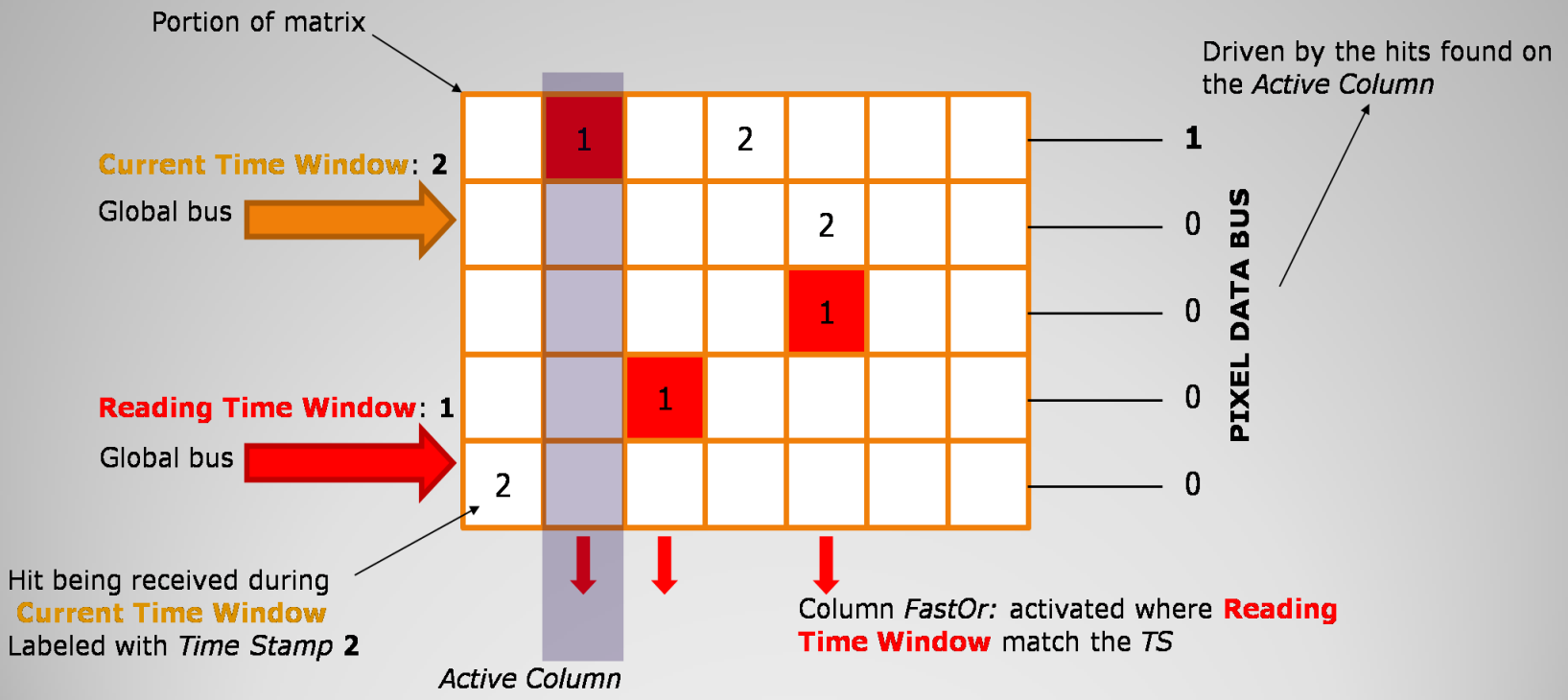
- One readout for **each** sub-matrix
- Vertical parallel sparsification (**one entire column** per clock cycle)
- Hit encoding
- Hit de-queuing system (**time sorting** preserved)



EXAMPLE

During **Time Window 2** :

- Some pixels getting fired and labeled with *Time Stamp (TS)* **=2**
- The readout queries the columns containing hits labeled with *TS*=1 (**Reading Time Window** → *FastOr* activation)
- The readout moves the *Active Column* over the columns with an active *FastOr*.



Matrix scan Logic example