Integrated front-end for drift chambers

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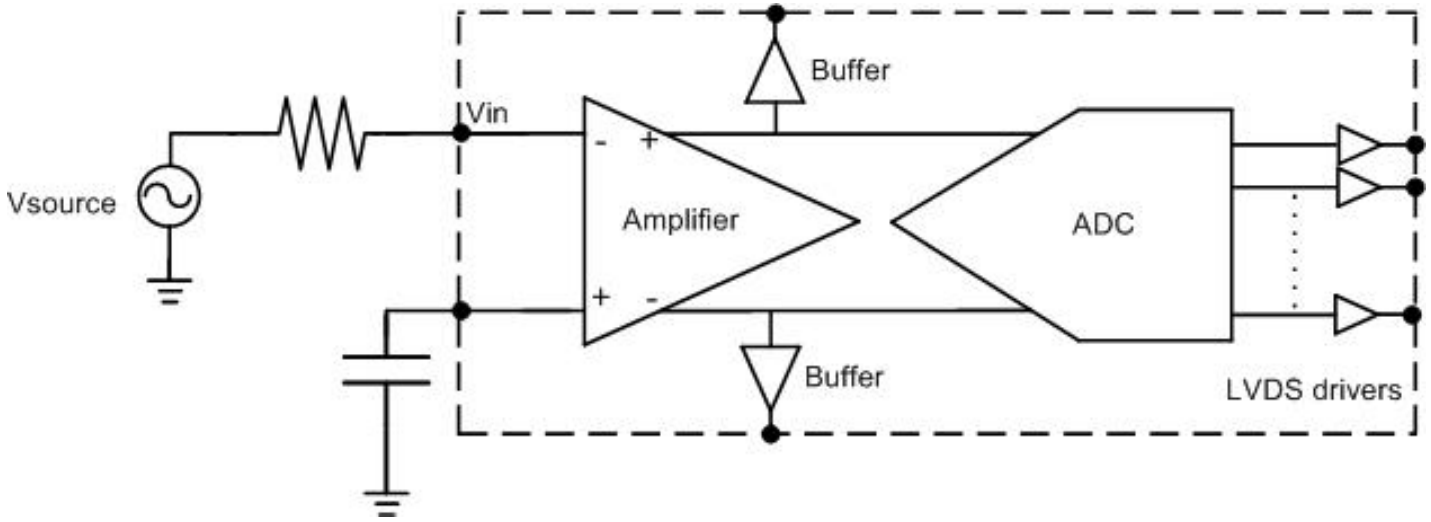
Overview

- Integrated front-end architecture
- I complete version of the front-end:
  - Circuits description
  - Measurements&performance
- II complete version of the front-end:
  - Circuits description
  - Preliminary Measurements
- Conclusions

Front-end architecture



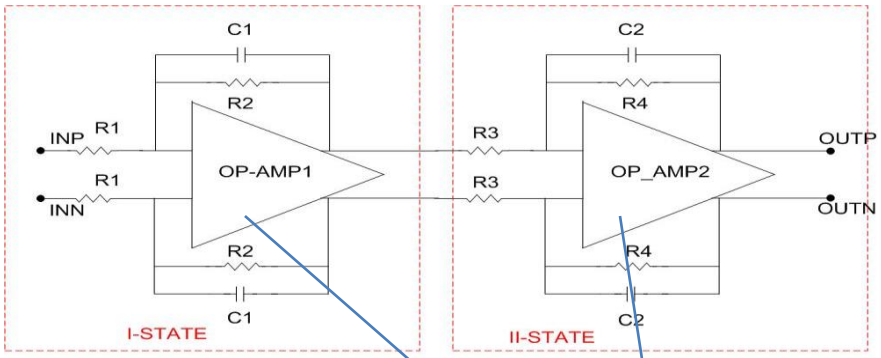
-Amplifier (single ended to differential conversion, 26dB gain)

-ADC(6 bits resolution, 1Gs/s)

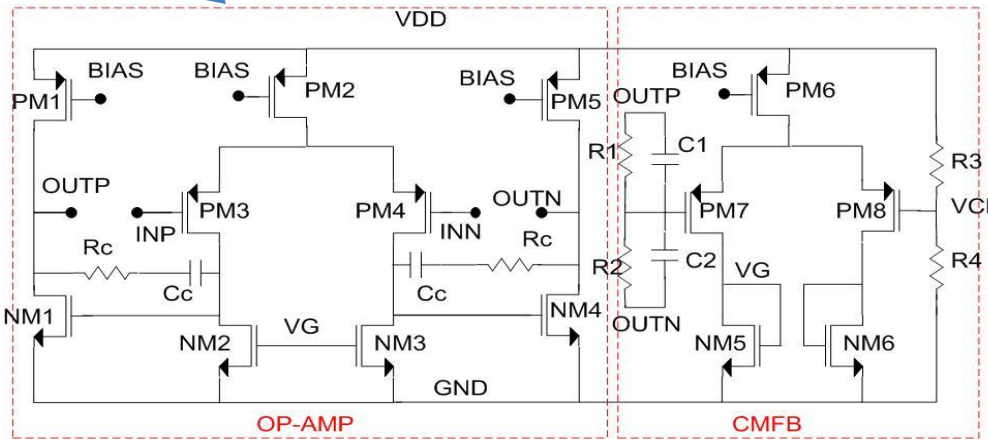
-LVDS drivers

-buffers

I complete version: the amplifier



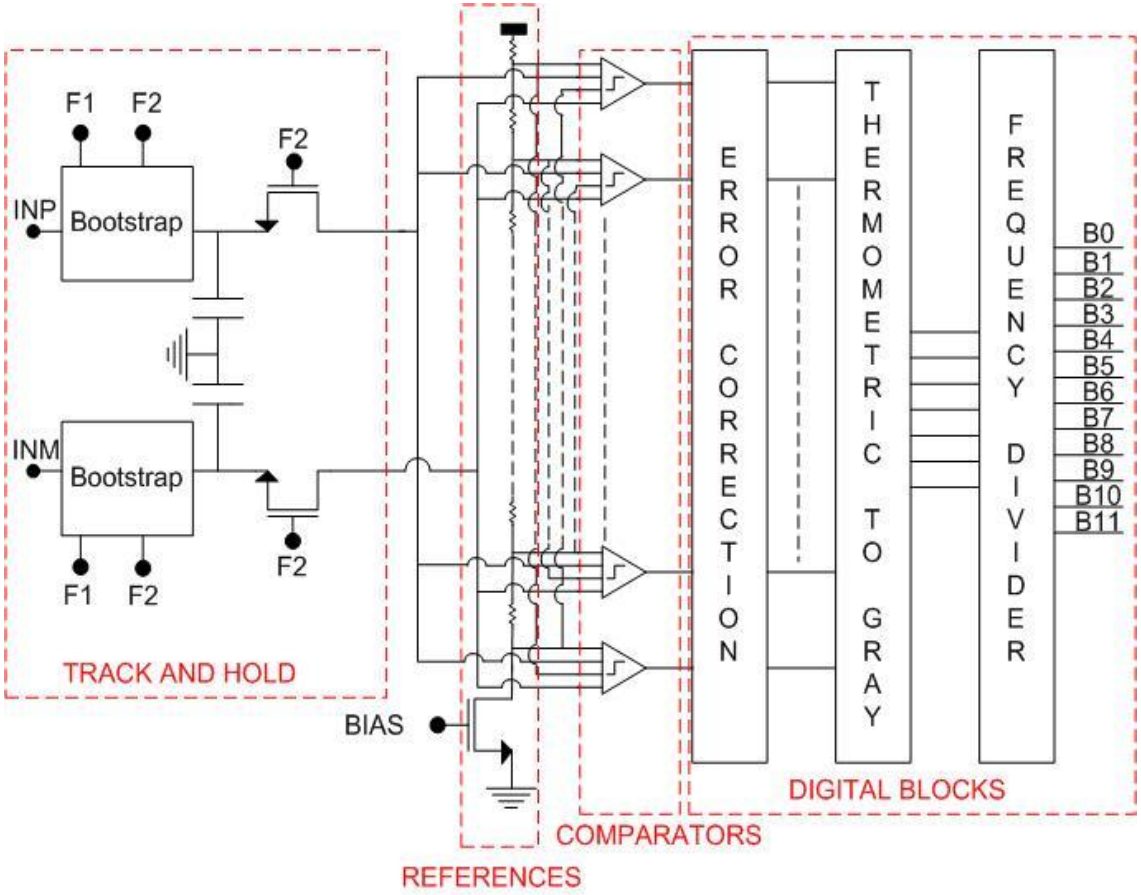
Parameter	Value
Input impedance	50 Ω
No. of stages	2
1rst stage gain	16 dB
2nd stage gain	10 dB



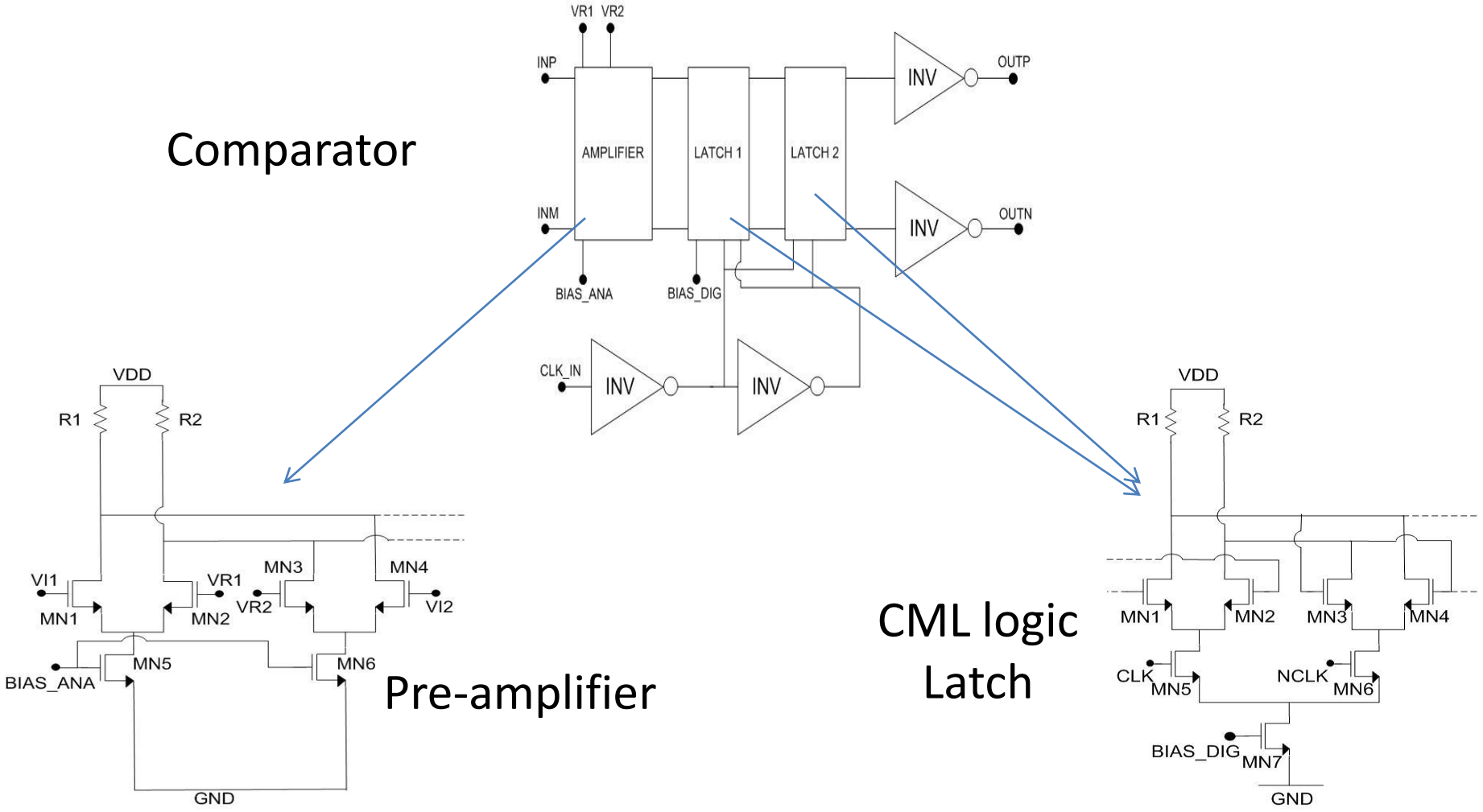
Miller opamp

I complete version: the ADC

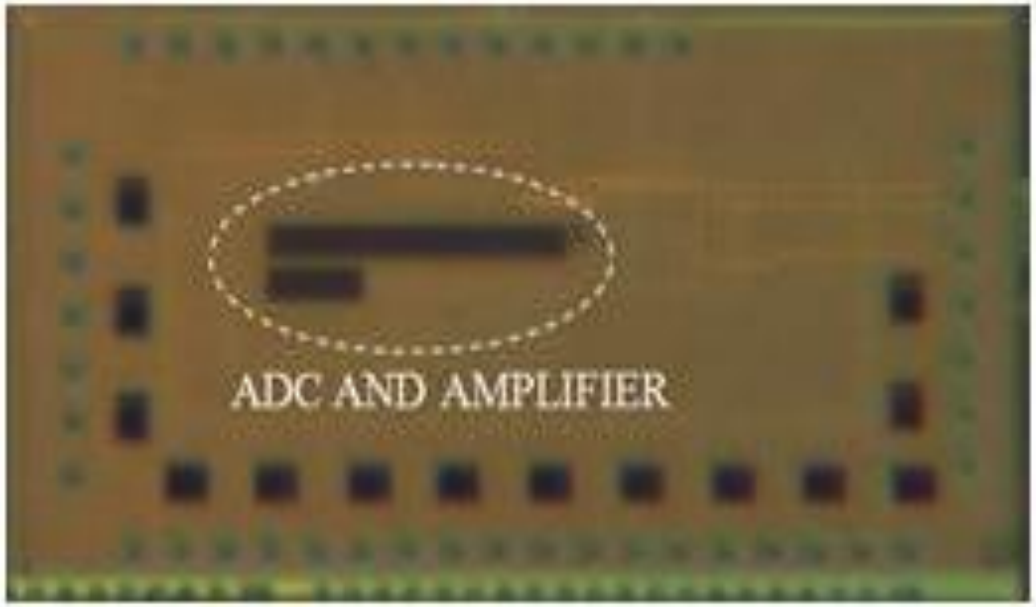
Full flash architecture



I complete version: details of the ADC



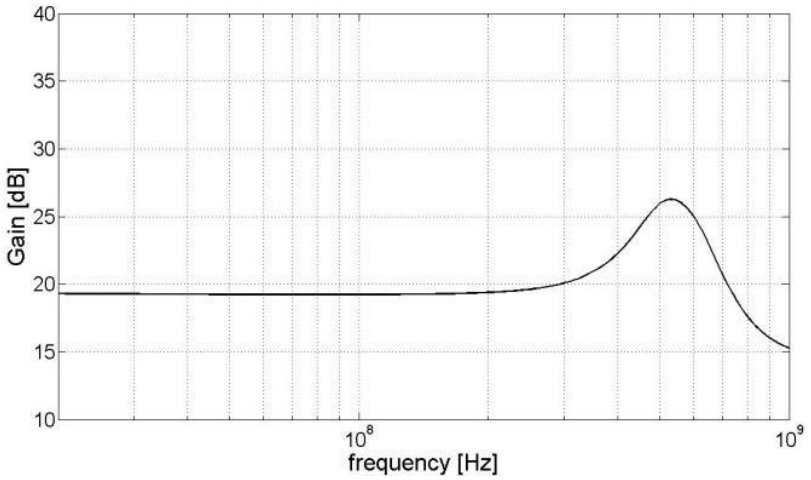
I complete version: Chip Microphotograph

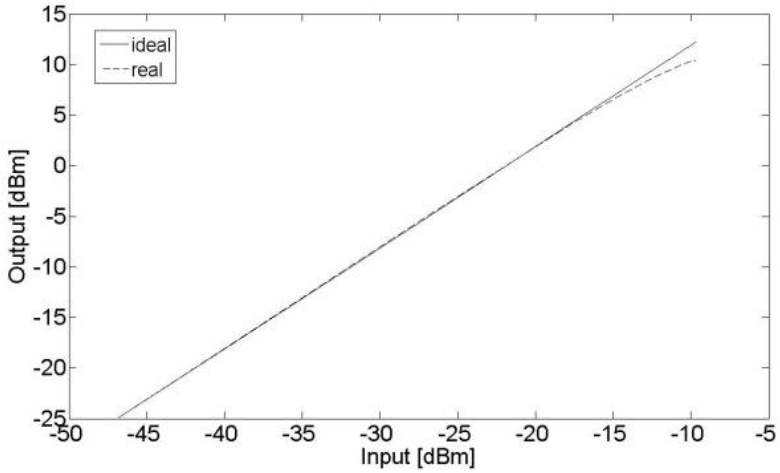


Technology: CMOS 0.13um
Chip size: 3mmX1.5mm

I complete version: experimental results

Measurements on the amplifier





Amplifier transfer function

DC – gain:20 dB (gain loss due to the internal resistance of the signal source)

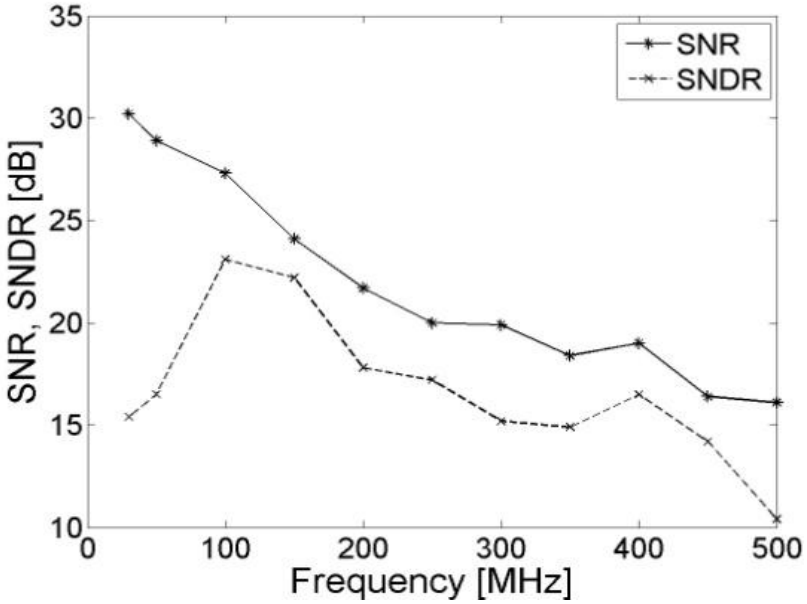
BW_{-3dB}: 870 MHz

1 dB compression point:

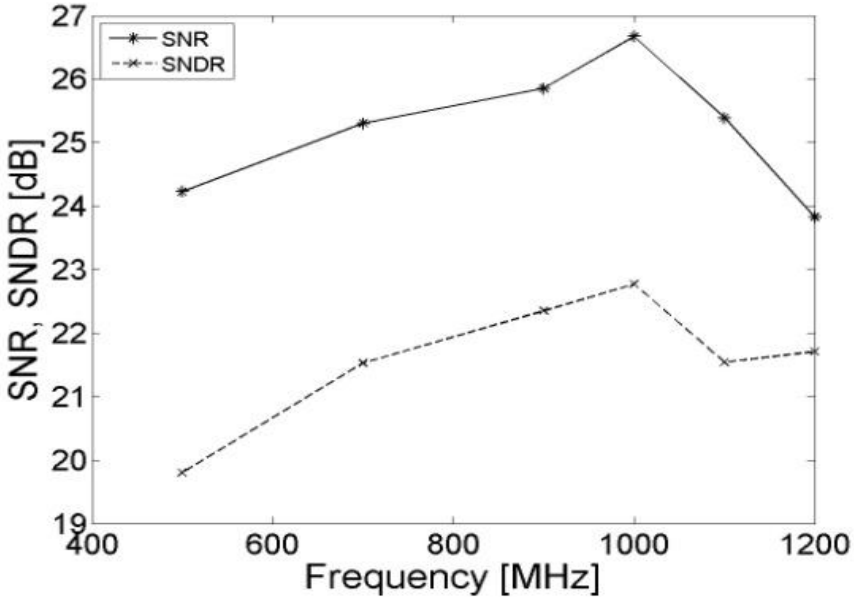
-11.8 dBm of input signal level

I complete version: experimental results

Measurements on the amplifier



SNR, SNDR vs input frequency

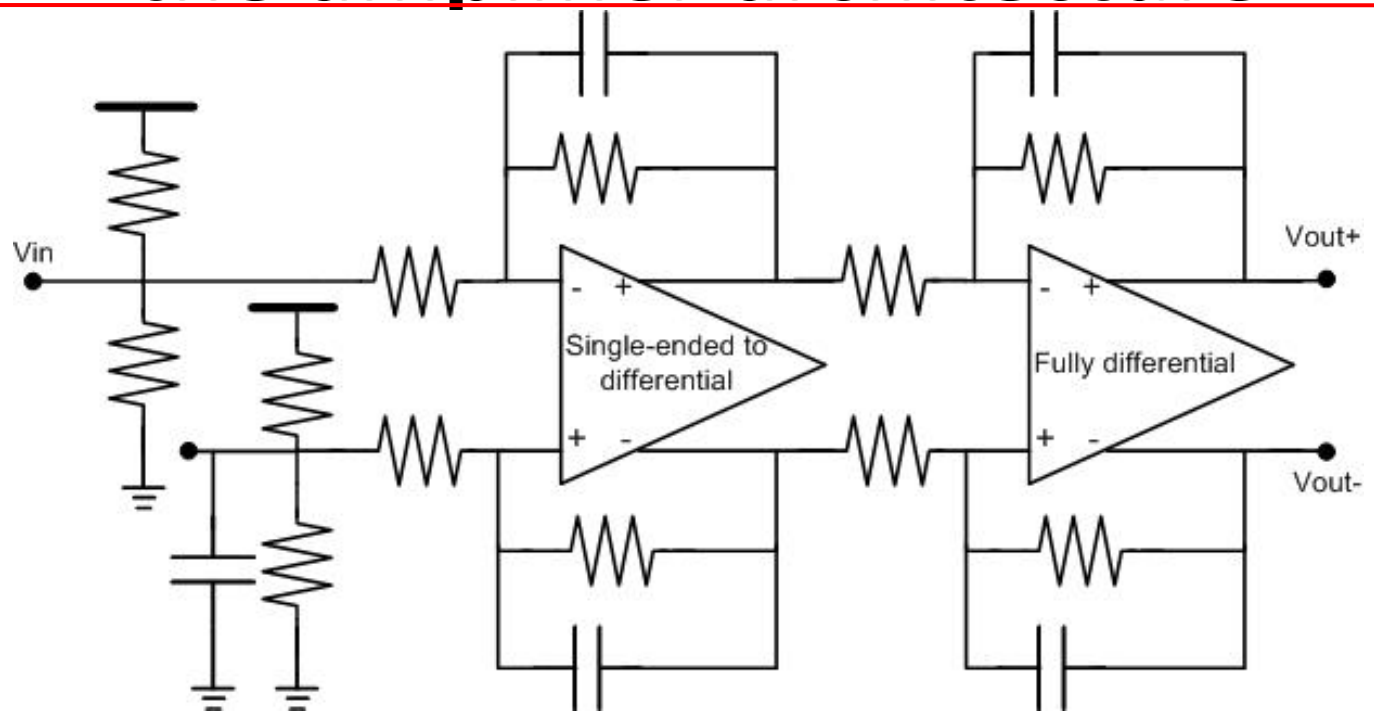


SNR, SNDR vs samply frequency
with input frequency of 100MHz

I complete version: experimental results

	Parameter	Value
	Technology	CMOS 0.13um
	Supply voltage	1.2V
	Chip area	3050x1525um^2
Amplifier	DC-gain	20 dB
Amplifier	BW_{-3dB}	870 MHz
Amplifier	1 dB compression point	-11.8 dBm
Amplifier	Amplifier current consumption	25mA
ADC	SNDR@100MHz	23dB
ADC	SNR@100MHz	27 dB
ADC	ADC current consumption	79mA

II complete version: the amplifier architecture



1th stage

-Single ended to fully differential conversion

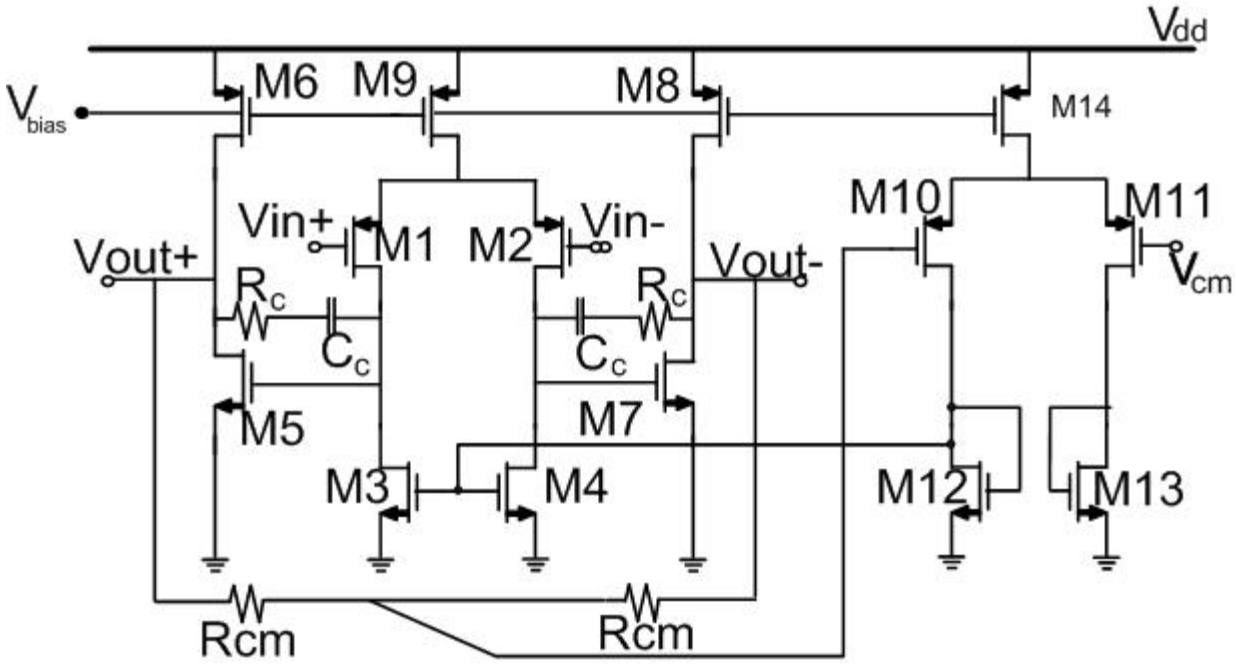
-Gain=16dB

2nd stage

-Fully differential stage

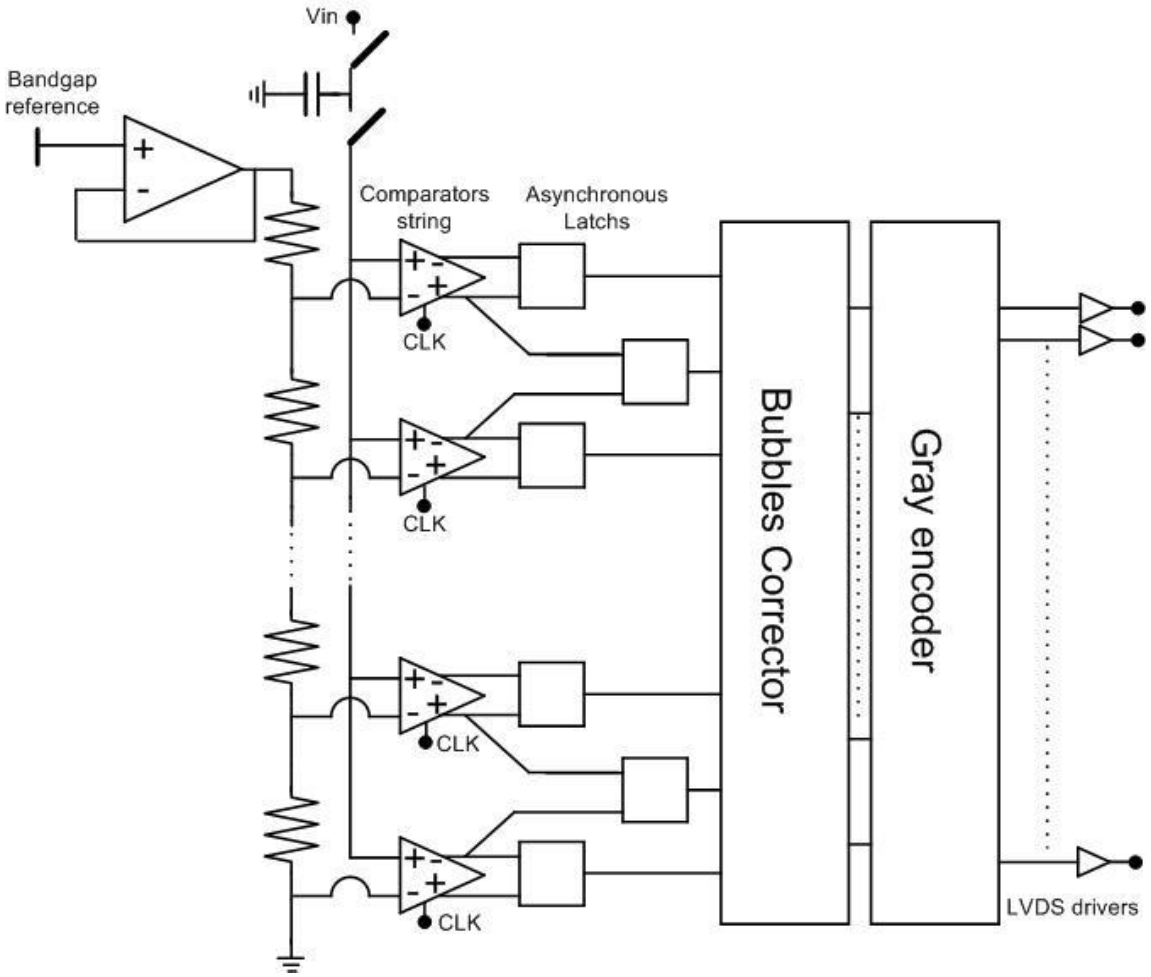
-Gain=10dB

II complete version: opamp schematic



Two stages Miller opamp

II complete version: ADC architecture

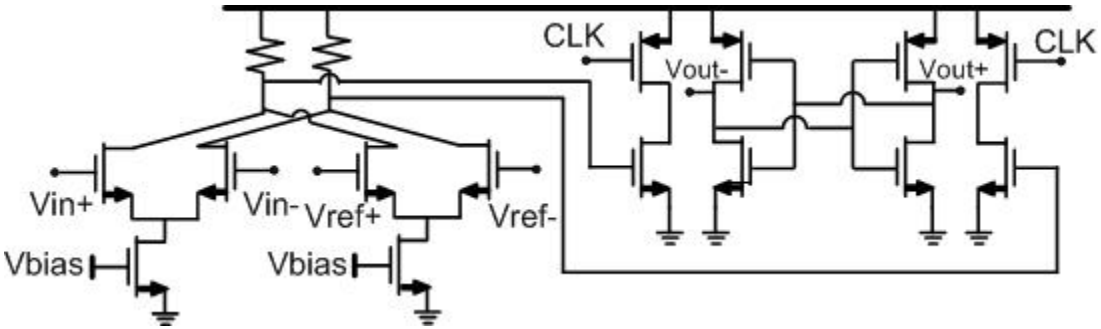


Flash interpolated architecture
- Reduction power consumption
- Reduction kickback noise

References generated by a bandgap circuit

II complete version: ADC details

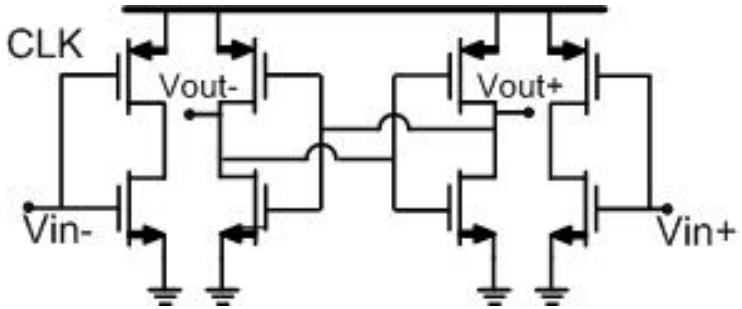
Two stages comparators



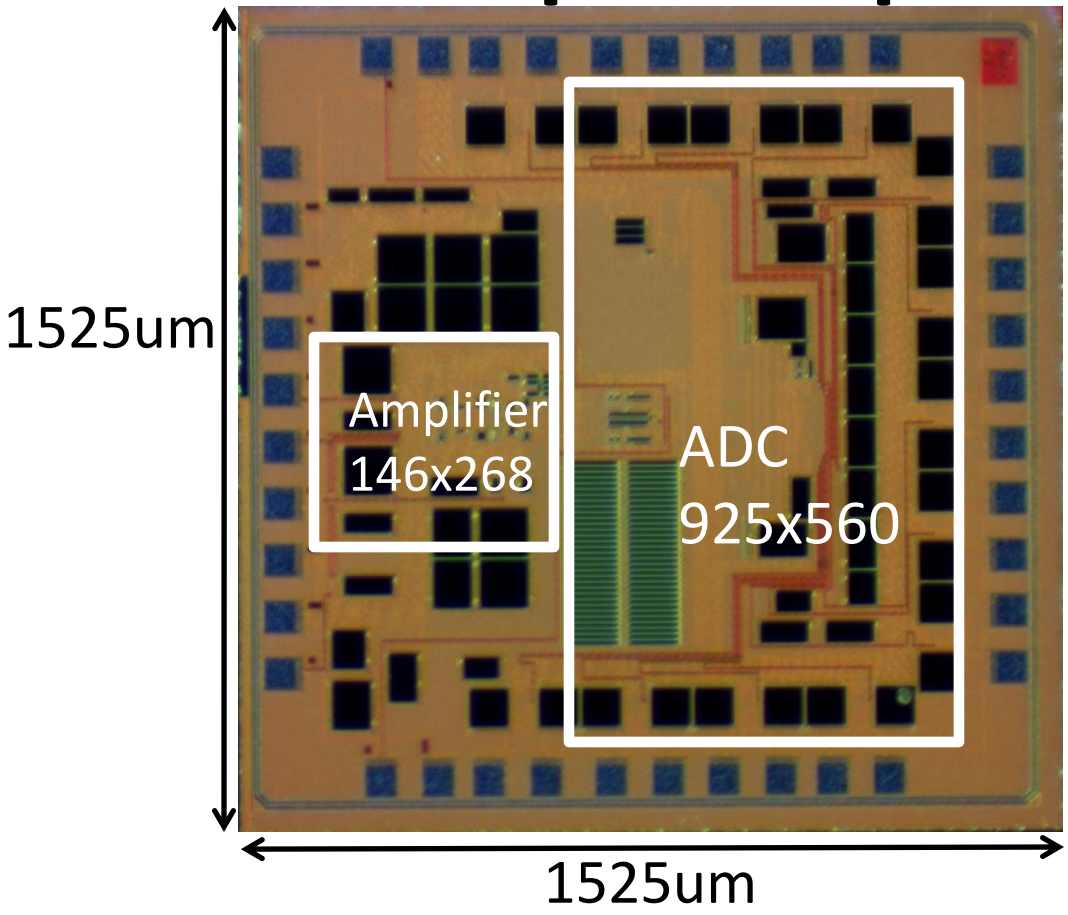
Preamplifier

Clocked latch

Asynchronous latch



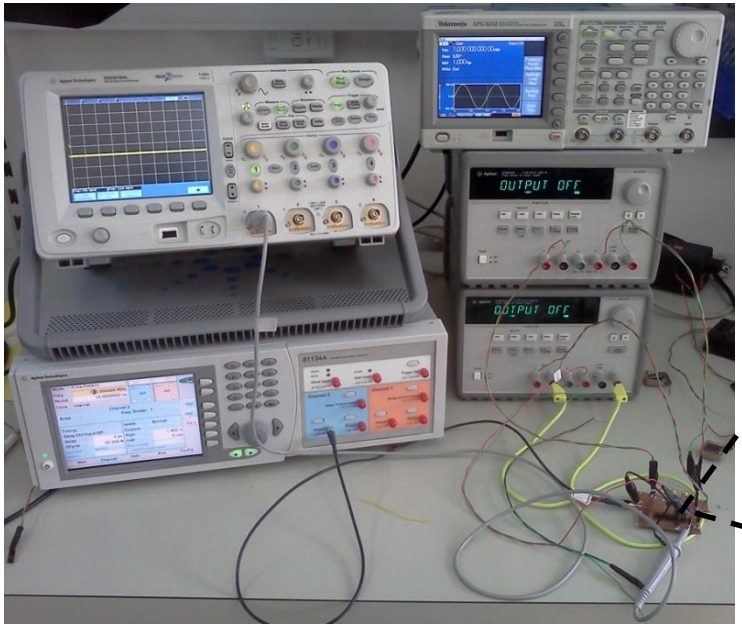
II complete version: Chip microphotograph

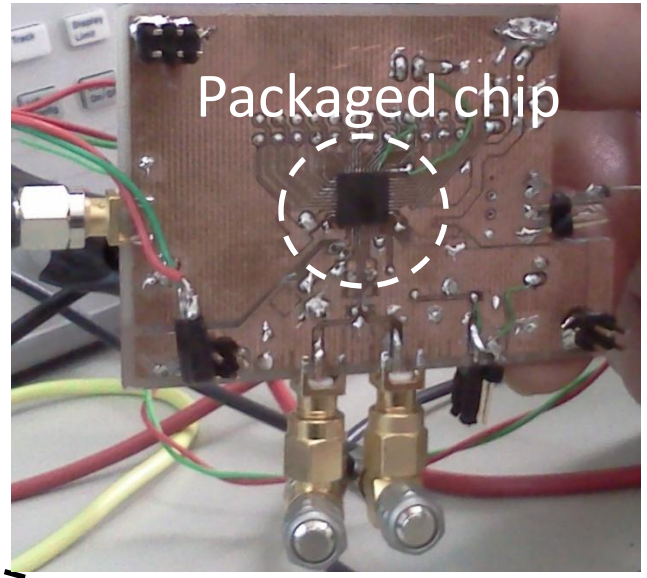


Technology: CMOS 0.13um

Chip size:1525umx1525um

II complete version: Measurements setup





II complete version: Preliminary results

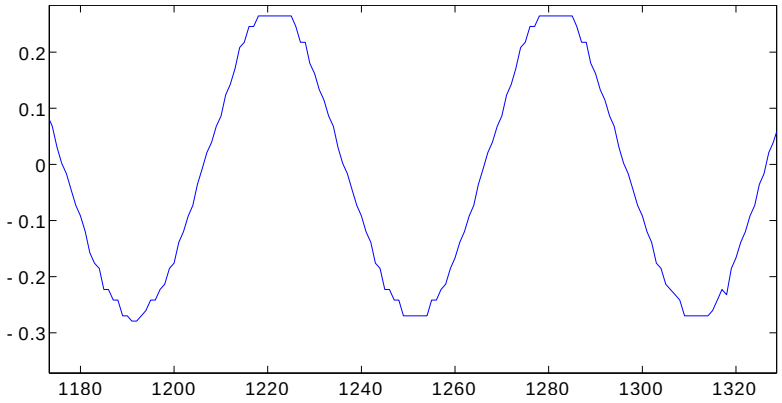
Power consumption

Section	**Consumption (mA)**
Analog (ADC+amplifier)	50
Digital	8
Bandgap	0,125
LVDS deivers	30

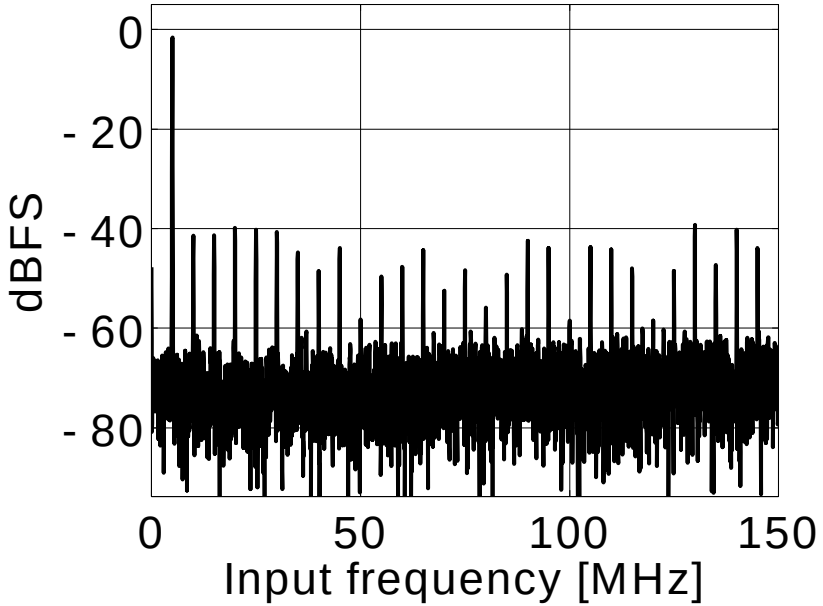
II complete version: Preliminary results

Single tone test

Output waveform



FFT



SNDR=30dB

Digital development platform

Xilinx Virtex VI platform was selected as general platform for cluster counting algorithms development and demonstration. Virtex VI devices combine programmable logic and a PowerPC into a single platform.

VIRTEX VI

Digital bus

IC Front-End

Conclusions and future prospectives

Two versions of the integrated analog front have been proposed

Measurements on the first version have been presented

A second version has been imlemented to get the following goals:

-amplifier bandwidth at 500MHz

-less power consumption

-improoved ADC linearity

-reduced chip area

Measurements on the II version of the chip must be completed

Measurements by the FPGA has to be set-up