CLUster TIMing Electronics Part II

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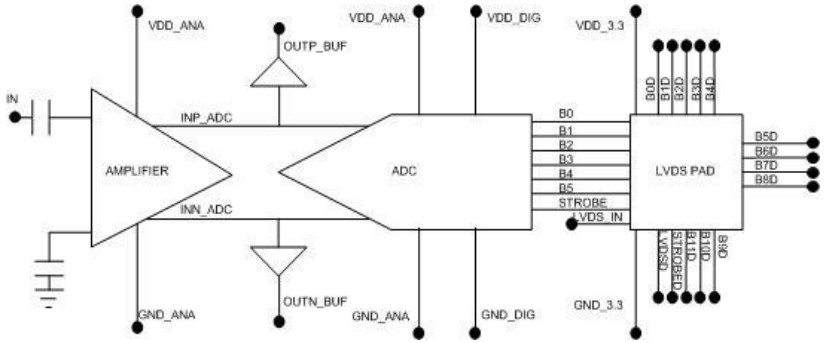
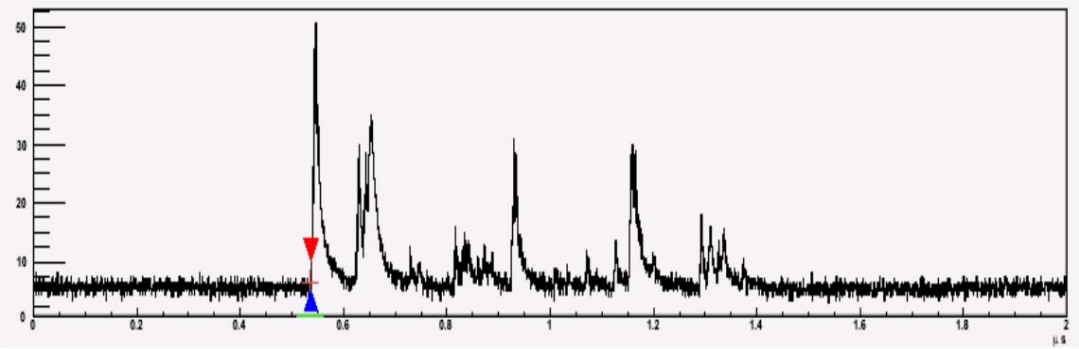
on behalf of CLUTIM group

Outline

- ADC output signal
- CLUTIM aims
- Device Selection (Virtex 5 vs 6)
- Virtex 6 Layout
- ISE Development Enviroment
- VHDL Algorithm
- FFT Test
- Future Planning

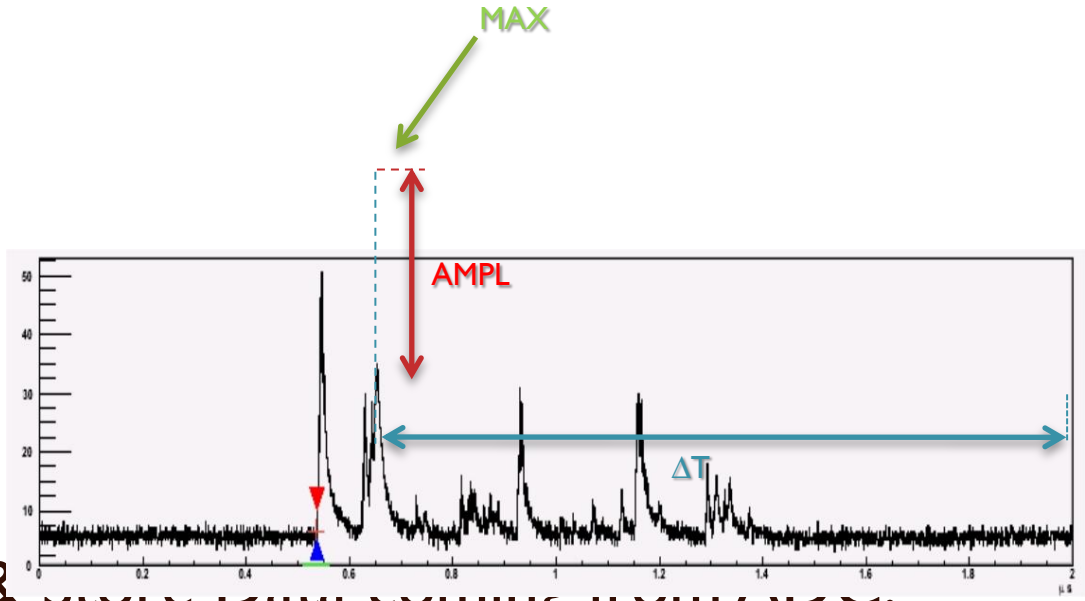
ADC output signal





- 12 bit (6+6) discretized signal
- 500 MHz frequency
- LVDS bus

CLUsterTIMing aims



- Read & store Data coming from ADC.
- Peak Detection
- Amplitude and Timing Peak Information Storage

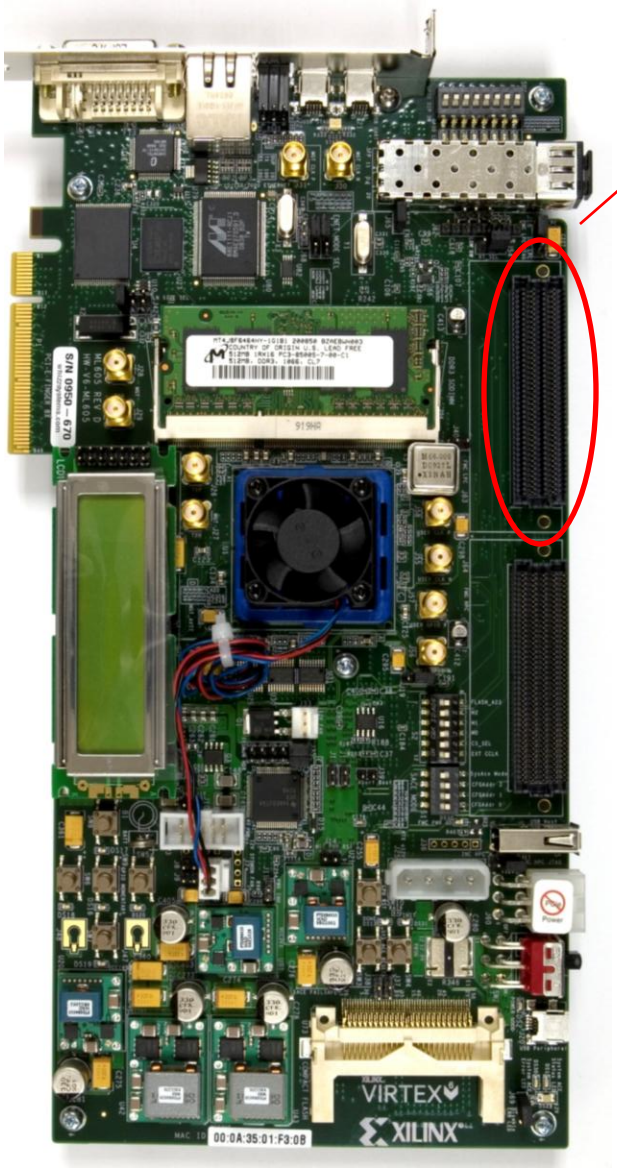
Device Selection

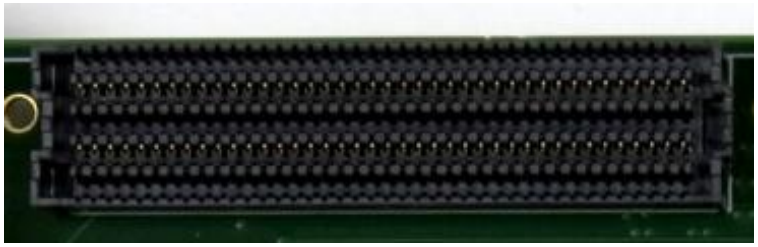
- Virtex 6
- ML605 Evaluation Kit
- FMC Connector

Table 60: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BIOCKO_O}	Clock to out delay from I to O	0.14	0.16	0.18	0.21	ns
Maximum Frequency						
F_{MAX}	I/O clock tree (BUFIO)	800	800	710	710	MHz

ML605 Evaluation Kit





- VITA 57.1 FMC LPC Connector
- Up to 700 MHz
- No coupling problems

VITA 57.1 FMC LPC Connector

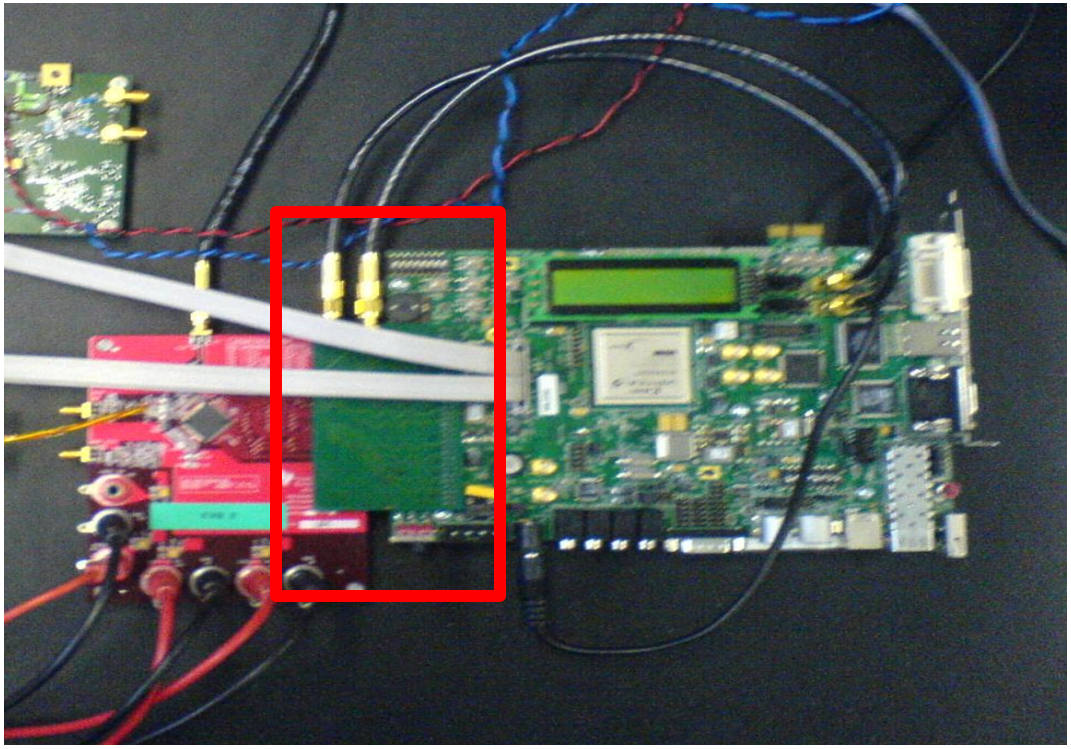
	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC

Figure B-1: **FMC LPC Connector Pinout**

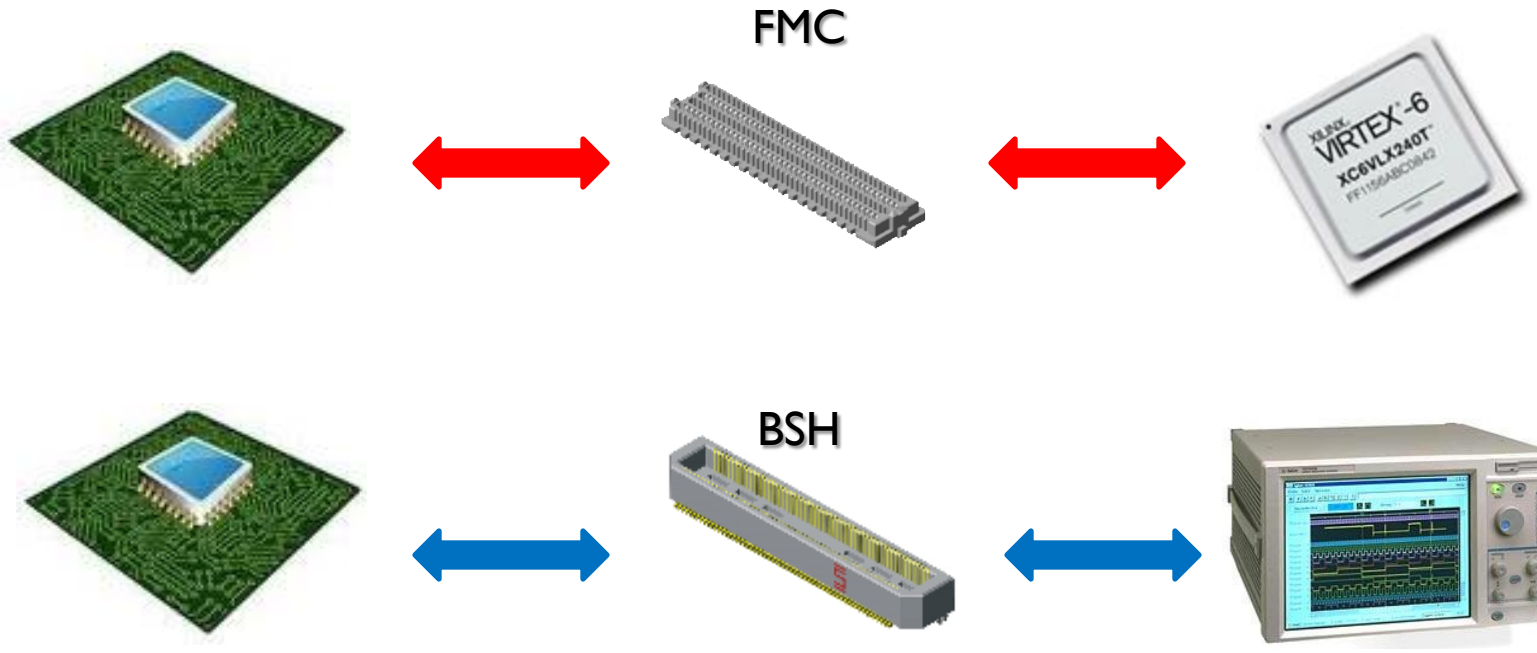
- 12 differential inputs
- 1 differential clock input

Possible Setup

- Possible direct coupling
- Using a daughter board
- Gandalf Experiment

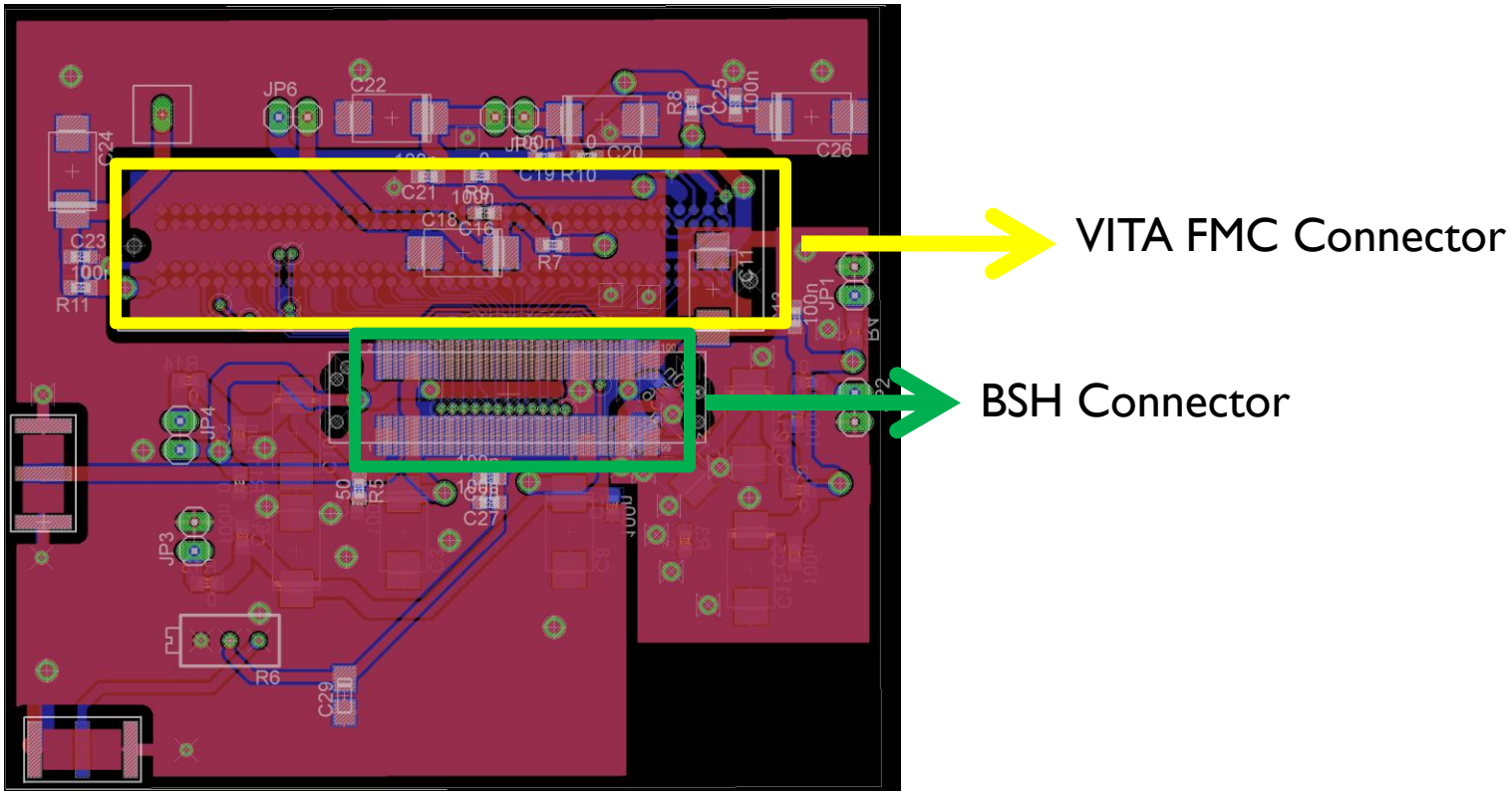


Developing Setup



- Use of a daughter board to connect ADC to Virtex 6
- Use of another daughter board to connect ADC to Logical Analyzer

Possible Setup – Daughter Board

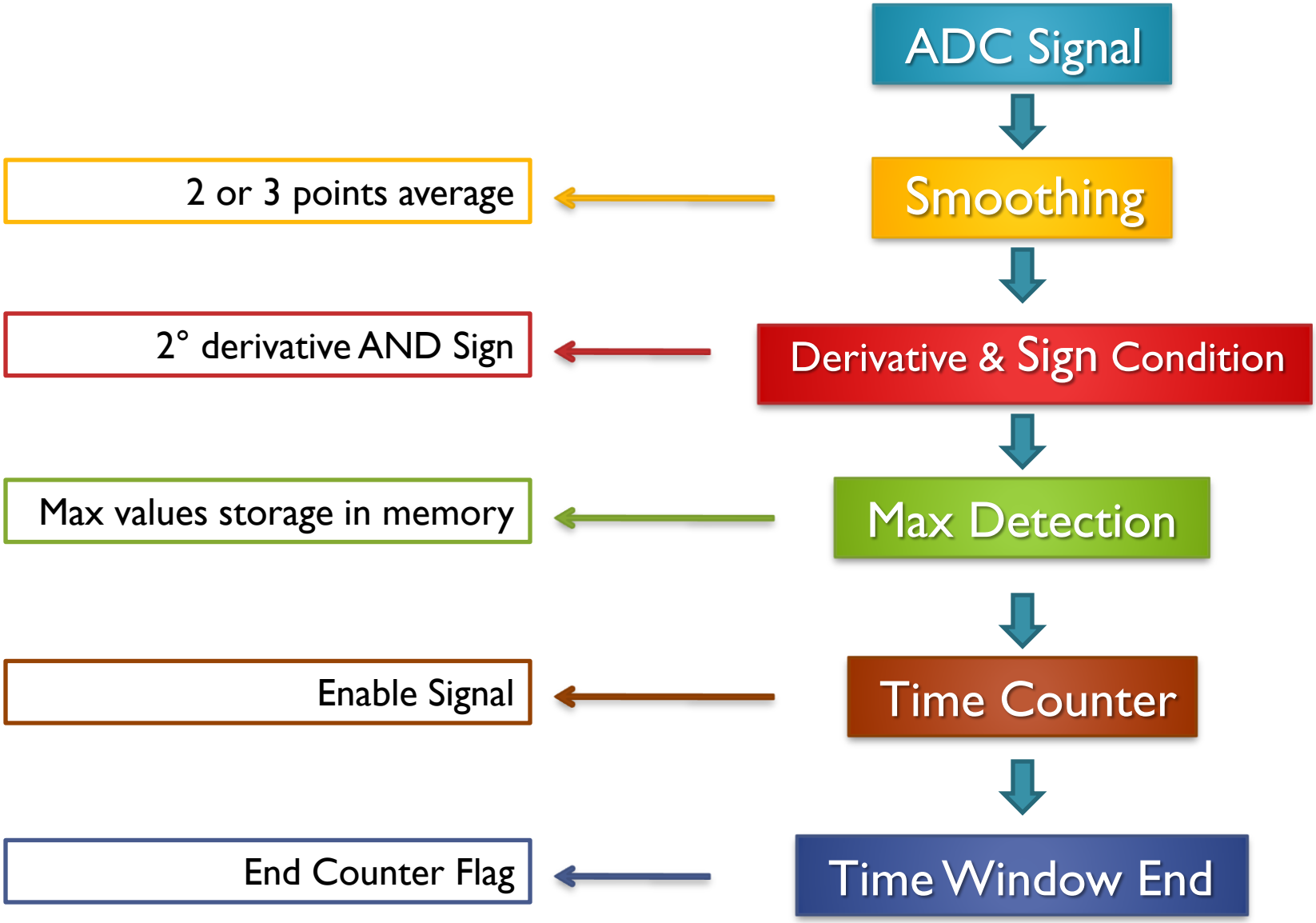


- Use of a daughter board to connect ADC to Virtex 6
- Impedance Matching

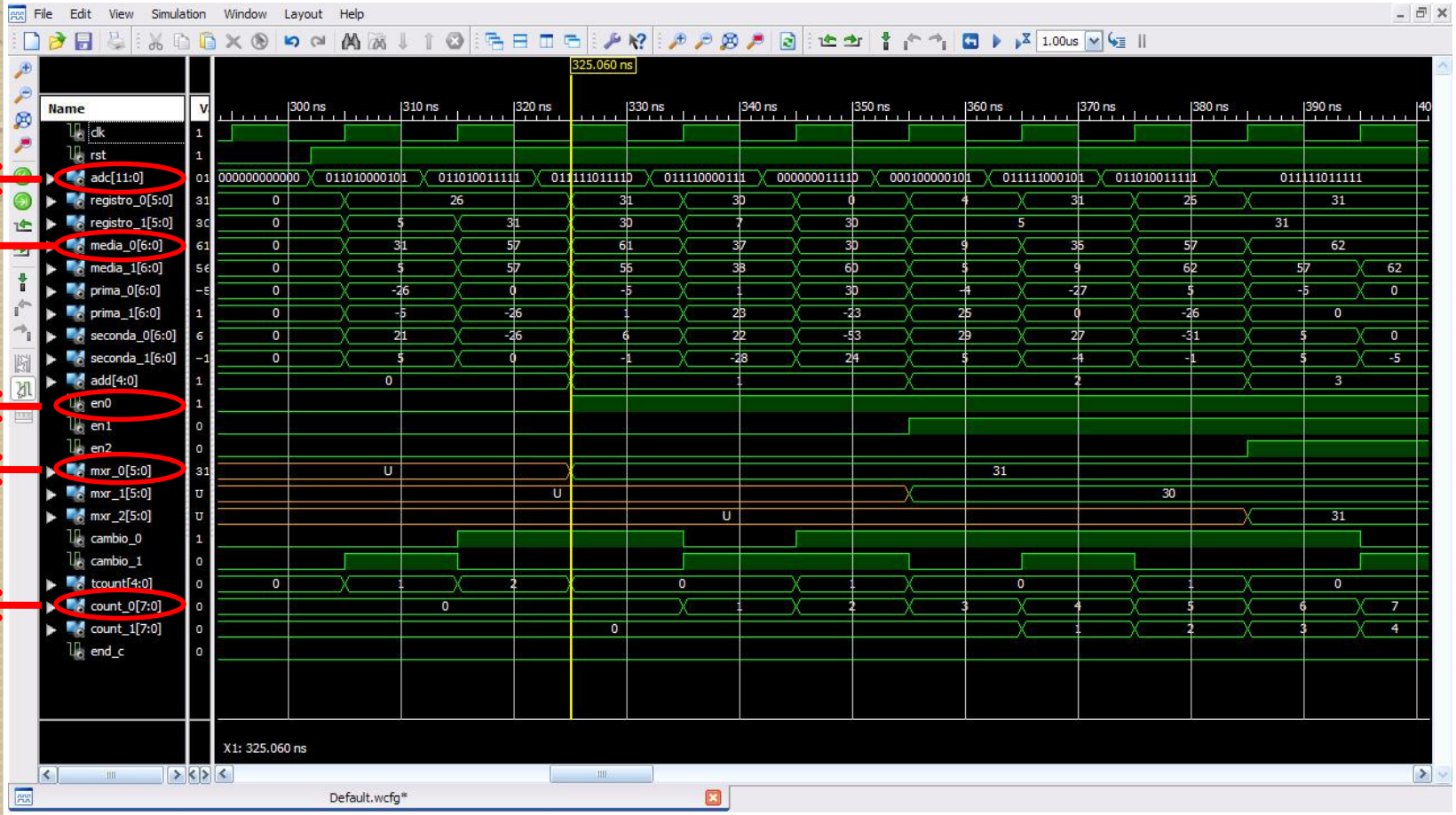
ISE Development Enviroment

- Version 12.4
- HDL-Based Design
- Behavioral Simulation
- Timing Simulation
- Constraints

VHDL Algorithm Overview



VHDL Algorithm – Behavioral Simulation



- Smoothing tuning
- Enable counter
- Max Register
- End counter

VHDL Algorithm – Counter

```
283  expired0 <= counter0(0) and counter0(1) and counter0(2) and counter0(3) and counter0(4)
284              and counter0(5) and counter0(6) and counter0(7);
285  counter_0: process(clk, rst)
286
287     BEGIN
288        IF (rst='0') THEN
289              counter0 <= (others => '0');
290        ELSIF (clk'EVENT AND clk = '1')  THEN
291
292           IF (Enable0='1' and expired0 = '0') then
293              counter0 <= inc_bv(counter0);
294           ELSE
295              counter0<=counter0;
296           END IF;
297
298        END IF;
299  end PROCESS;
300
```

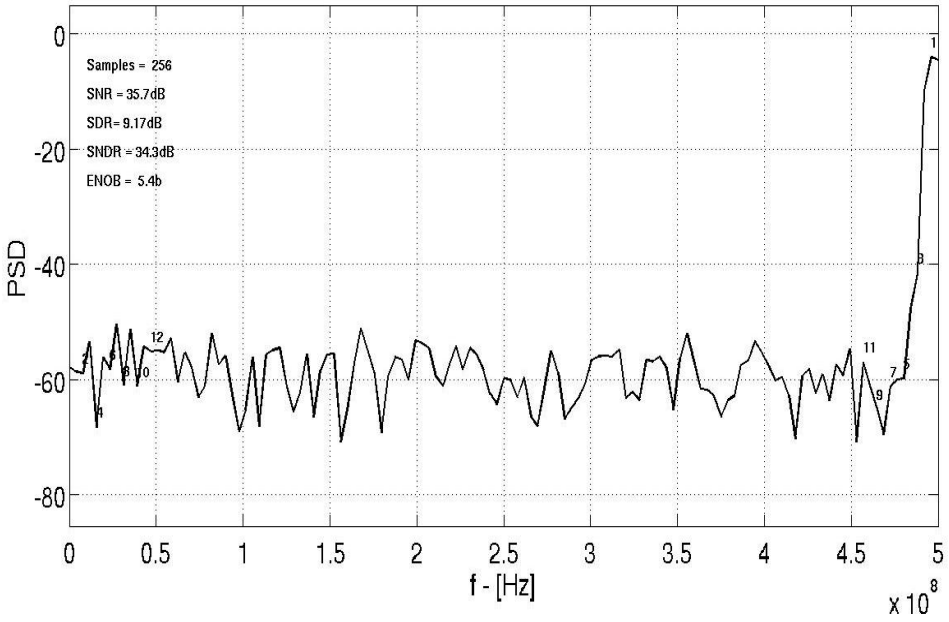
- Triggered by Enable signal
- It gives peak timing information

VHDL Algorithm – Timeout

```
1086  timeout_counter: process (clk, rst, rst_tout)
1087     begin
1088
1089        if ((rst='0')or(rst_tout='1')) then
1090           tout_counter <= (others => '0');
1091           end_counter <= '0';
1092
1093        elsif (clk'EVENT and clk='1') then
1094           if (tout_counter = "11111") then
1095              tout_counter <= tout_counter;
1096              end_counter <= '1';
1097           else
1098              tout_counter <= inc_bv(tout_counter);
1099           end if;
1100
1101        end if;
1102  end process;
1103
```

- It gives the end of the event
- It is reset by rst_tout signal that is set when a peak is found
- End_counter flag

FFT Check Algorithm



- FFT with input signal frequency 500 MHz
- ADC Output Signal vs Virtex 6 Input Signal
- Find potential signal distortions

State of the art

- III Version of ADC chip developed
- VHDL code improvement in progress
  - Timing Simulation
  - Constraints
- FFT Readout algorithm in progress
- Daughter boards layout ready, waiting for realization

Future planning...

- Once the entire chain (ADC + Virtex) will be tested and the VHDL code will be optimized we think to realize a VME board in order to read up to 4 ADC channels.

Thank you
for your attention