DCH FEE

28 chs DCH prototype FEE

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DCH readout chain development status

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Outline

- DCH prototype front-end and HV distribution
  - Requirements
  - Feedthrough lock board
  - Field wires GND boards
  - HV distribution board
  - Signal extraction (decoupling & protection) board
  - Preamplifier board
- Cluster Counting update
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  - Cluster Counting based on FADC
  - Cluster Counting based on derivative circuit
  - Derivative circuit – Simulation result examples
- Readout chain update
  - Readout chain including derivative circuit
  - ADC data readout example
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DCH prototype front-end

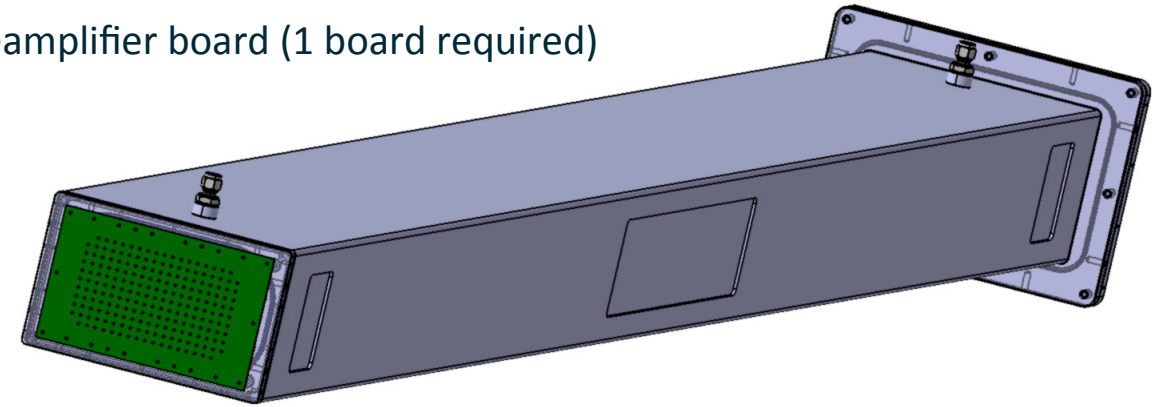
28 chs DCH prototype FEE

Signal amplification requirements

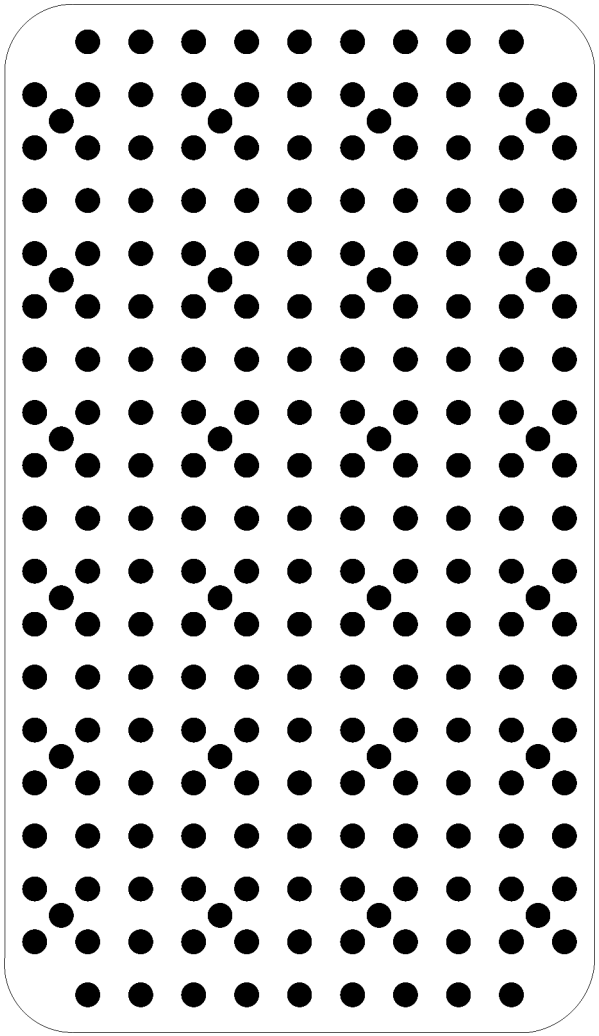
- BW ≥ 250 MHz
- Amplification ≥ 5 mV/fC
- Noise < 2000 erms

On Detector FEE boards

1. Feedthrough lock board (2 boards required)
2. Field wires GND boards (2 boards required)
3. HV distribution board (1 board required)
4. Signal extraction (decoupling & protection) board (1 board required)
5. Preamplifier board (1 board required)



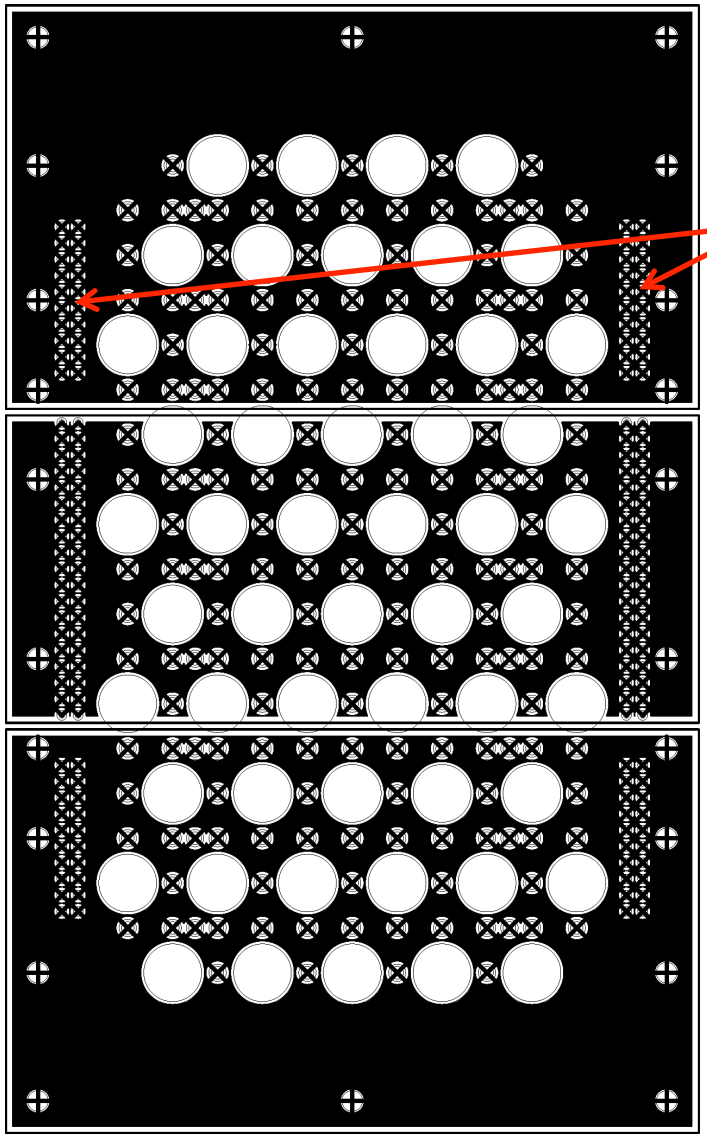
28 chs DCH prototype FEE – Feedthrough lock board



The board is used to lock feed-throughs, in order to avoid stressing (or breaking) wires while working on ground or front-end boards. The lock boards must be anchored on each end-plate.

NB: A similar architecture must be foreseen for the DCH, to avoid accidental damages to the wires when working on FEE boards.

28 chs DCH prototype FEE – Ground board

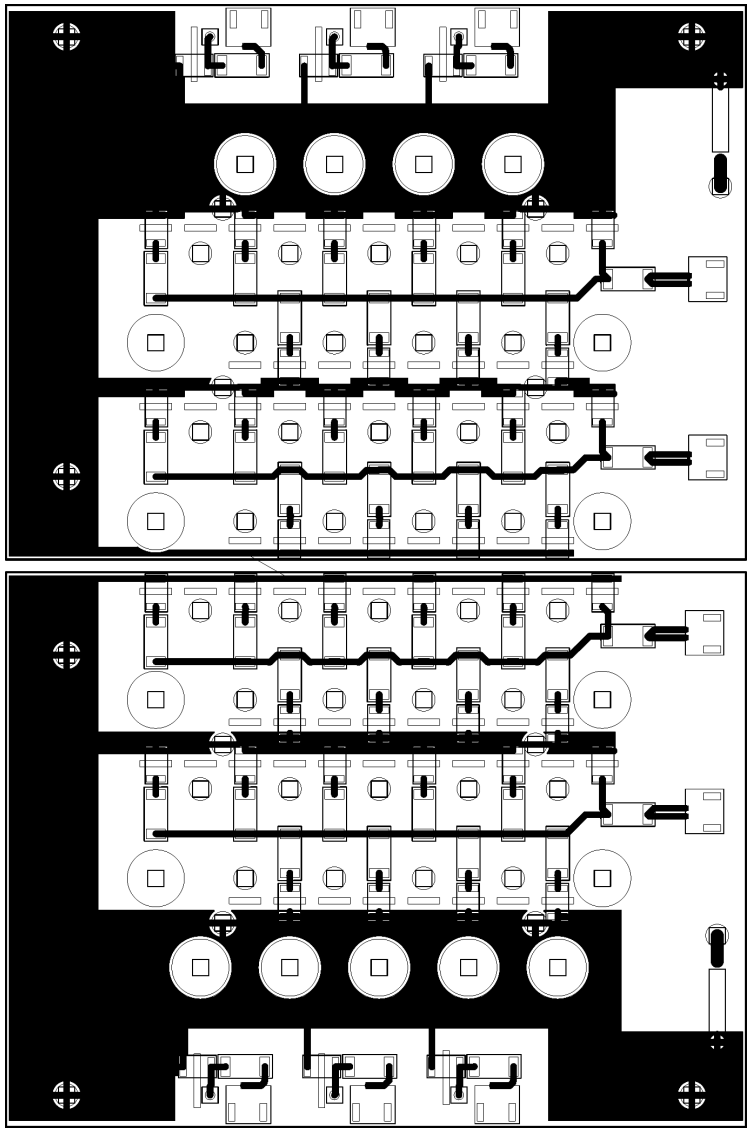


The board is used

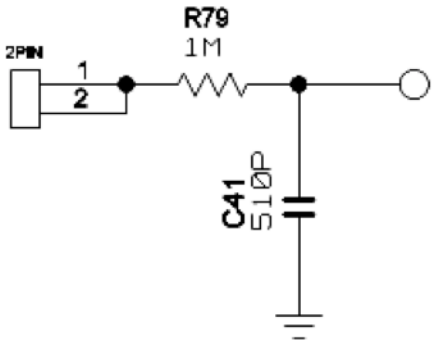
- To connect field wires to GND by means of female connectors soldered on the PCB itself.
- Holes in the board allow for signal extraction and HV distribution by means of appropriate boards.

NB: the same approach can be used for DCH. Dedicated connections will be required for some field wires if we plan to measure wire tension from time to time.

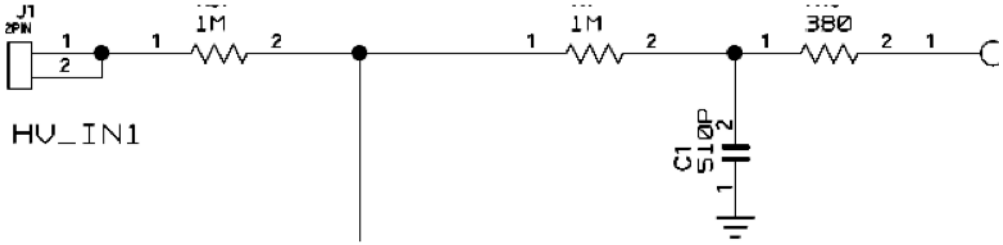
28 chs DCH prototype FEE – HV distribution board



Guard wires

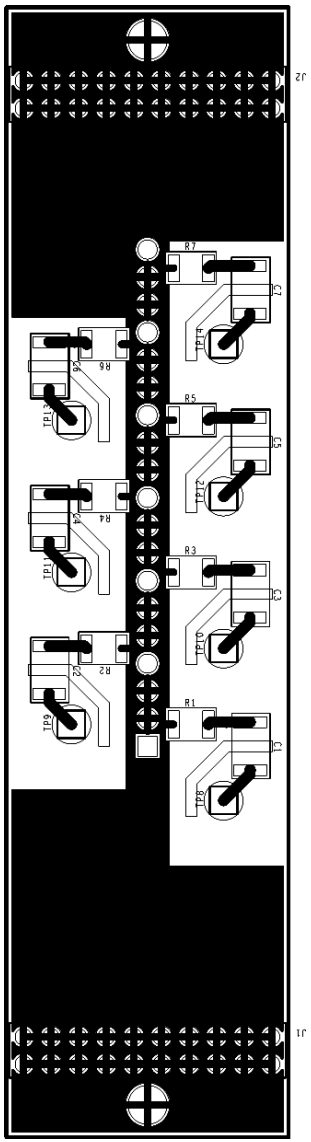


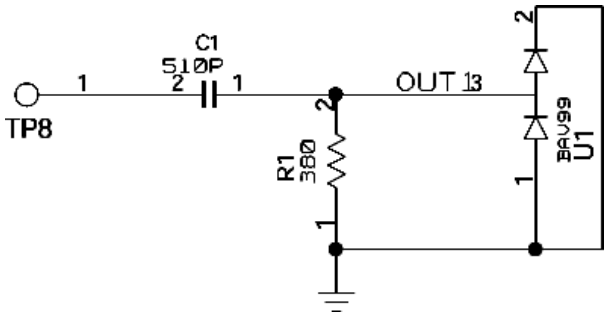
Sense wires



The board provides HV filtering and distribution to sense and guard wires

28 chs DCH prototype FEE – Signal extraction board

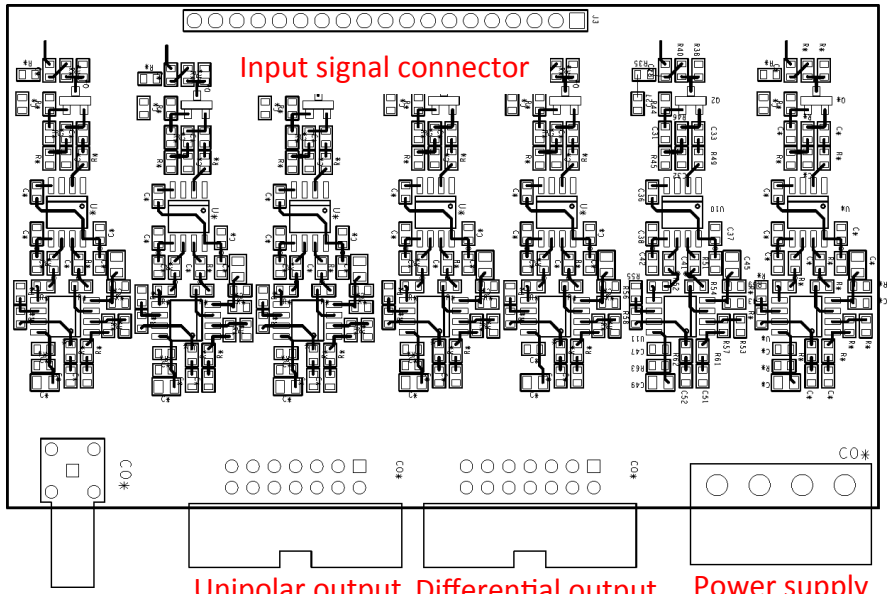




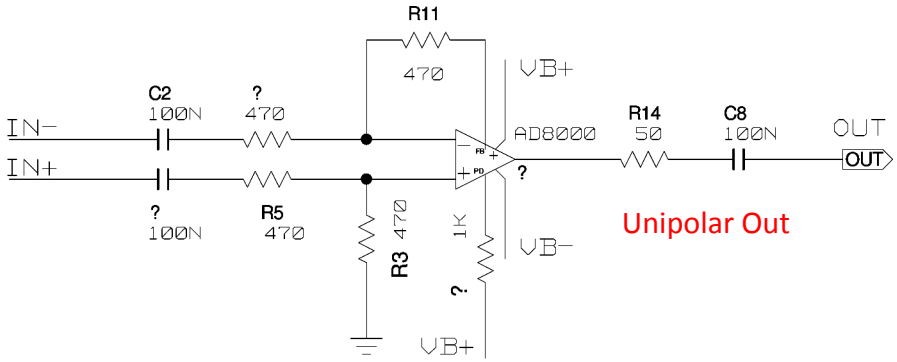
The board is plugged into sense wire feedthrough and GROUND board GND connectors.

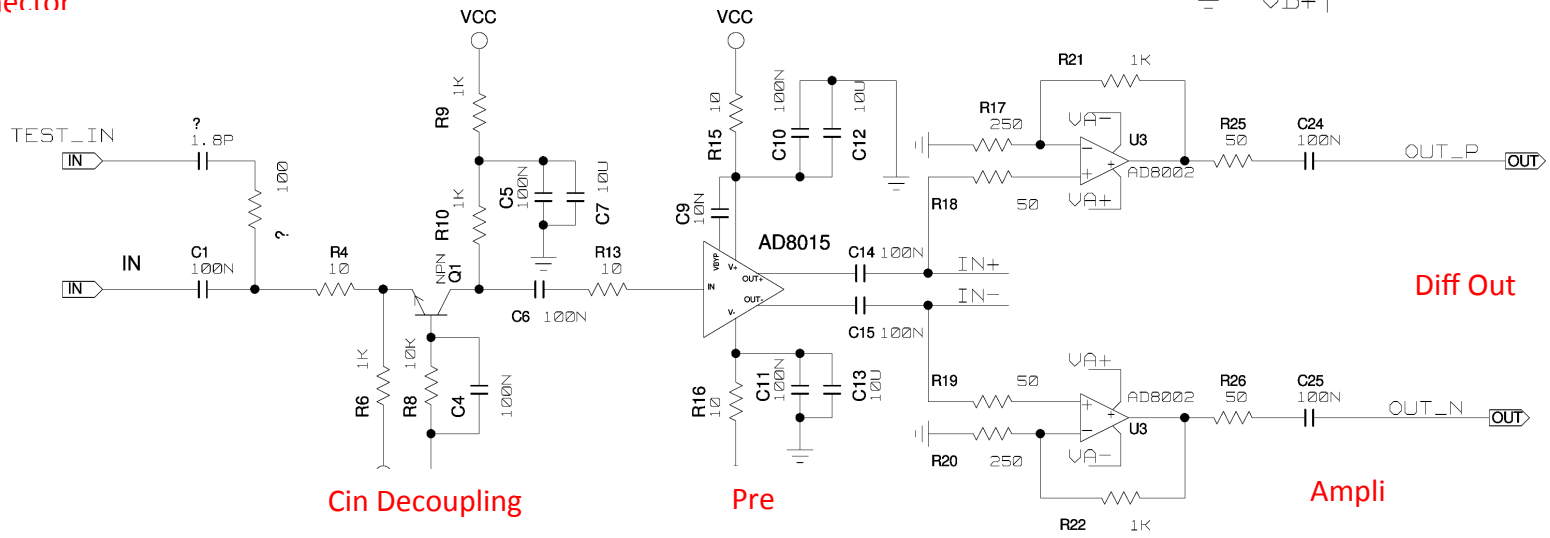
It includes HV decoupling and spark protection circuit

28 chs DCH prototype FEE – Preamplifier board



It is plugged into the signal extraction board and provide amplification to the wire signals





Cluster counting

Cluster counting scenarios

Cluster Counting based on FAST (1 GS) sampling device

Pro

- Flexible data analysis (software/firmware implementation)

Con

- Huge data throughput

Cluster Counting based on derivative method

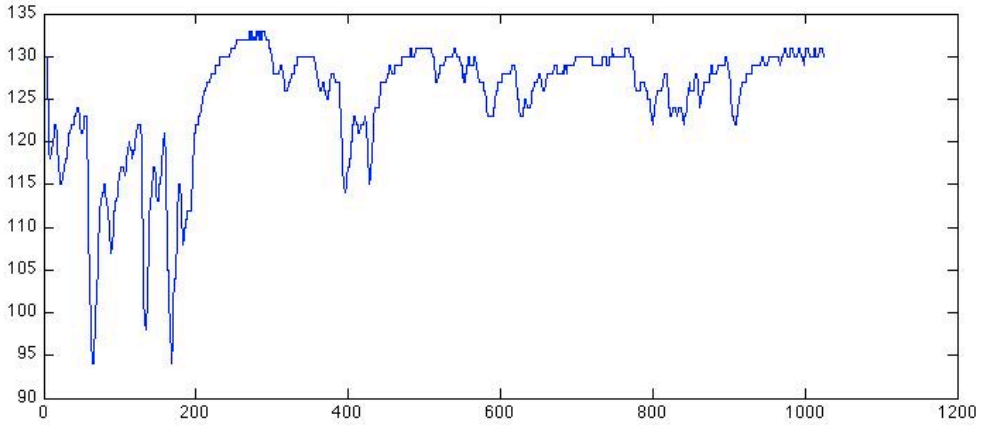
Pro

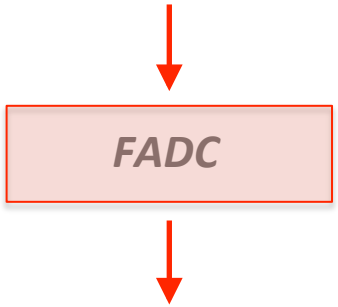
- Easy to integrate in a readout chain (requires a multi-hit TDC)

Con

- Sensitive to channel noise
- Low flexiblity

Cluster counting based on FADC



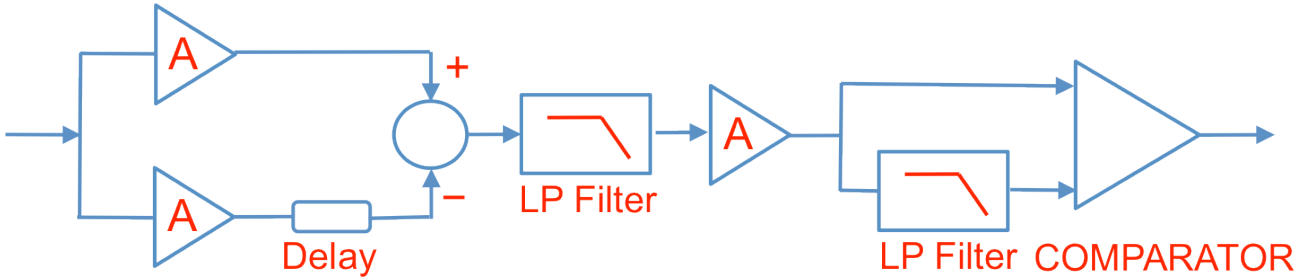


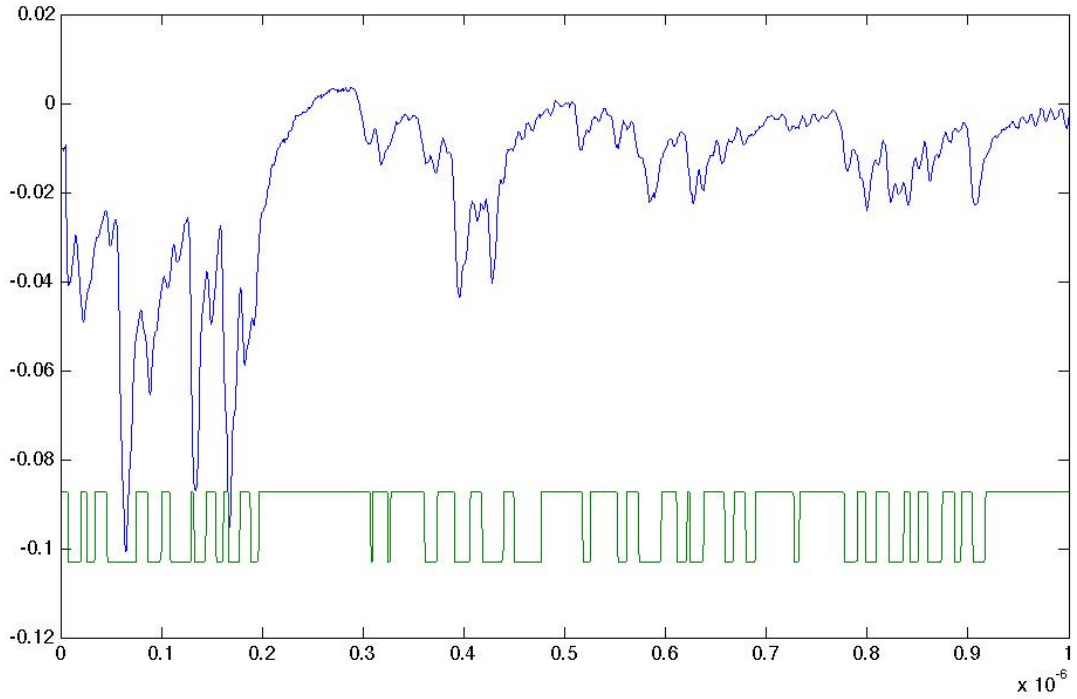
Data throughput (1 µs @ 1 GS)

8 bits (FADC resolution) x 1000 (samples) x 10000 (channels) x 0.1 (occupancy) x 150 kHz (average trigger rate) = 1.2×10^{12} bits/s (→ 600 links @ 2 Gbits/s)

→ FPGA implementation of a fast algorithm required for cluster detecting (→ loss of accuracy in peak detecting)

Cluster Counting based on derivative method

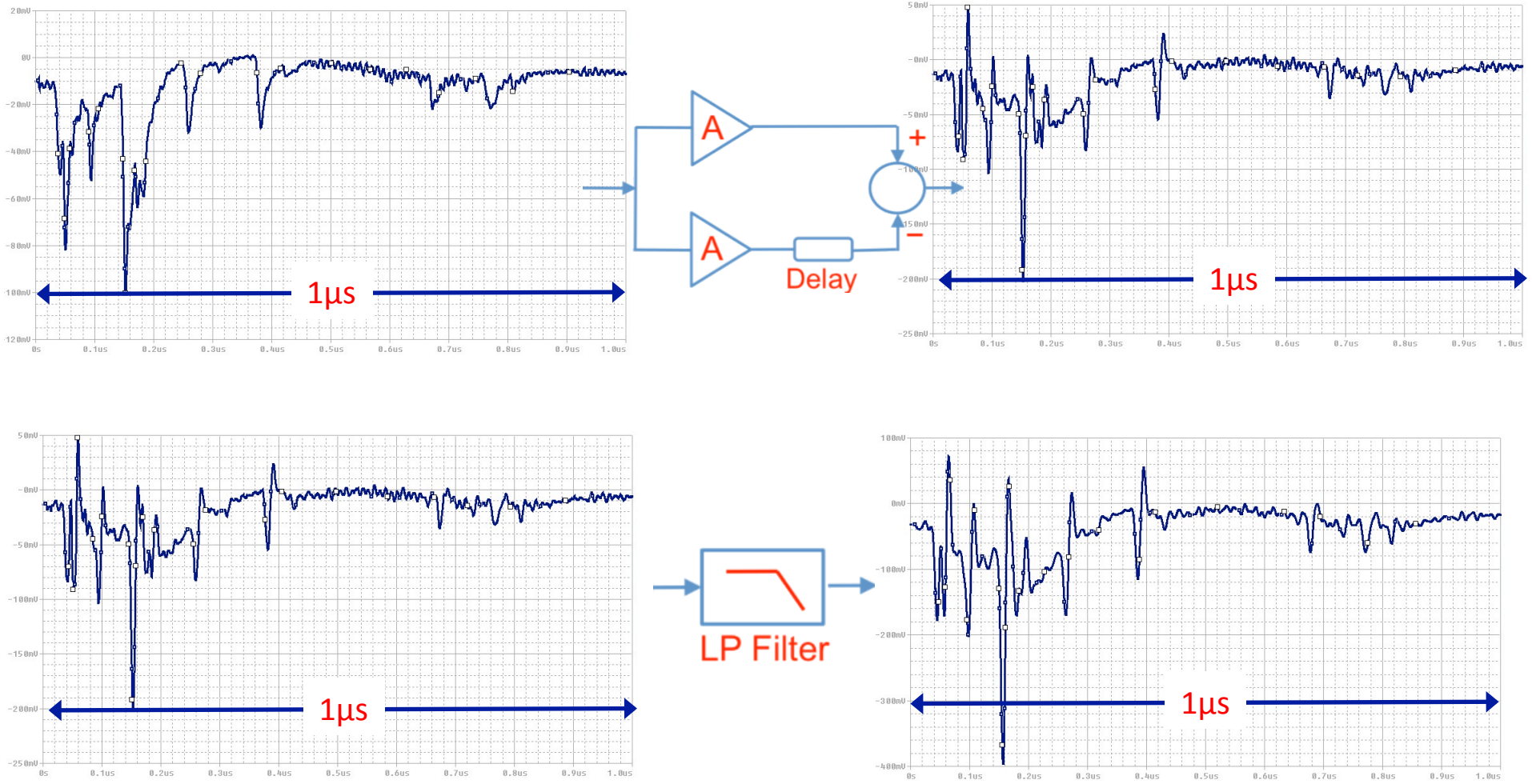




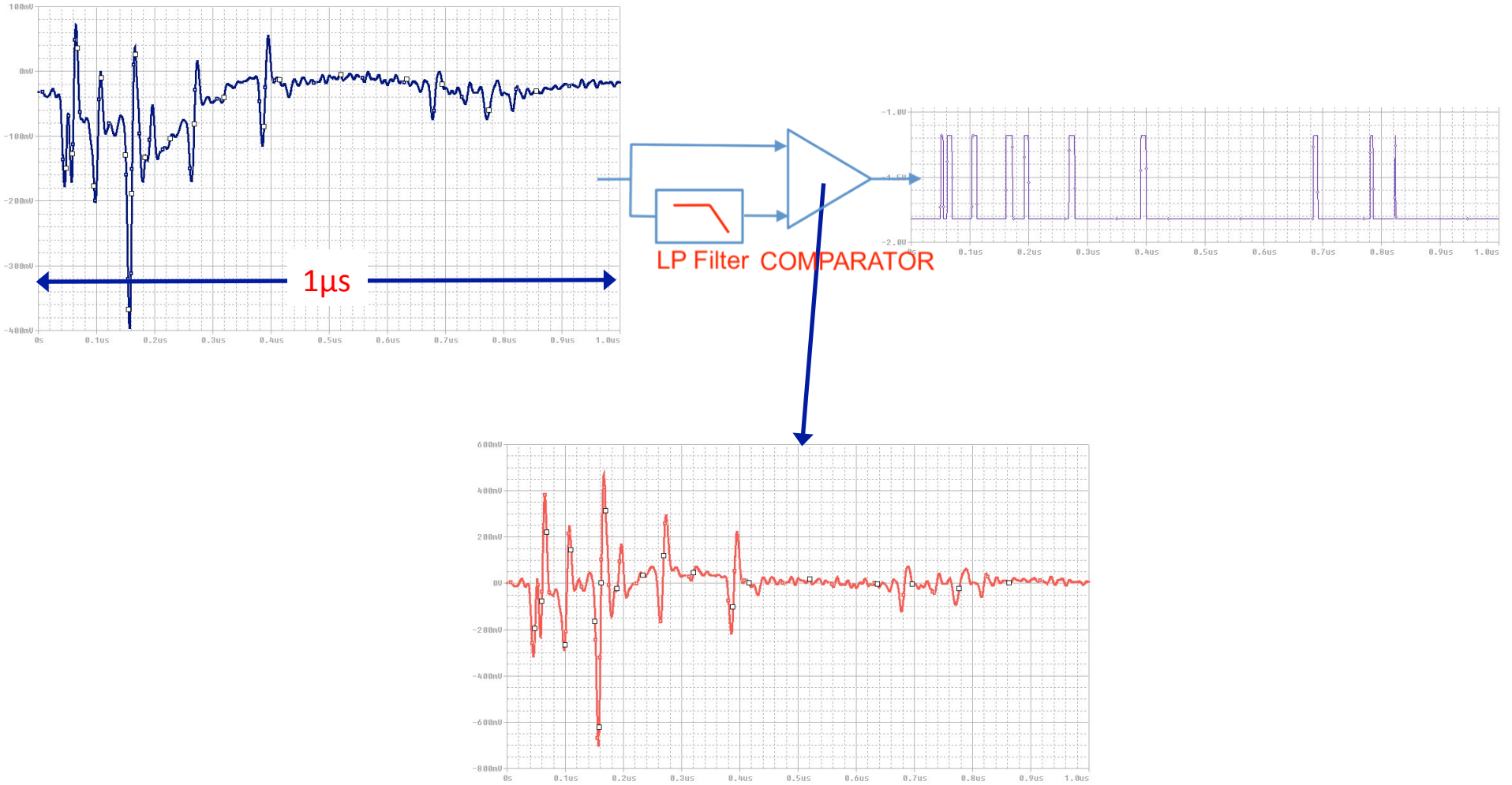
Studies to verify Cluster Counting capability by means derivative circuit are going on.
The method will be extensively tested by means of the 28 chs DCH prototype

How the circuit works (I)

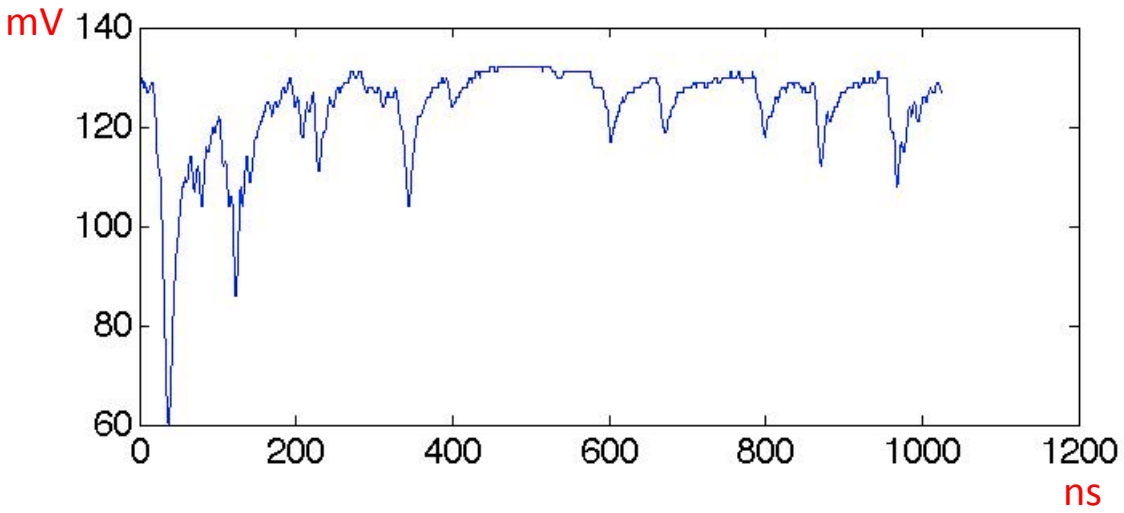
- Pspice simulation
- Signal acquired with DRS digitizer (1 GS)



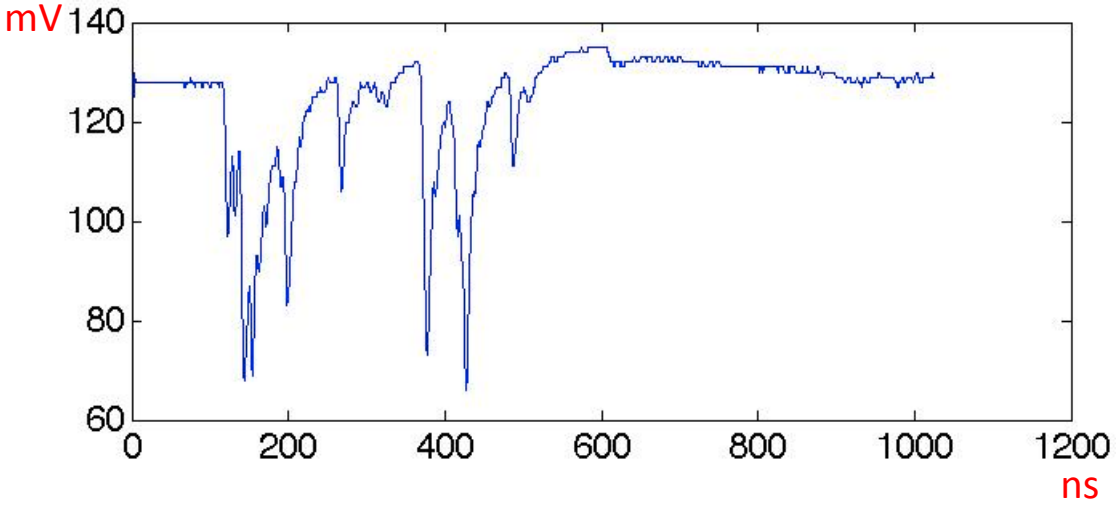
How the circuit works (II)



Derivative circuit - Simulation result examples



Vth	Counts
-10mV	33
-20mV	27
-30mV	21
-40mV	14
-50mV	16
-60mV	16
-80mV	15
-90mV	15
-100m	14

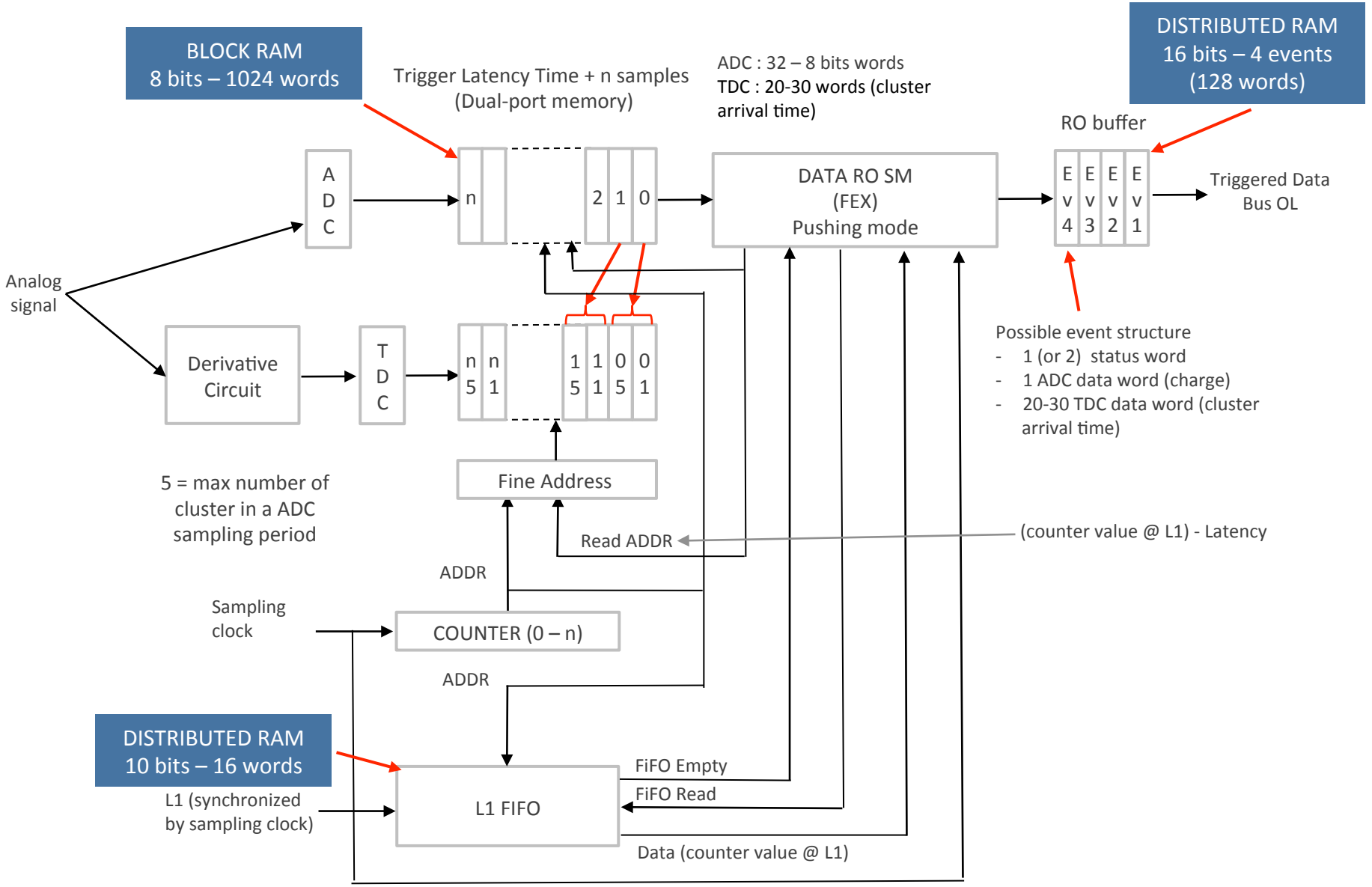


Vth	Counts
-10mV	28
-20mV	24
-30mV	20
-40mV	17
-50mV	15
-60mV	14
-80mV	14
-90mV	12
-100m	11

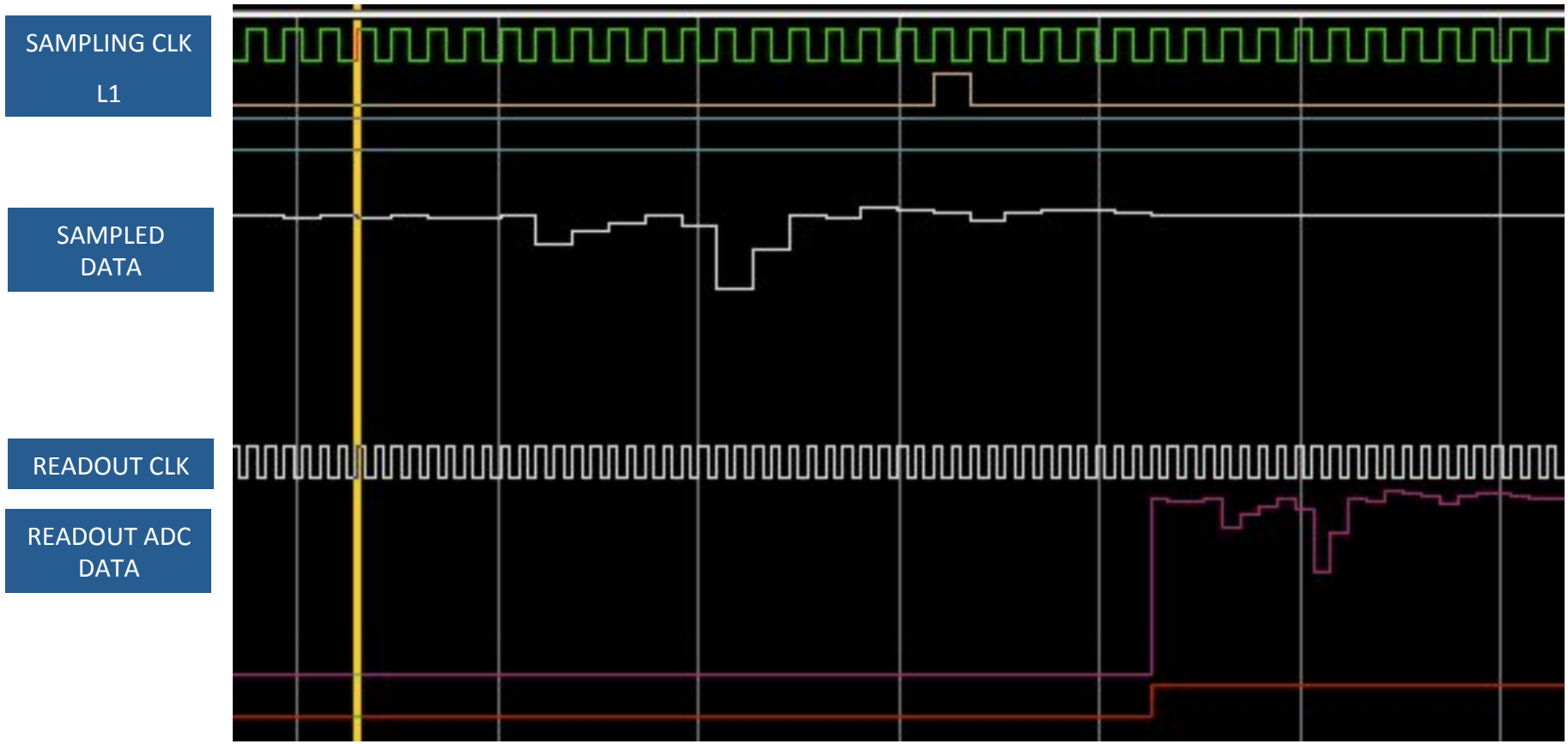
Readout chain implementation based on

Charge ADC, TDC & derivative circuit

Readout chain including derivative circuit



ADC data readout example



Conclusions

- DCH prototype front-end and HV distribution boards have been already designed. Boards production will start within one week.
- DCH prototype will be used to verify cluster counting implementation both using fast digitizer and derivative circuit.
- A new version of derivative circuit has been designed and simulated using (as stimulus file) data acquired by means of DRS digitizer. Simulation with Garfield data are going on to tune circuit parameters.
- Readout chain requires large use of programmable logic (FPGA), then both accurate study of background radiation and radiation tolerant design are required (in our design off-detector readout chain is located near the detector)
- Up to now we focused our attention on off-detector front-end electronics, nevertheless we need also preamplifiers to amplify wire signals …