INFN Istituto Nazionale di Fisica Nucleare
Laboratori Nazionali di Frascati

SuperB

FPGA implementation of a multi-channels, 1 ns time resolution, multi-hit TDC

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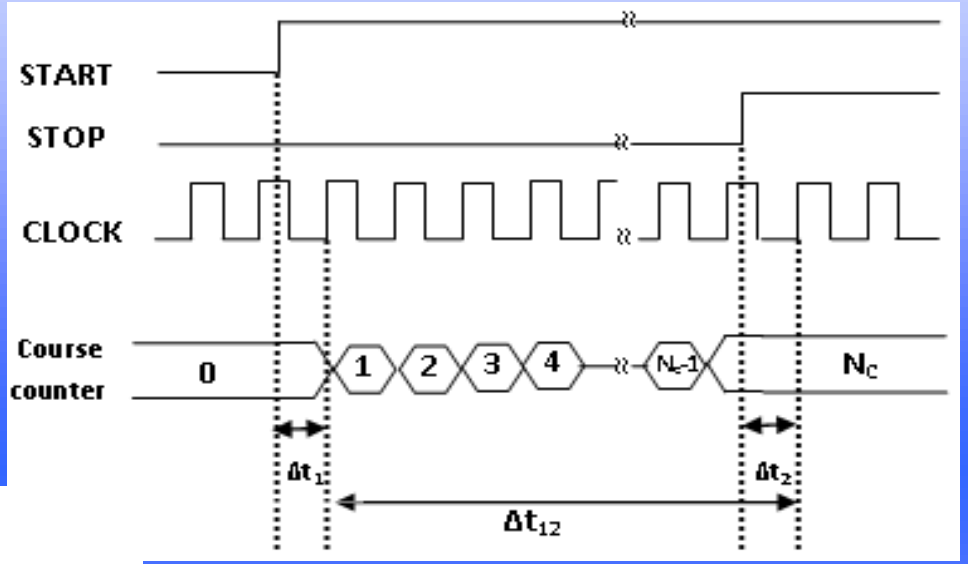
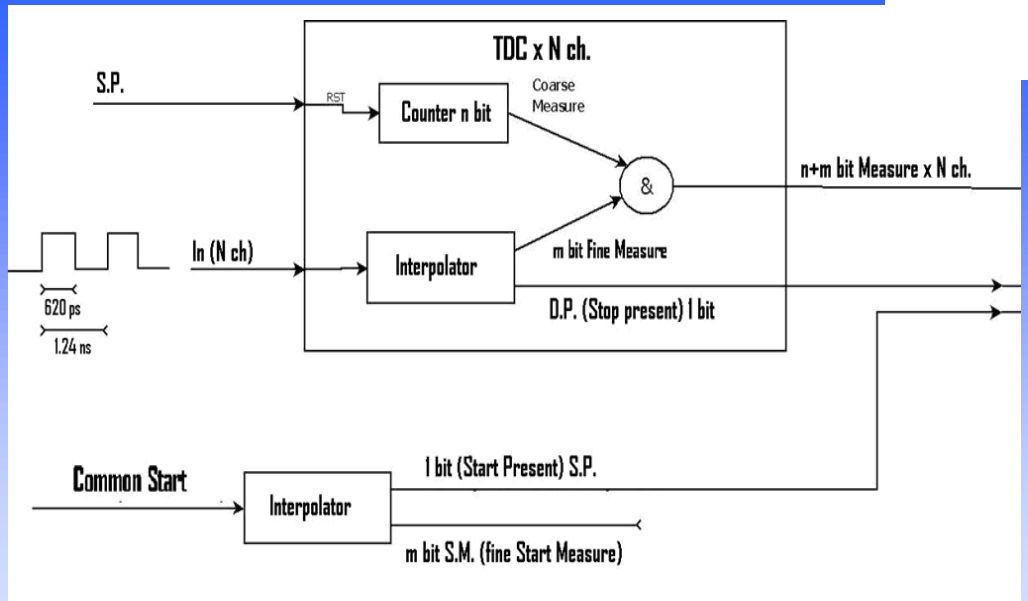
Overview

- TDC architecture
- Interpolator techniques overview
- 4xOversampling interpolator TDC tests and features (developed for HET tagger in KLOE2)
- SuperB DCH requirements
- Conclusions

TDC architecture

- TDC technique: Interpolation.
- Advantage: longer TDC range.

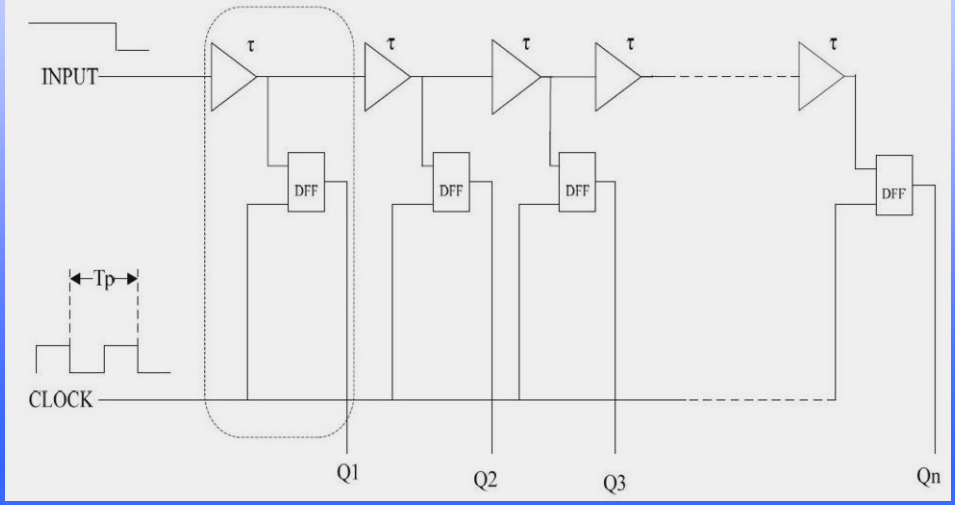


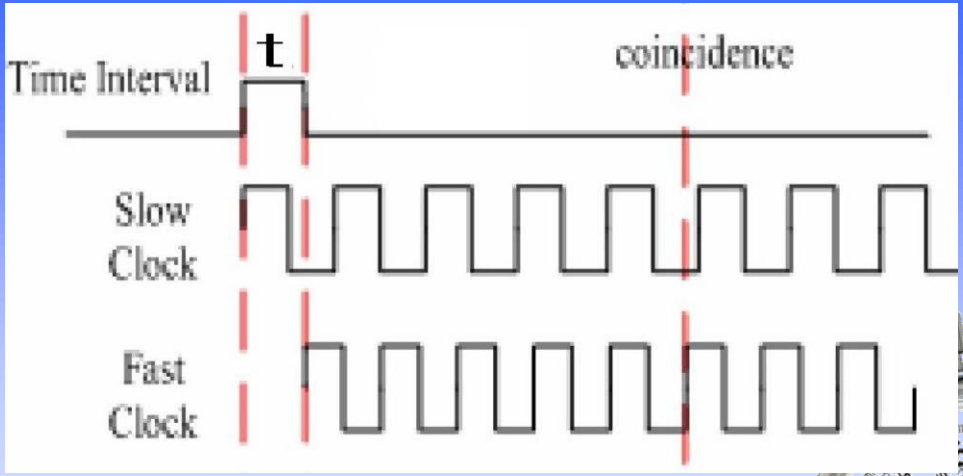


$$t = \Delta t_1 + \Delta t_{12} - \Delta t_2$$

Interpolators

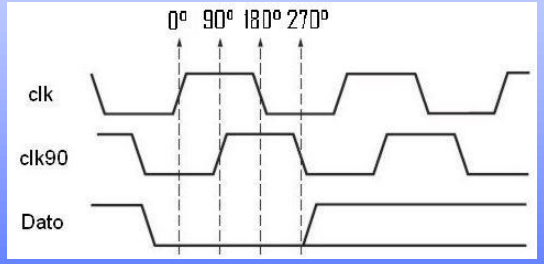
- **Main task**:
  - measure time between input and first clock positive-edge.
- **Interpolator architecture**:
  - different interpolation architectures can be implemented but only digital techniques can be used on FPGA.
- **Family of digital interpolator techniques:**
  - Tapped delay line.
  - Digital time stretching.

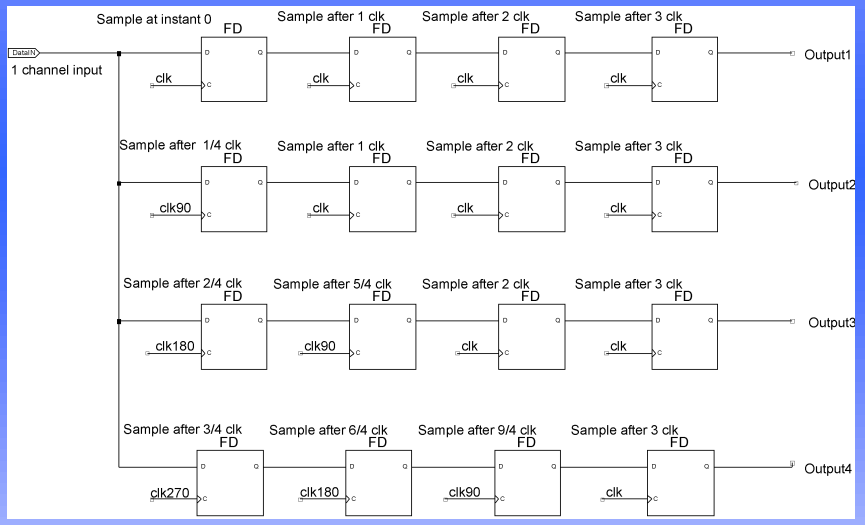


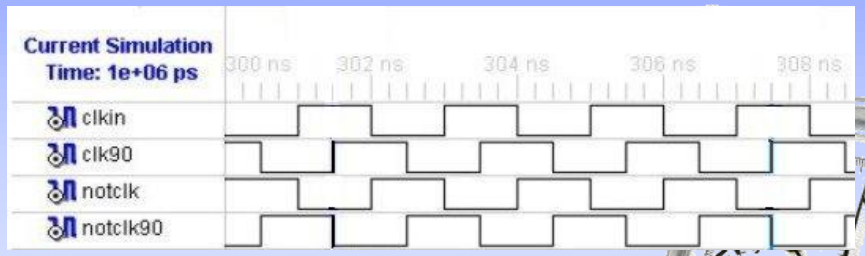


4xOversampler interpolator

- **4xOversampling**:
  - Four samples each clock period.
  - Same technique of tapped delay-line, but the clock is delayed instead of the input.
  - Advantages:
    - **Only one delay-line for many channels;**
    - **Delay line implementable on FPGA embedded DLL;**
    - **Not much logic resources are necessary.**
  - Drawbacks:
    - **input skew increase the DNL error;**
    - **clock jitter decrease the precision**
    - **max-resolution is 500ps with Virtex5.**







4xOversampler interpolator TDC features 1/4

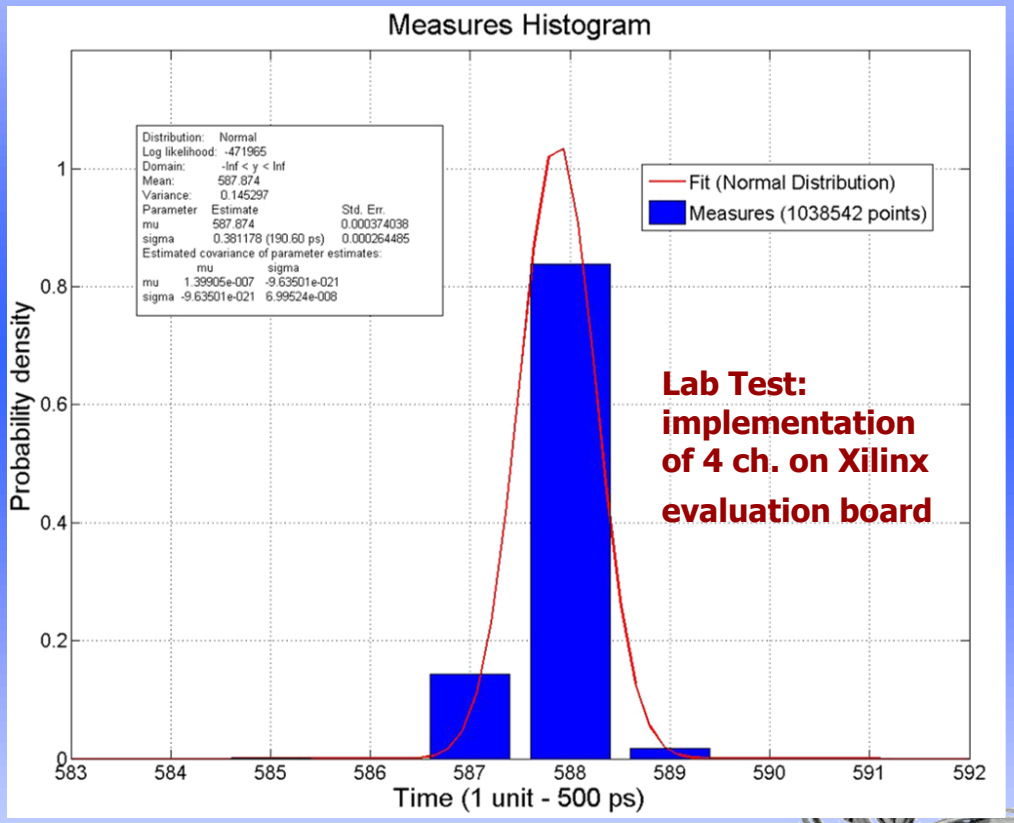
- **Resolution** Smallest time interval that can be resolved in a single measure: $1/4T_{clk}$=625ps (500ps for test only)

- **Precision**

  Standard deviation for repeated measures:

  σ=191ps (measured)

  $\sigma_Q \cong 166$ps (theoretical from quantization error)

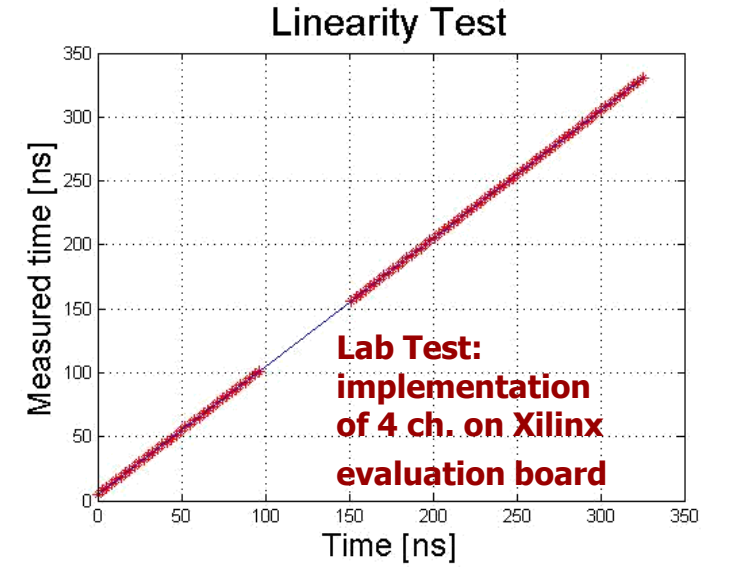


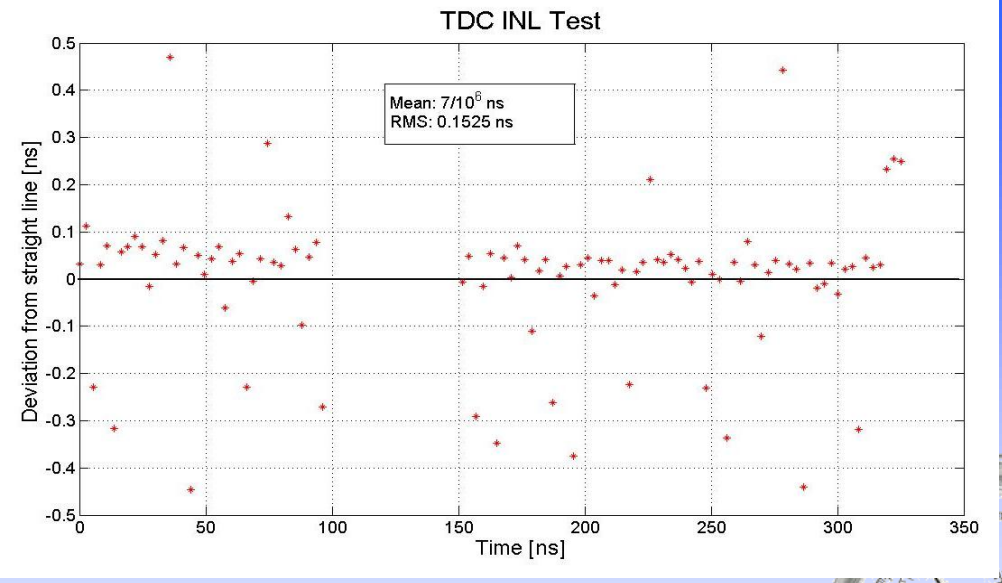
4xOversampler interpolator TDC features 2/4

- **Integral Non Linearity error**: deviation of the input-output characteristic from the ideal straight line.

$$Max\left\{\left|Deviation\right|\right\} = 470\,ps$$

$$RMS\left(Deviation\right) = 150\,ps$$



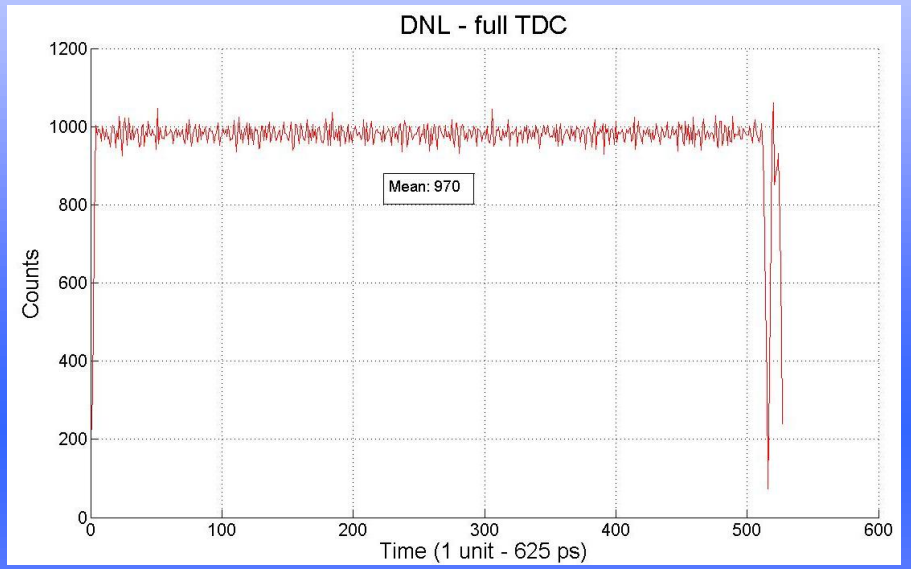


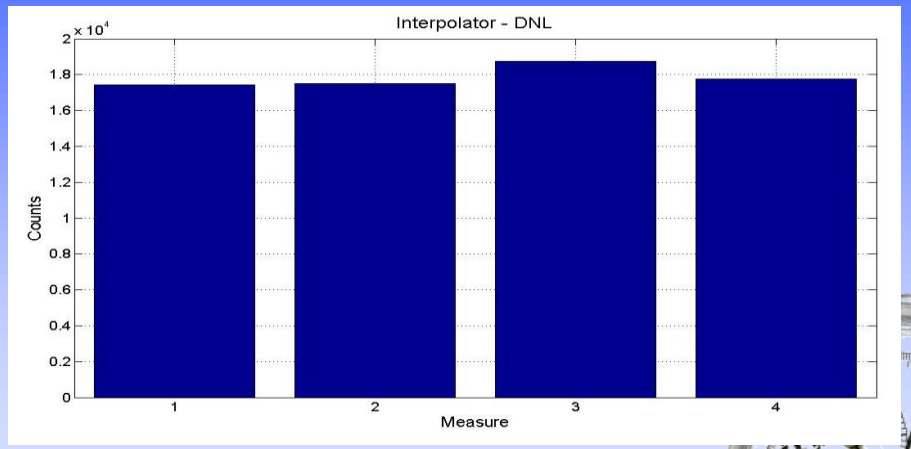
4xOversampler interpolator TDC features 3/4

- **Differential Non Linearity error**: deviation of a single quantization step from the ideal value of 1 LSB.

$$max\left\{\left|\frac{Counts(i)}{Mean}-1\right|\right\}$$

- 0.06 (Full TDC)
- 0.05 (Single interpolator)





4xOversampler interpolator TDC features 4/4

- **Other features**:
  - **Measurement Range**: depends on the number *n* of bits of the counter ($T_{clk} \cdot 2^n$);
  - **Minimum time between two hits**: 1.24ns (for Virtex5);
  - **Number of implementable channels**: depends on the FPGA (kind and package) and on the required logic resources. Up to 128 ch. have been already implemented on a prototype board with Virtex-4 FPGA by SELF group (A.Balla).

Requirements for SuperB drift chamber TDC

- **The developed techniques can be used to match the following SuperB DCH requirements:**
  - Multi-channel
  - Multi-hit
  - Resolution≤1ns
- **New techniques (different devices and fault tolerant design) have to be studied to match the following SuperB DCH requirements:**
  - Radiation tolerance

Conclusions

- Several technique can be used to implement a TDC on an FPGA
- The performances of the 4xOversampling technique agree with the requirements for SuperB DCH
- The same FPGA can be used to implement the read-out system for an ADC
- Radiation tolerant design is under study

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Thank you for attention!

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