Update on SVT activities

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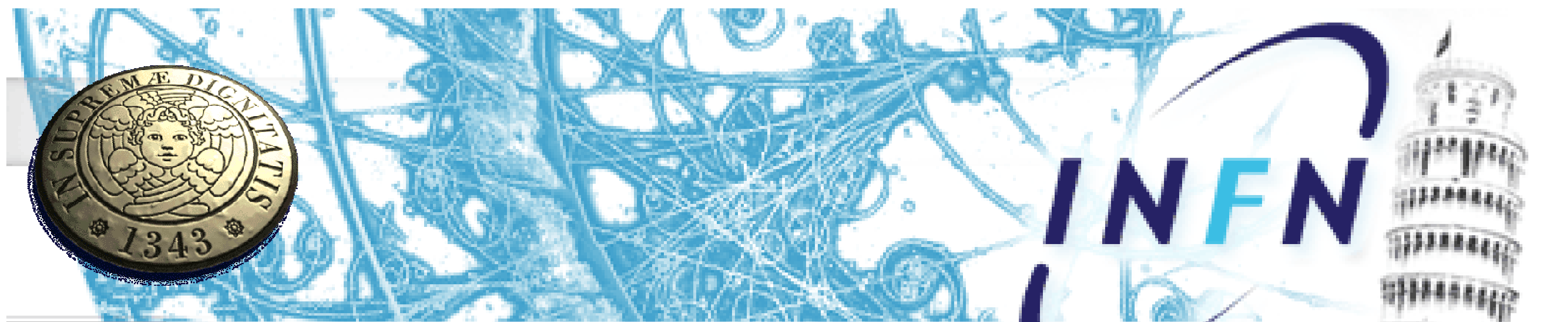
Universita' di Pisa & INFN

on behalf of the SuperB SVT Group



SuperB Workshop INFN-LNF – Plenary session 7th April 2011

Outline

SVT towards the TDR

- Progress in R&D activities reported on the SVT parallel sections:

  - SVT project outlook (G. Rizzo)
  - Update on activities in Pavia (V. Re)
  - First characterization of V.I. MAPS (S. B.)
  - HDI and peripheral electronics (M. Citterio)

  } SVT parallel #1

  - SVT Mechanics (F. Bosi)
  - Update on activities in Torino (D. Gamba)
  - Requirements on FE analog resolution (N. Neri)

  } SVT parallel #2

  - Update on activities in Trieste (L. Vitale)
  - Update on activities in Bologna (F.M. Giorgi)

  } SVT parallel #3

- Conclusions

SVT – project outlook

To finalize the TDR phase into a project ready for the construction, mandatory to go through all the engineering steps of the design, by critically reviewing the (conceptual) solutions to evaluate the critical aspects.

Work out the technical details, as if we had to build now actual prototypes. Only going to a deeper level of design we can spot the real difficulties and properly estimate the needed manpower/time to converge on the whole SVT project.

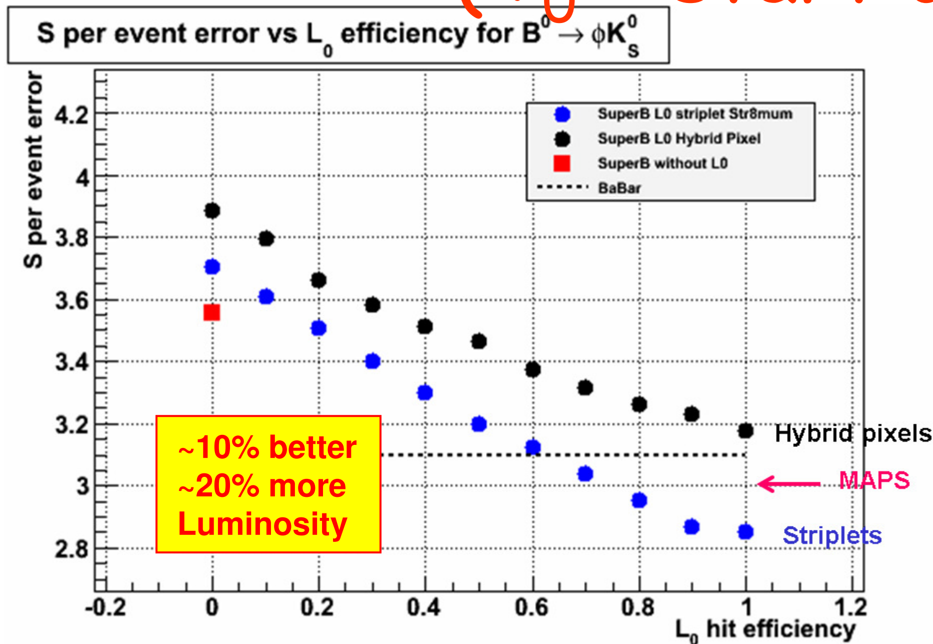
Crucial aspects:

- consider the geom. constraints on SVT by a still-evolving interaction region
- not to take for granted technological choices (i.e. striplets for baseline) before reaching the end of the complete design "exercise"
- re-evaluate the performances implementing close-to-real (i.e. X_0 material) configurations, geometries and resolutions, taking into account reasonable time-projection on T_0 and assumptions on available (always limited) manpower
- make an effort to finalize the current R&D on the more robust options against poorly known experimental bkg. conditions, and evaluate if its' worth investing manpower for boosting more advanced solutions.

Only along the process of engineering the SVT project we can find the solutions to these issues.

G. Rizzo

Layer 0 Striplets vs Hybrid Pixel for T_0 (T_0 = start of data taking)



In the updated plot, expected that difference among striplets and hybrid pixel becomes less important.

Furthermore @ full luminosity expect striplets efficiency ~ 90%

- analog dead time + high background

We need to answer these questions:

- Is an upgrade to pixel really needed?
  - maybe not if we discovered that background is lower than expected so striplets can survive @ full luminosity and after
- Do we really want to build a striplets-L0 just for the first 2 yrs of data taking?
  - A lot of work and manpower is needed since striplets are not easy to build.
  - Development of striplets FE chip could be an issue for T_0.
- Should we instead focus manpower on development needed to have hybrid pixel mature for T_0 (effort helpful to get ready with thin pixels soon after T_0)?
  - Development of FE chip for hybrid pixel could be an issue for T_0, but we need anyway to get FE pixel chip ready for upgrade (T_0 + 2yrs) if striplets cannot survive!

Focus on Work for TDR (I)

Sensors:

- L0 striplets & geom. optimization of L1-5 det. models
- Silicon Sensors Suppliers investigated (4"→6" wafers)

Readout chip (striplets/strip) - critical :

8 months needed to define a robust proposal for the TDR , involving:

- Pavia group design the analog cells (started)
- Fermilab (non-DOI funds needed) or other equivalent group for the digital architecture.
- Document on requirement for strip/striplets FE chips in preparation and already in good shape (→June 2011). Very different specs among layers
  - need to develop 2 new chips: L0/L1-2-3 and L4-5
- Just started to evaluate if readout architecture we developed for pixel could be used for strip and striplets FE chips. Before Elba we must understand that and give a realistic estimate of the Timescale for this VHDL simulation (needed for the TDR).
- Manpower is an issue since same people (BO-PI-PV) are involved in development for pixel chips (chip submission + testbeam)

On detector electronics (Fanout/HDI/transition cards+links)

- Pixel bus development took longer than expected
  - results on bus prototype for pixel module probably available in Oct. 2011
- Realistic design of HDI is starting now after better definition of mechanical/electrical requirements.
- Fanout work for striplets/strips still need to start.
- Manpower is still an issue!

Work to be done for TDR (II)

DAQ: development of the SVT FEB

- Some of the work can be done only after a clear definition of some common SuperB components (FCTS, ECS, links).
- Design can be completed in ~ 10 months

Mechanics:

Manpower extremely critical: need to add ~ 2 FTE mechanical eng. to complete the engineering of the system in 1 yr.

1. Design of Layer 0 modules (striplets and pixel) & beam pipe covered and well advanced. Need 6+2 months.

   Good progress in a realistic design of Layer0 with striplets
   - Mechanical constraints quite stringent
   - HDI design become more challenging

2. Quick dismounting:~ 4 months needed.
3. Design of L1-L5 module & SVT support structure (cones, space-frame …) not started and not covered!
   - 6+6 months needed.

   Important update on Manpower:

   QM (UK) interested in SVT mechanics and some manpower available. Just started to organize the work.

V. Re

R&D on SVT strips readout electronics

- New readout chips with triggered readout of hit strips with analog information are to be designed (layer 0-5, from short strips to long strips)
- Specs are so different from inner to outer SVT layers (signal peaking time, sensor capacitance,…) that two different chips are most probably needed
- Electronic noise estimates show that some more parameter optimization is required for the SVT sensors

Layer	C_D [pF]	t_p [ns]	ENC from R_S [e rms]	ENC [e rms]	Channel width [μm]	Hit rate/strip [kHz]	Efficiency 1/(1+N)
4	52.6	1000	340	820	11370	21.9	0.950
		800	380	870	10730		0.960
		500	490	1000	9430		0.974
5	67.5	1000	500	1010	13500	18.7	0.957
		800	560	1080	12680		0.965
		500	710	1250	11060		0.978

R&D on SVT Layer0 pixels

R&D on advanced pixel sensors for Layer0 is in progress:

- **INMAPS (CMOS 0.18 μm)**

  APSEL-like architecture, deep P-well and high resistivity epilayer to enhance charge collection; submission in preparation

- **CMOS 65 nm**

  Tests have begun on small prototypes (MAPS, fast front-end circuits)

- **Pixels based on 3D integration**

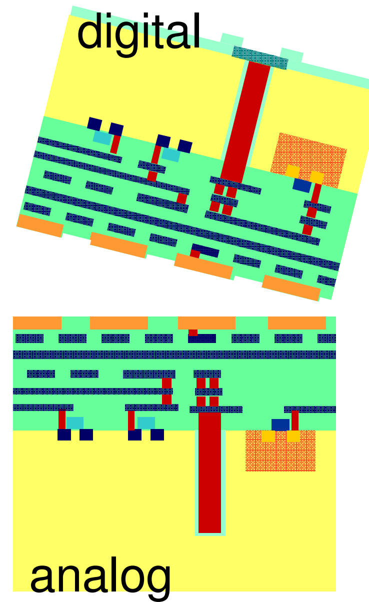
  First Tezzaron/Chartered prototypes are presently in the 3D interconnection stage; a second submission is in preparation with a 3D MAPS and a 3D integrated circuit for high resistivity pixels

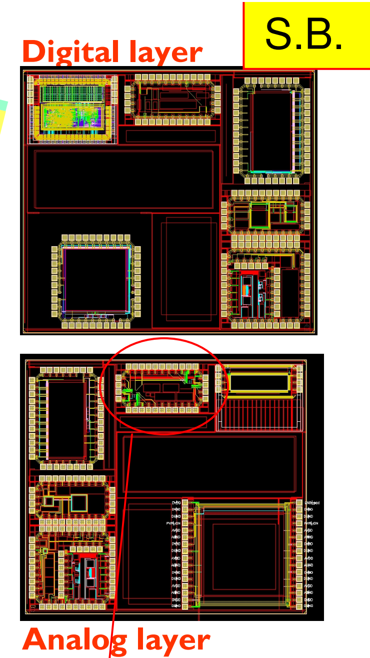
  An alternative 3D technology will be explored by AIDA

First results on MAPS from Chartered/Tezzaron process

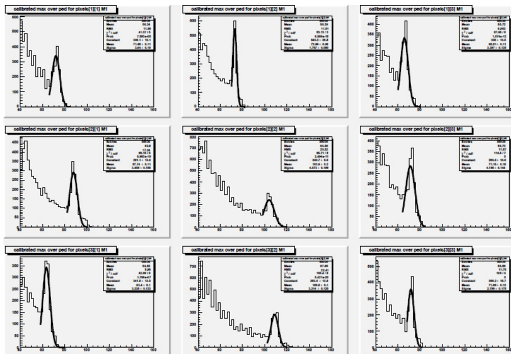
S.B.

- 2D MAPS (same CMOS process used for vertical integration of 3D) now under test:
  - Encouraging results from the characterization of the process

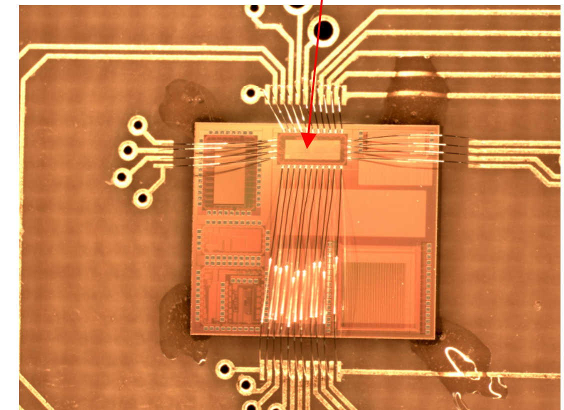




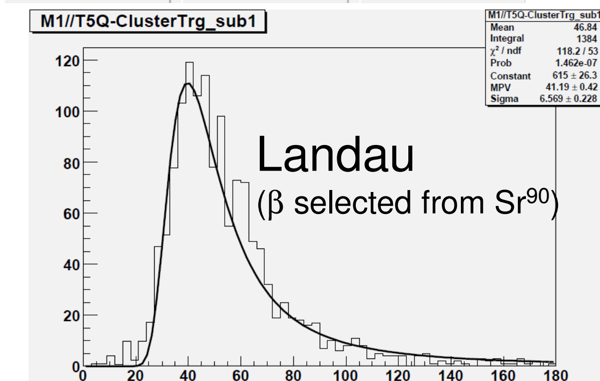
Fe^{55} γ on test (3x3) matrices



M	<μ> [mV]	<σ> [mV]	G [mV/fC]	ΔG/G [%]	<enc> [e-]
1	80	3.4	304	21	44
2	72	2.9	276	20	40



→ ENC~45e-
Gain([mV/fC] ~ 300



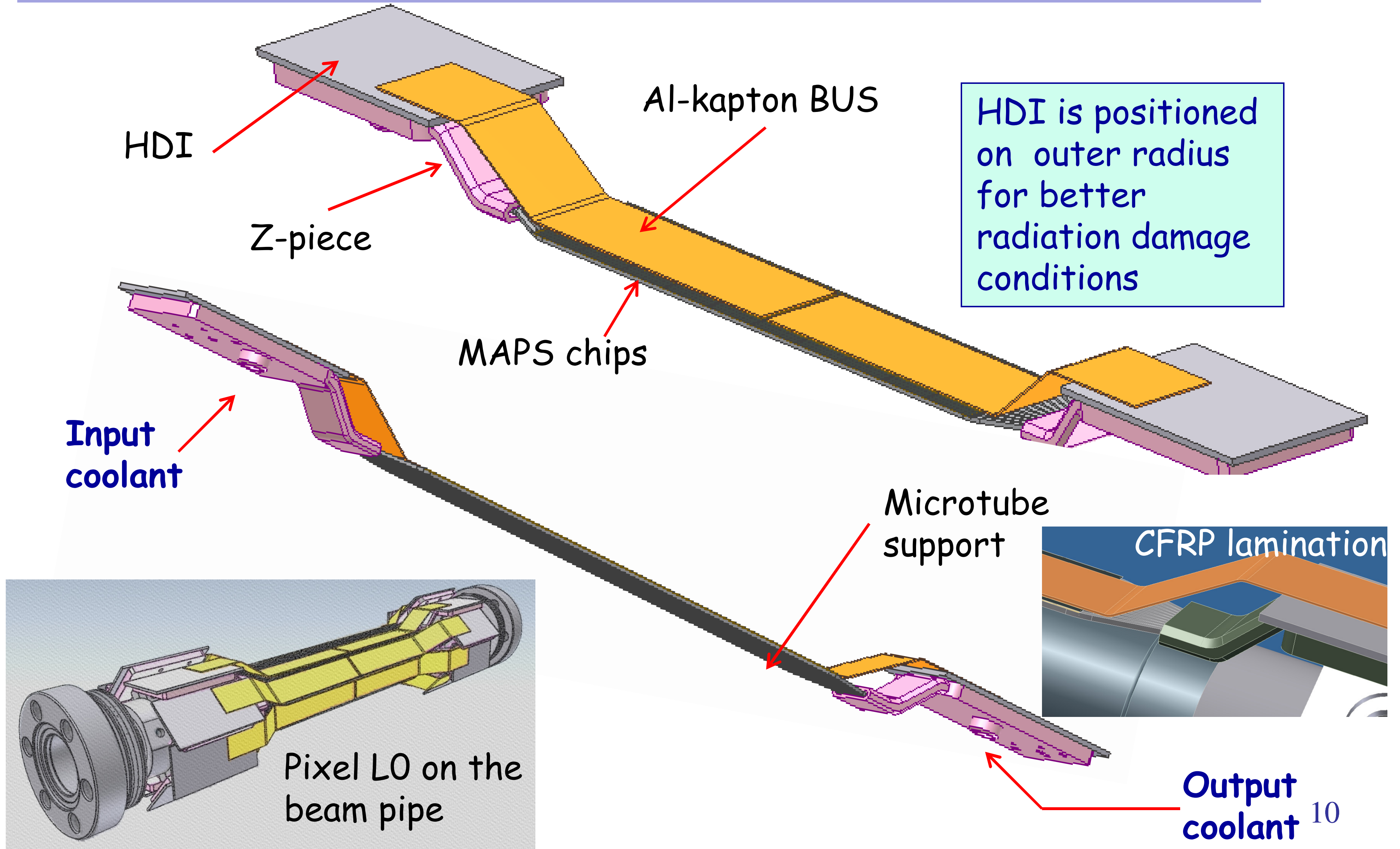
→ First estimate of MIP-signal ~ 800e-

3D wafers coming soon!

Pixel L0 module Design

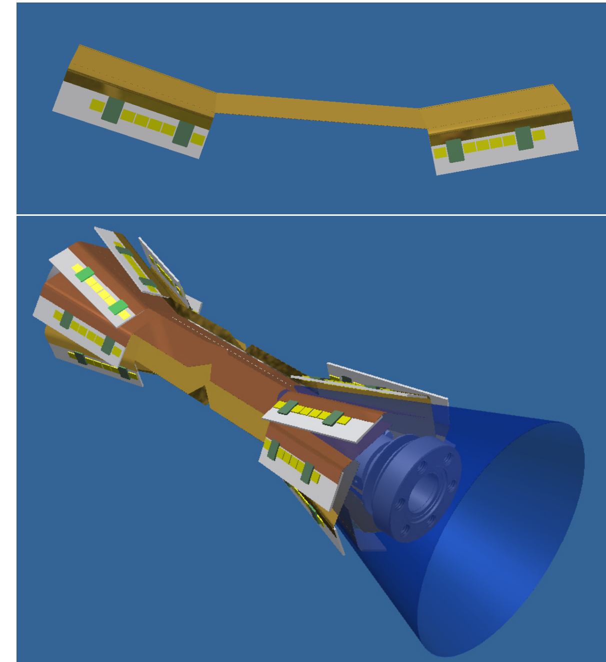
F.Bosi

Necessary thermal-structural simulation to verify L0 module mechanical stability



L0 Striplets module

CDR geometry revisited



Fixing buttons

Sensor position

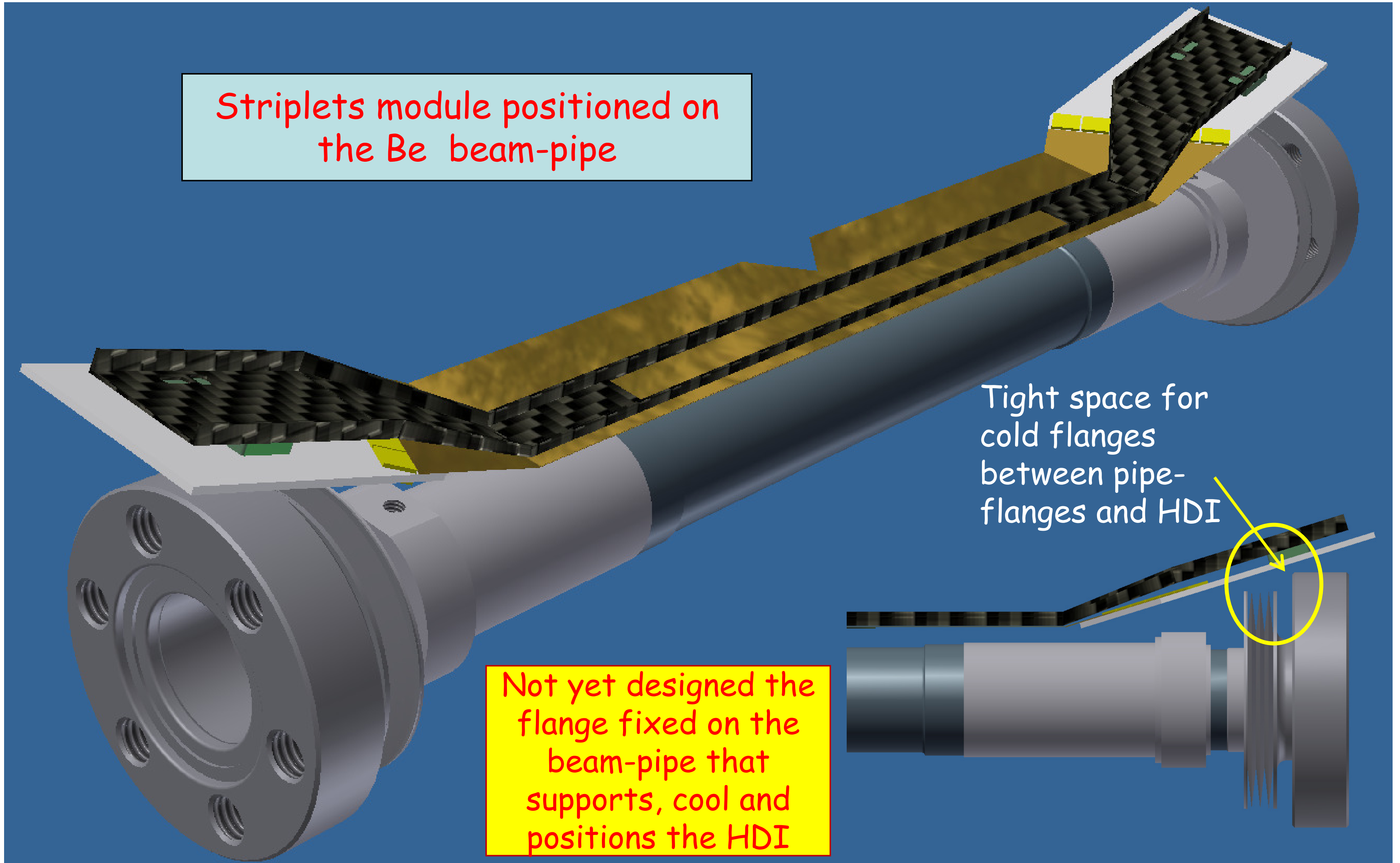
R-ϕ fanout

Front-end chips

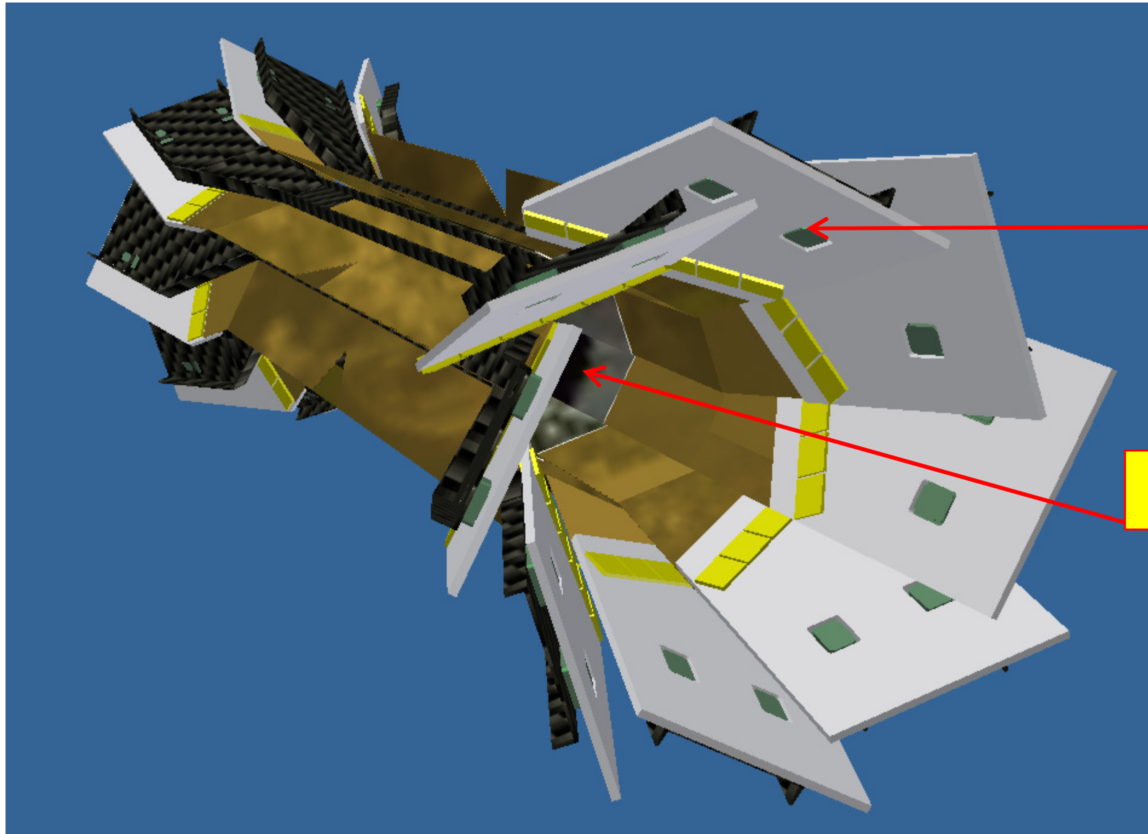
HDI

Final solution: HDI in axial direction tilted at 300 mrad, with front-end chips 30° oriented

Striplets Module



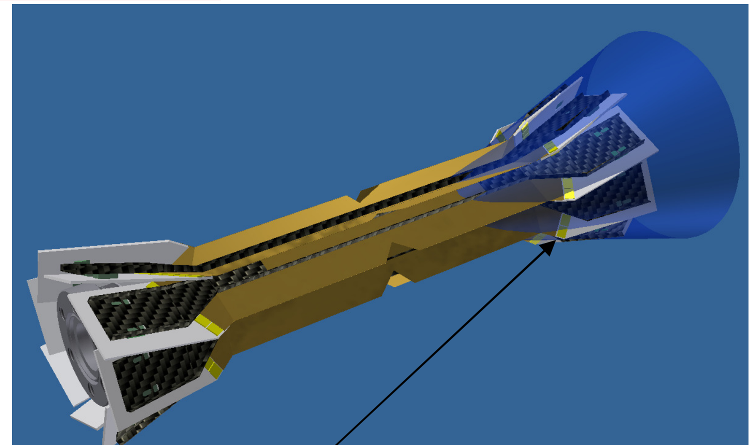
Striplets Modules



Surfaces devoted to couple to the support flange fixed on the beam-pipe

Sensors

In this view are missing the z fanouts to be able to see sensors and the back HDI side



The passive material (1.5 cm^3) outside of 300 mrad cone is 1/3 less of which accepted in Babar

To do list

Need to define the general architecture of the SVT and L0 supports
Tight interaction between machinist and detector engineers.

I.R. engineering design of Be pipe, contacts with Electrofusion company for appropriate brazing technology and evaluation of feasibility of the weldable joint.

Start with engineering work to design the mechanics for quick demounting of the SVT+L0 from the I.R.

Our Goal is to construct a full scale system L0 (maps-strplets) +Al. beam-pipe model to test by thermal point of view at the TFD lab.

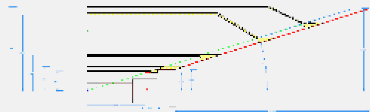
D. Gamba

A preliminar exercise: how many det. types are required to cover 300mr?

Working Hypothesis:

- L0,1,2,3 barrel- L4,5 Arch shaped

Symmetric vs I.P.

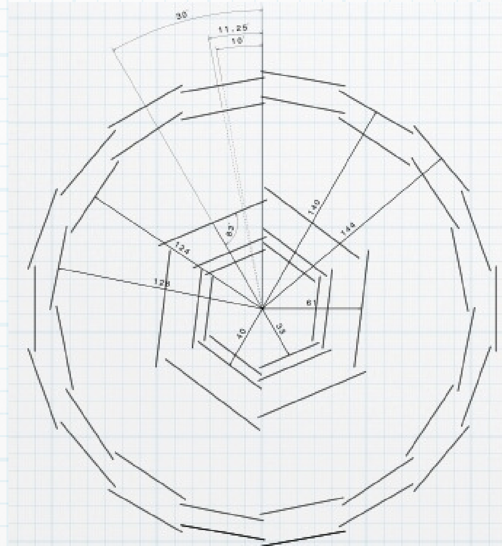


300 mr acceptance

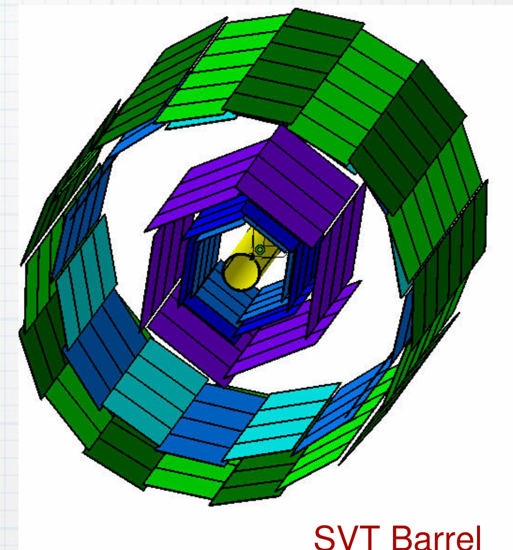
- Det. Fabricated on 6" Si wafers

Minimum # of DSS types: 5

M1 for L1
M2 for L2
M3 for L3
M4 + M5(wedge) for L4&5



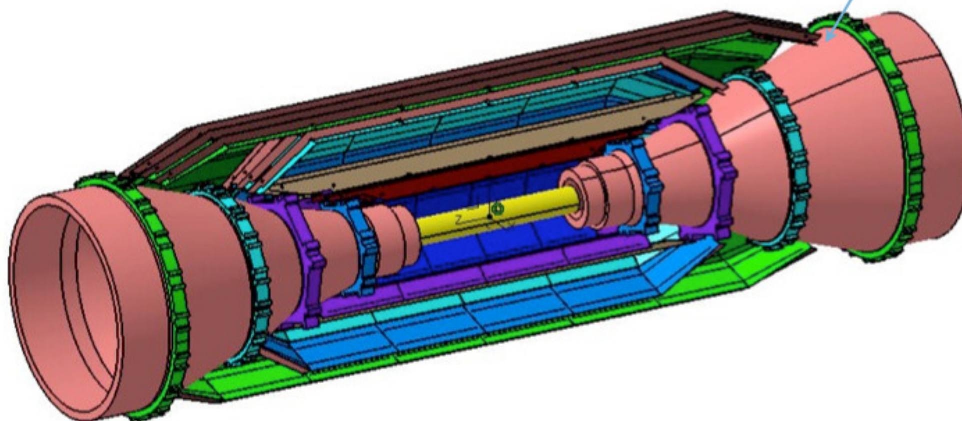
Keep the SVT barrel r-ϕ section

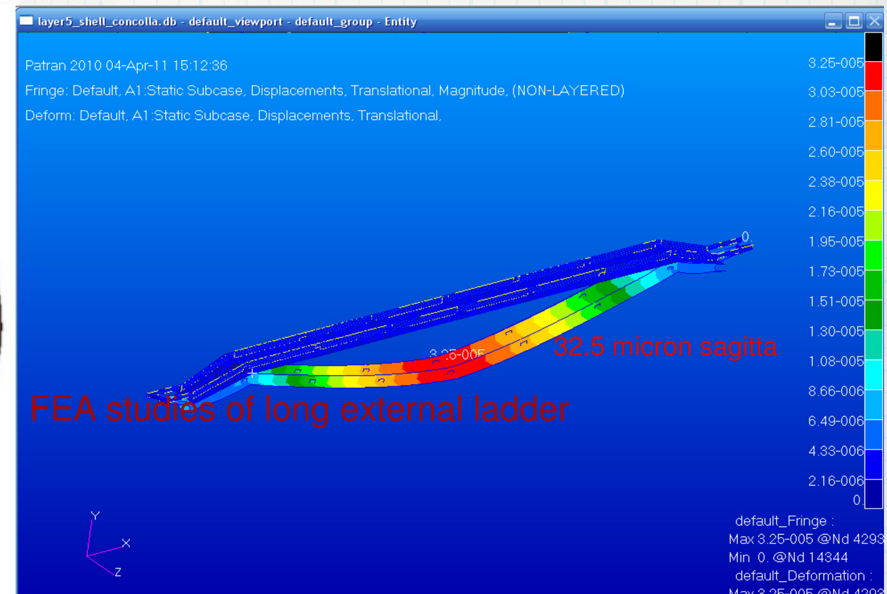


SVT Barrel

End pieces missed

First tentative full SVT drawing (support cone mechanics still to be designed)

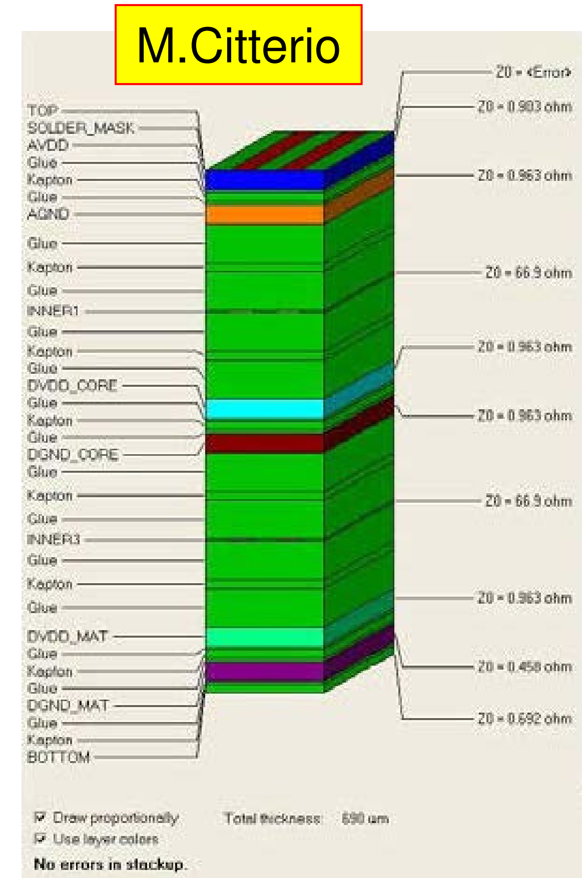


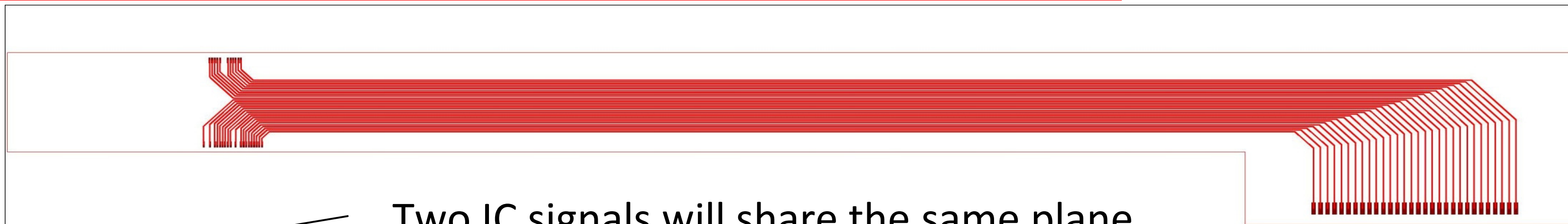


FEA studies of long external ladder

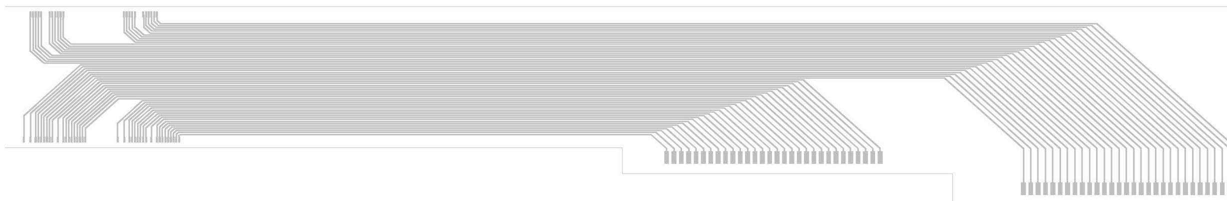
Pixel Bus second generation:

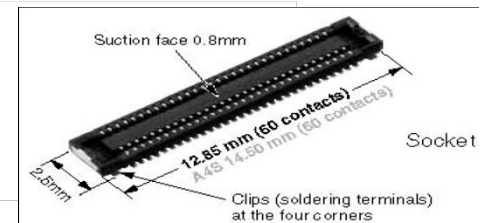
- → Layout details following CERN suggestions
  - → Signal layers used in first prototype were Aluminum (15 um thick and 75 um wide)
  - → Cern is suggesting to adopt Cu (3 um thick, 50 um wide)
  - → Bus will have two signal layers (striplines)
- → Consequences:
  - → BUS with slightly decreased thickness
  - → Two front-end IC lines will be on a same layer
  - → Simulation indicates a maximum “operating frequency” of ~ 130 MHz due to crosstalk
- → Production: it should start soon
  - → Evaluation of process → made on first “sandwich” to verify process parameters
- → Production conclusion estimate → ~ end of June (8-10 weeks)
- → Bus production will give info also for the design of the detector FANOUTs



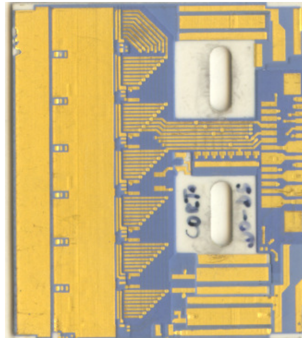


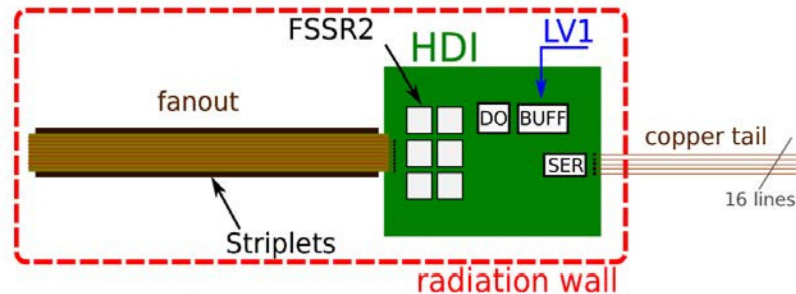
Two IC signals will share the same plane

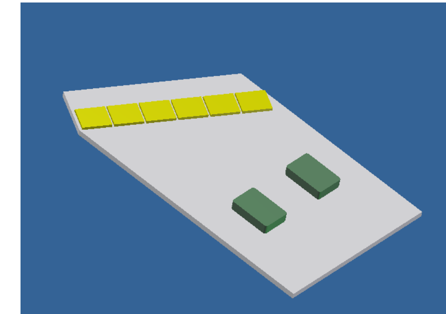




From BABAR to SuperB HDI …







Technology : AlN thick film hybrid	Similar technology for SuperB HDI Maybe new material ….
Detector fan-out is glued on the hybrid edge and chips inputs are wire bonded to the fan-out.	Same approach
Five conductive layers (3 power/ground layers, 2 for signal)	Probably the same number of layers. Maybe one more for HDI-0
Layout rules: - each layer has a thickness of 65 um (15 um conductor and 50 um dielectric) - traces are 15 um thick, 250 um wide - traces pitch is 400 um and pads dimensions are 250 x 400 um'2. - minimum distance between two vias is 400 *um*	Technology has improved in 10 years. We should be able to do better. Of particular interest is the implementation of differential lines

The new HDIs accomodate not only the FE ICs, the passive components but also some ”additional” rad-hard ICs (data organizer, buffers, and serializer) ... at least for the innermost SVT layer.

Some open questions:

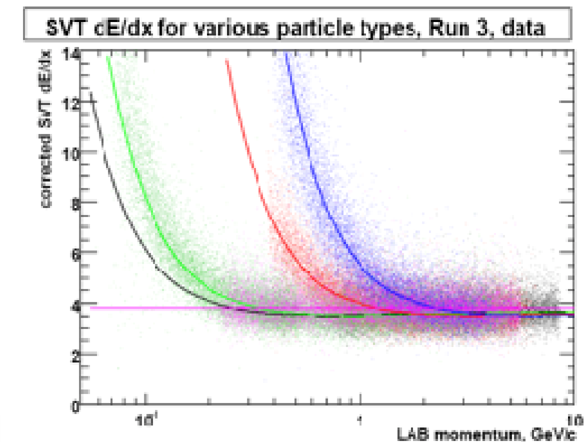
→ How many data lines from the FE ICs are reasonable for a realistic HDI design?
→ Where and how to implement the Data Organizer and the Buffers?
→ What rad-hard serializer (2GBps)?

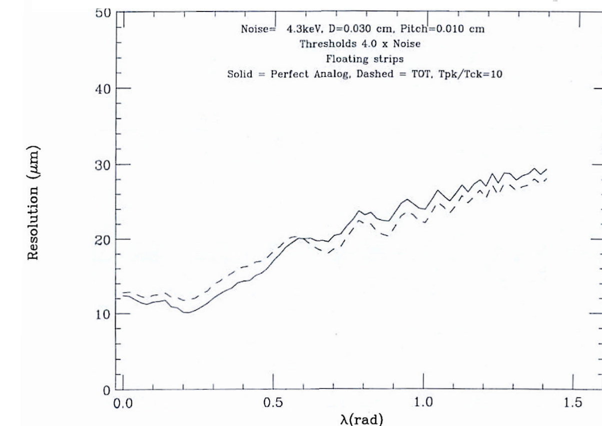
N.Neri

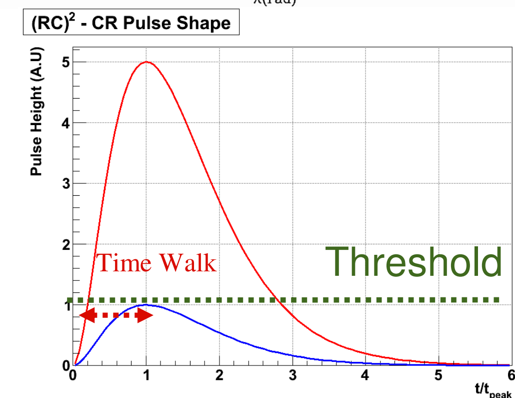
Pulse height information for SVT hits

Relevant information for:

- dE/dx measurements for low momentum tracks with low number of DCH hits (e.g. bkg rejection of electron positron pairs at SuperB);
- improving hit spatial resolution w.r.t. digital information (pitch/√12);
- correcting time walk and improve time resolution of hits. Implications on background reduction for hit reconstruction.







Notes

- dE/dx with SVT measurements is crucial at SuperB for reducing bkg from low p_T electron-positron pairs. This was not the case at BaBar.
- In BaBar, dE/dx measurement with SVT with 4 bit ToT and 10-15 <MIP> Pulse height (Ph) dynamic range allows for 14% resolution for MIPs. There might be room for improvement here. Alternatives to ToT? Flash ADC information?
- With ToT, Ph dynamic range depends on t_{peak}/t_{clk} (~3 in BaBar), on number of ToT bits and finally on ToT response of the chip. A Ph dynamic range of 10-15 <MIP> is required.
- ToT provides excellent information for cluster centroid determination. Compatible with perfect analog information. Difficult to do better in this case.

F.M.Giorgi

PIXEL TEST CHIP SUBMISSIONS

- Architecture tailored on (code branch):
  - APSELVI 96x96
  - APSELVI 96x128
  - SuperPix1 32x128

Area **estimate** with ARM cell library for **TC submission**

Which one? →

CHIP	N. Cells	Cells area (mm2)	RO area (mm2)
APSELVI96x96	78k	0.89	**8.71**
APSELVI96x128	102k	1.12	**11.31**
SuperPX1	68k	0.77	**7.57**

- NB: architecture functionality specifications still need to be closed!
- INMAPS submission: starting to evaluate the Design kit.

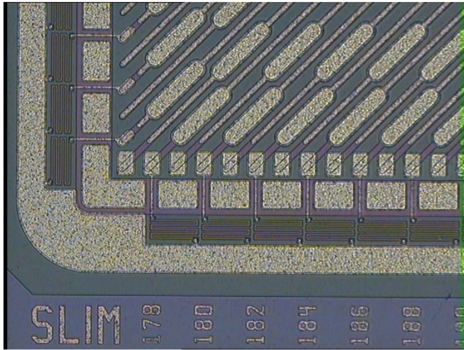
- Test beam 2011 DAQ update in progress
  - Different pixel FE chips have to be tested together. (control by the same Edro Programmable Mezzanine Card)
    - **APSEL4D / 4D_1**
    - **APSEL3D_TC**
    - **SuperPX0**
  - EPMC Firmware upgrade for the required flexibility 70% completed. (to be tested)
  - TDAQ and Configuration software must be updated as well. (process about to start).

EPMC new firmware
- 2 FE module slots
- Specific FE module plug-ins developed for each FE chip to be tested

SPS Operation **Period 5 2011 Sep 12 to Oct 18**

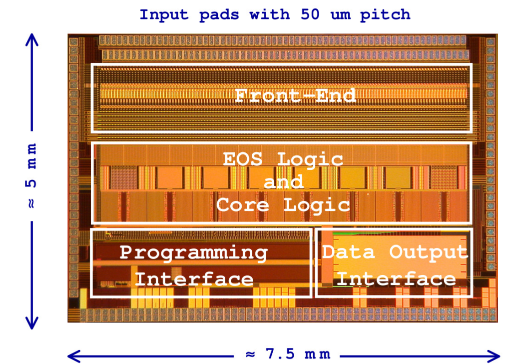
Schedule issue date: 23-Mar-2011 Version 1.0 (colour code: purple (dark) = scheduling meeting , light green (light) = weekend or holiday)

Machine	8 8 BIG MD; 8 2 8 WED MD; 8 2 8 WED MD
T2 -H2	NA61-Protons Z Fodor proton; 8h P Luukka; CMS-SiBT 8h A Malinin; CREAM H2B; 8h CMS-CALO D Lazic
T2 -H4	8h L Schmitt PANDA; 8h M Battaglia SOIPIX; 8h W Lustermann PEBS; 8h H R Schmidt FAIR
T4 -H6	8h R Pestotnik BELLE ARICH; 8h S Bettarini SuperB; 8h H Wilkens ATLAS-IBL; 8h TH Bergauer BELLE II SVD; MONOPIX M W / H W AMMEGAS
T4 -H8	8h E Thomas LHCb CALICE; 8h R Poeschl CALICE; 8h E Thomas LHCb CALICE



L.Vitale

Update on activities in Trieste



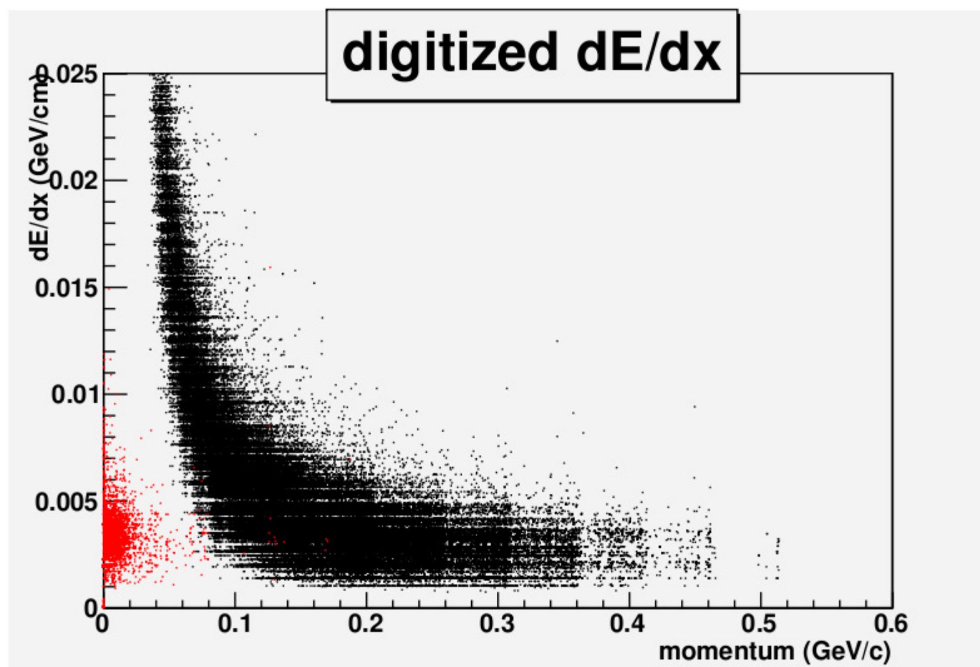
Group is involved in strip(lets) detectors and in DAQ with FSSR2 (still used for beam tests)

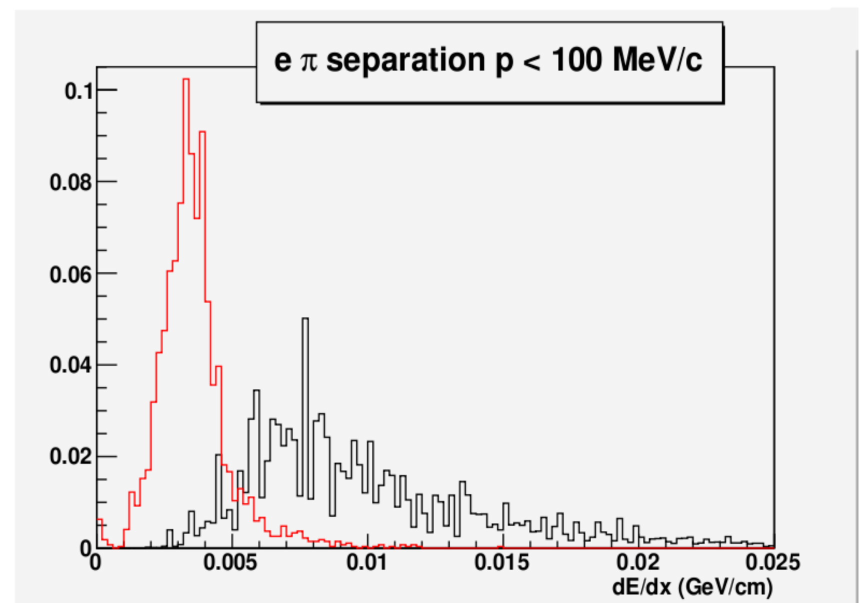
Ongoing activities :

- Sensors and Fanout specifications for the TDR
  - News: it seams feasible to increase the strip metalization thickness to reduce R_{series}
- Beam Test in Sept. (spare telescope modules construction and striplets run)
- dE/dx in SVT Studies with Bruno
- Irradiation tests

dE/dx Studies in SVT

- We tried to "digitize" dE/dx with 3 bits with linear and logarithmic thresholds
- Tools are useful and promising.
- Work still in progress:
  - Quantify the e-π separation within different options





Conclusions

- A lot of activities are ongoing on many items.
- Some critical aspects have been spotted and a lot of work must be done on them, such as:
  - Readout-chip(s)
  - Design of the whole SVT mechanics
- U.K. Institutions started to be more involved on the design of the SVT.
- The SVT group is heavily working toward the TDR.
- Several items have been identified and need more manpower to be completed on time:
  - The group is open to new collaborators/institutions who want to get on board, take responsibilities and find smart solutions to those important SVT issues.