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Analog front-end for Monolithic and Hybrid Pixels in a vertical integration CMOS technology for the SuperB Layer0

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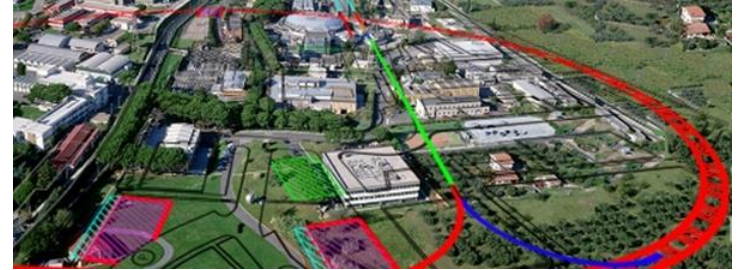**Industriale I-24044**
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Outline

- **Motivation**

- **Vertical Integration (3D) Technologies**

- **DNW MAPS and Hybrid Pixels in 3D Technology**

- **Analog FE for ApselVI 3D MAPS Chip**

- **Analog FE for Superpix1 3D Hybrid Chip**

- **Characterization of SDR1**

- **Conclusion and Plans for the Future**

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Motivation

- The **SuperB Factory**, a high luminosity, e^+ - e^- collider intended for heavy flavour physics studies, has been recently funded by the **Italian Ministry of Education, University and Research** in the framework of the 2011-2013 National Research Plan

A possible site where SuperB experiment will take place: Rome, Italy

- Need for a new **Silicon Vertex Tracker** (very similar to that of the 5 layer BaBar SVT) supplemented by a new **Layer0** to measure the first hit as close as possible to the production vertex. Goal is coverage to 300 mrad both forward and backward

- In the R&D activity for the Layer0 of SuperB, three different approaches are being pursued

  - **Striplets**: thin double sided silicon sensors with short strips (mature technology, not so robust against background)

  - **Hybrid Pixels**: it could become the baseline Layer0 option for the TDR in case MAPS are not considered mature enough by that time. The front-end pitch and the total material budget can be reduced to meet Layer0 requirements

  - **CMOS MAPS**: very promising technology, extensive R&D on Deep N-Well devices 50x50 μm^2 with fast readout architecture

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Vertical Integration (3D) Technologies

- In wafer level 3D processes, **multiple layers of planar devices** are stacked and interconnected using inter-layer connections

- 3D processes offers:
  - extra flexibility in system design placement and routing
  - improved packing density
  - reduced parasitics
  - crosstalk immunity
  - reduced power
  - ability to implement added functionality
  - fabrication process optimized by tier function

- The 130 nm CMOS process is provided by Chartered Semiconductor (now part of Globalfoundries). Vertical integration of the wafers is manufactured by Tezzaron Semiconductor

- Tezzaron's 3D solutions:
  - wafer-level stacking
  - via-first approach
  - metal-to-metal thermal bonding with copper

- Key 3D technologies:
  - bonding between layers
  - wafer thinning
  - Through Silicon Via (TSV)
  - high precision alignment of parts before bonding

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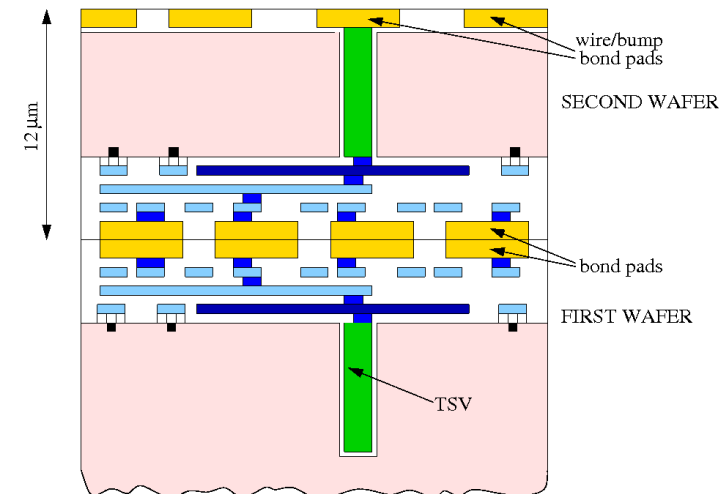
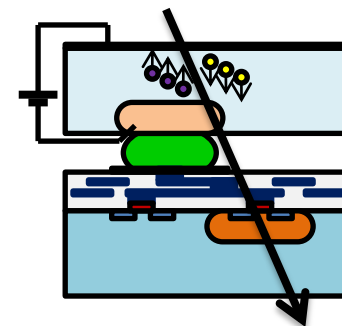# DNW MAPS and Hybrid Pixels in 3D Technology

DNW MAPS

- The deep n-well (DNW) acts as collecting element for the charge released in the substrate

- A readout chain is used for Q-V conversion
  → The gain is decoupled from C_D

- Sensor can cover a large area of the pixel cell
  → PMOS can be included in the design

- The DNW can host NMOS of the analog section
  → The additional area (as compared to standard CMOS sensors) allows the designers to implement more complex, fast readout circuits, with pixel level sparsification and time stamping techniques

- In 2D MAPS pixel electronics and detector share the same area, whereas in a 3D version very close 100% fill factor is achievable

- PMOS competitive n-wells can be placed on a separate layer from the sensor
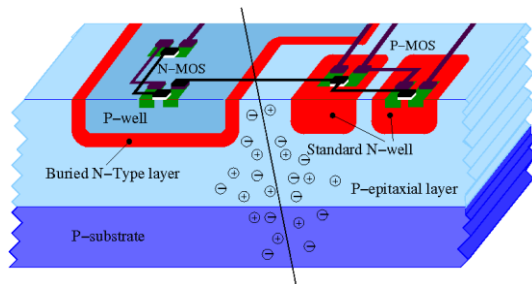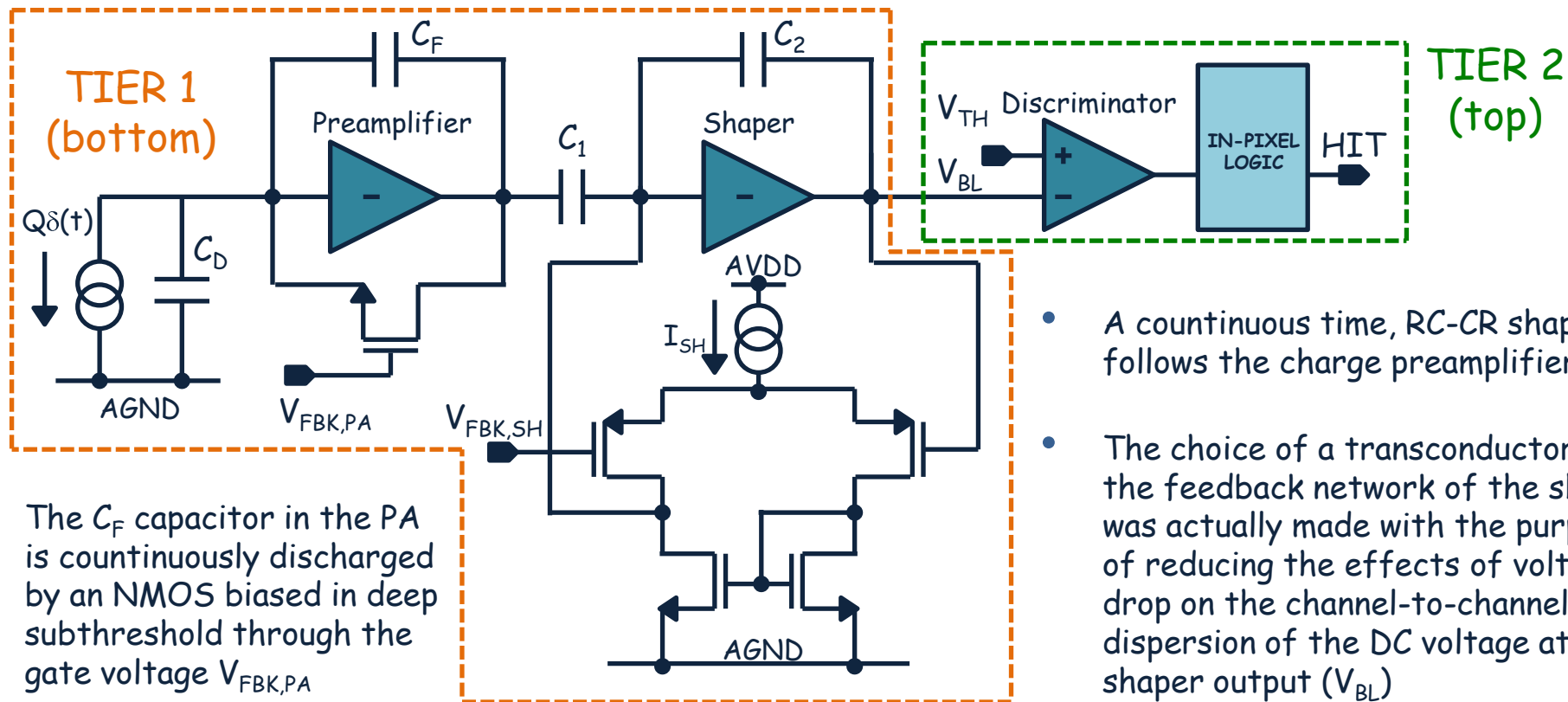

Hybrid Pixels

- Such devices are back-to-back assembled from two chips, one for the readout electronics and one for the sensor array, by means of bump bonding techniques

- Hybrid pixel detectors usually provide:
  - high signal-to-noise ratio
  - high radiation tolerance
  - 100% fill factor
  - the possibility to implement sophisticated in-pixel electronics without the problem of crosstalk between digital section and sensor

- Relatively large material budget (particle scattering)
  → fine pitch bump bonding methods and other, more innovative direct bonding techniques (Ziptronix or TMicro/ZyCube)

- In 3D design the use of two layers provides a large amount of functionality in the pixel cell

# Analog Front-end for ApselVI 3D MAPS Chip

- A countinuous time, RC-CR shaper follows the charge preamplifier

- The choice of a transconductor in the feedback network of the shaper was actually made with the purpose of reducing the effects of voltage drop on the channel-to-channel dispersion of the DC voltage at the shaper output (V_{BL})

- The C_F capacitor in the PA is countinuously discharged by an NMOS biased in deep subthreshold through the gate voltage $V_{FBK,PA}$

- The signal at the shaper output is compared to a chip-wide threshold V_{TH} by means of a discriminator

- The in-pixel logic stores the hit in a flip-flop and takes care of communicating with the peripheral blocks for fast data retrieval

- By using a transconductor, it is possible to set V_{BL} to a given (chip wide) value by means of a voltage reference placed at the periphery of the chip, which is not affected by voltage drop issues

Analog Front-end for ApselVI 3D MAPS Chip

- The final version of the MAPS detector is going to include 128x96 elements

- The pitch of the pixel cell is 50 μm

Main front-end design features	
Preamplifier Input Device [$\mu m/\mu m$]	32/0.25
Analog Power Dissipation [μW/pixel]	33
Peaking Time (Q_{inject} 800 e-) [ns]	320
Charge sensitivity @C_D = 300 fF [mV/fC]	850
ENC [e- rms]	34
Threshold dispersion [e- rms]	103
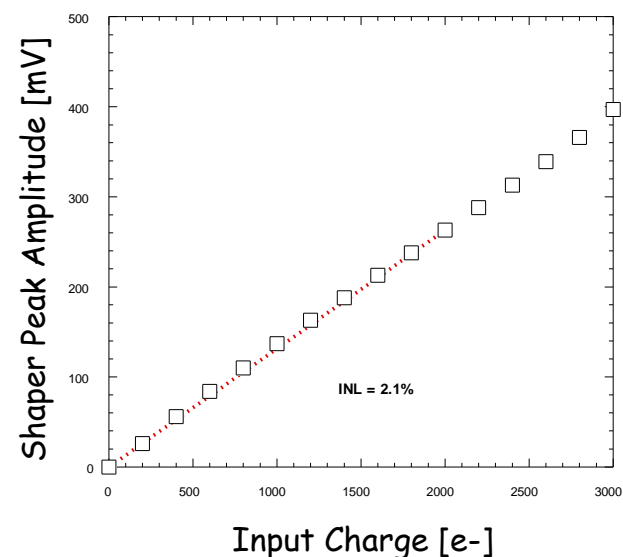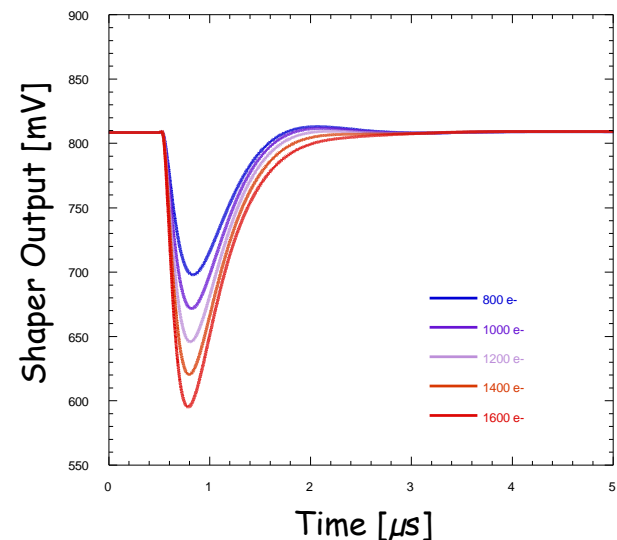
Analog Front-end for Superpix1 3D Hybrid Chip
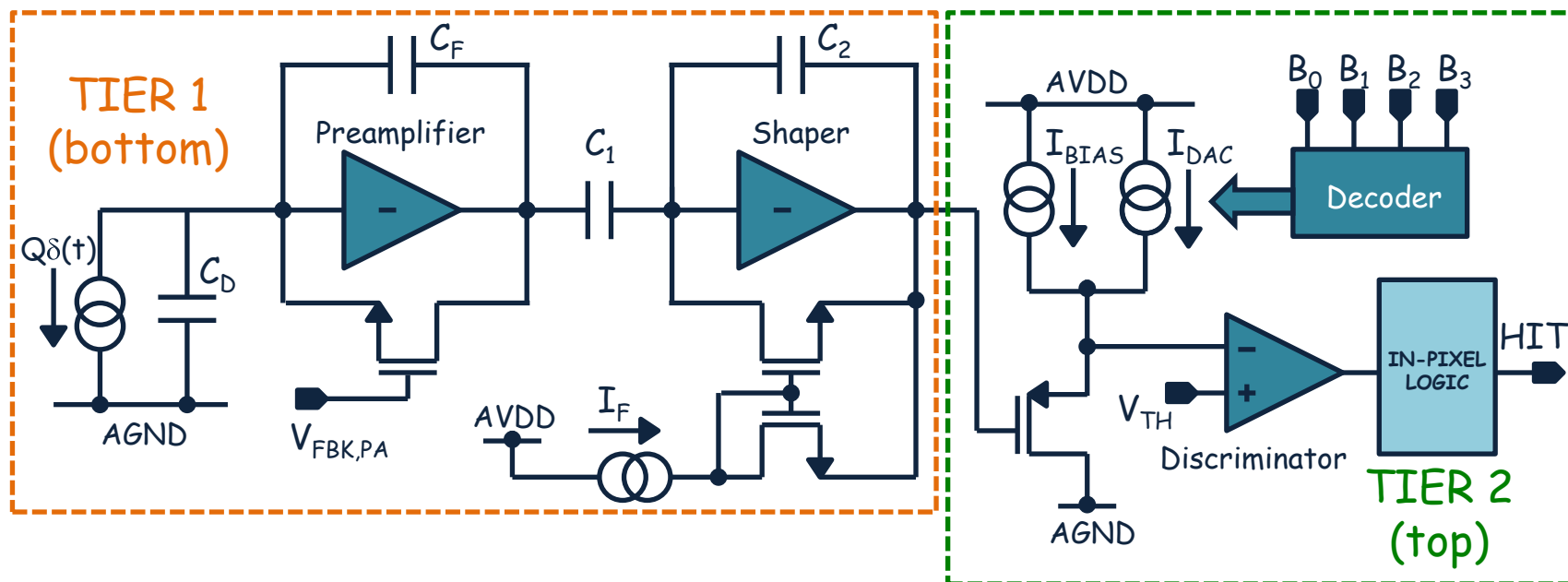
- C_2 is discharged by a constant current, proportional to the mirror reference current I_F
  → The recovery time increases linearly with the signal amplitude

- In order to limit the effects of the threshold dispersion a local fine tuning system is placed between the shaper stage and the discriminator

- The current value of the I_{DAC} source is set by a 4-bit current steering DAC in each channel

- The DAC block contains 15 unity current sources selected through a thermometric code by a decoder
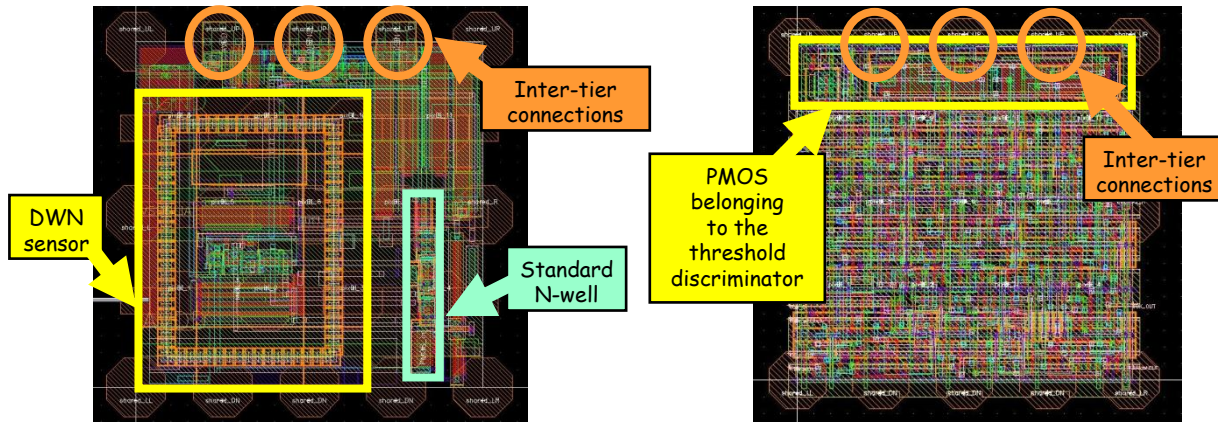
Analog Front-end for Superpix1 3D Hybrid Chip

- The chip to be submitted consists of a 32x128 matrix

- The pitch of the pixel cell is 50 μm

Main front-end design features	
Preamplifier Input Device [$\mu m/\mu m$]	18/0.25
Analog Power Dissipation [μW/pixel]	10
Peaking Time (Q_{inject} =16000 e-) [ns]	260
Charge sensitivity @C_D = 150 fF [mV/fC]	48
ENC [e- rms]	130
Threshold dispersion (before/after correction) [e- rms]	560/65

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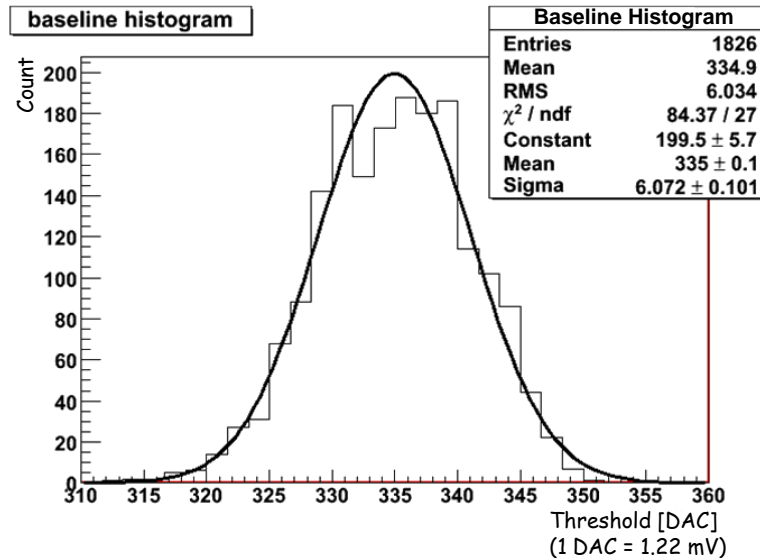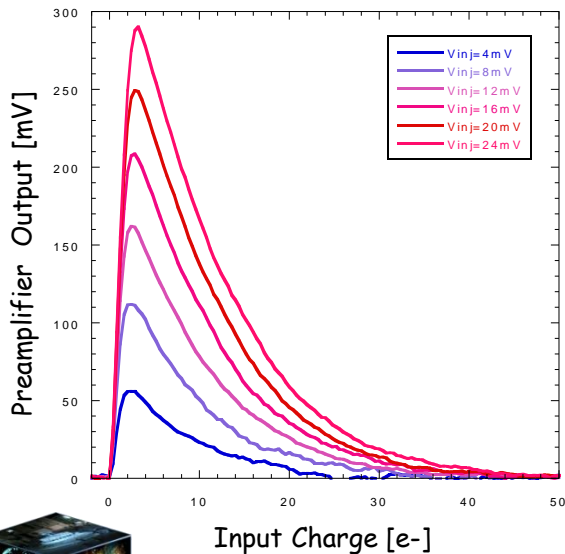Università degli Studi di Pavia
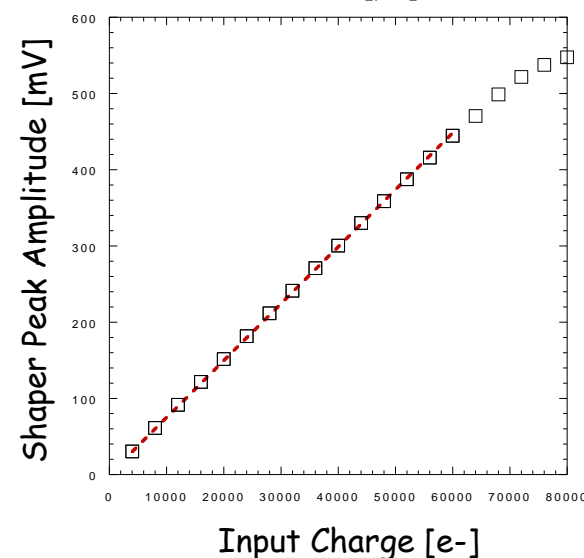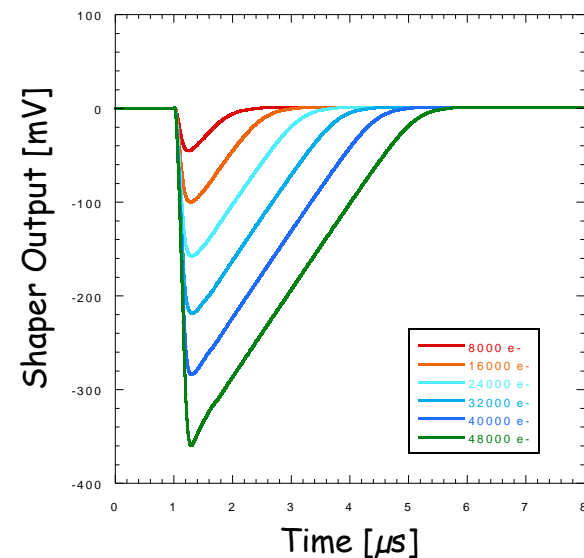
Characterization of SDR1

- SDR1 (Sparsified Digital Readout) chip represents the first generation of 3D MAPS with advanced readout architecture for high data rate

- This prototype was especially designed for vertexing applications to the International Linear Collider (ILC) facility

- This is a shaperless version of MAPS front-end with a pixel pitch of 20 μm

Inter-tier connections

DWN sensor

Standard N-well

PMOS belonging to the threshold discriminator

Inter-tier connections

Statistical distribution of the PA Baseline

baseline histogram	Baseline Histogram	
	Entries	1826
	Mean	334.9
	RMS	6.034
	χ^2 / ndf	84.37 / 27
	Constant	199.5 ± 5.7
	Mean	335 ± 0.1
	Sigma	6.072 ± 0.101

Threshold [DAC]
(1 DAC = 1.22 mV)

Preamplifier Output [mV] vs Input Charge [e-]

Vinj=4mV
Vinj=8mV
Vinj=12mV
Vinj=16mV
Vinj=20mV
Vinj=24mV

Noise and Gain Result	CHIP 2	CHIP 3
ENC [e-]	76	77
Charge Sensitivity [mV/fC]	560	535

Threshold Scan Result	CHIP 1	CHIP 3
Threshold [mV]	410	409
Threshold Dispersion [e-]	47	58

Conclusions and plans for the future

- Two different analog processors for hybrid pixels (SuperPIX1) and monolithic sensors (ApselVI) have been designed in view of applications to the SVT Layer0 of the SuperB Factory

- They will be fabricated in a vertical integration, 130 nm CMOS technology, whose properties have been exploited to increase the functional density of the mixed-signal front-end and to improve the immunity of the analog section (and of the sensor in MAPS devices) from digital signals

- From the standpoint of MAPS design, use of a 3D process may help improve the collection efficiency when a large DNW collecting electrode is adopted

- The results of the SDR1 characterization are only preliminary and we are waiting for the 3D structure

- Characterization of the SDR1 prototypes will require measuring the sensor detection efficiency through tests with infrared laser