Front-End Analog Cell for Hybrid Pixel Sensors and First Measurements on Apsel5T chip

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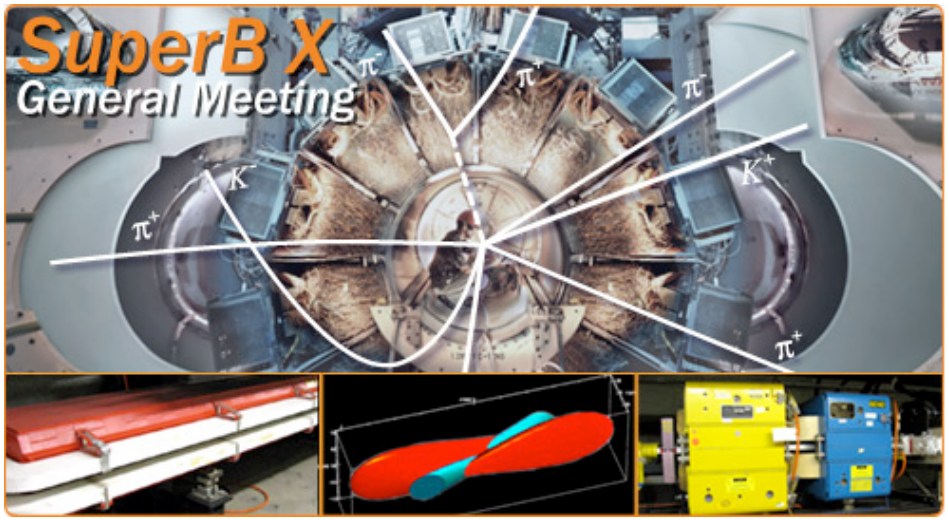

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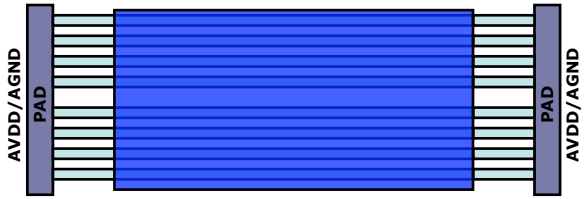
and INFN Pavia

SVT layer0 options for SuperB

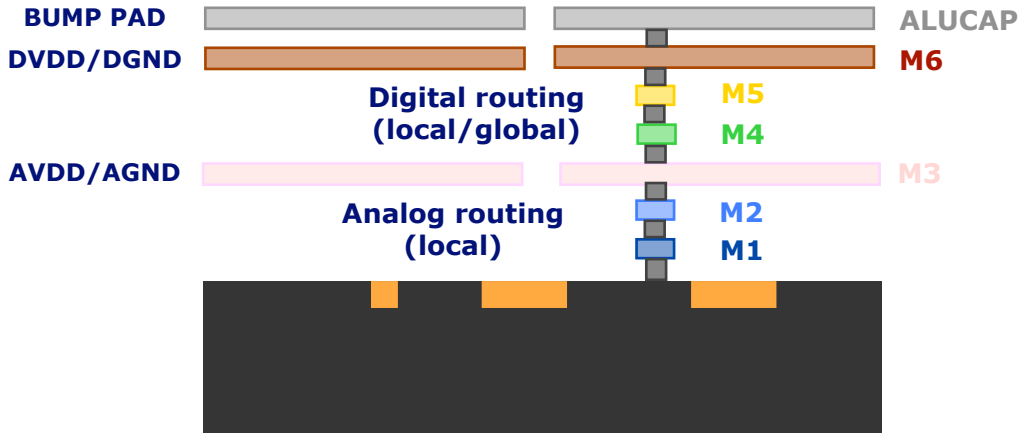
- **Design of the SVT layer0 at SuperB has to comply with severe requirements**
  - large background, >5 MHz, small thickness, <1% X_0
- **Striplets**
- **Hybrid pixel detectors**
  - presently the baseline solution for the TDR
  - a 130 nm CMOS front-end chip (32x128) submitted in September
  - fine pitch (50 μm) bump bonding (IZM, Munich) with a 200 μm thick pixel detector (FBK-irst, Trento)
- **Deep N-well CMOS monolithic sensors (DNW-MAPS)**
  - extensive R&D ongoing in a 130 nm CMOS process, Apsel4D1 and small matrices tested on the PS beam at CERN in July 2009 (see talk by S. Bettarini)
  - characterization of last prototype Apsel5T is ongoing
- **Vertically integrated DNW CMOS monolithic sensors**
  - Apsel-like prototype designed and submitted for fabrication in a 3D process

Analog cell for hybrid pixel sensors: specifications & constraints

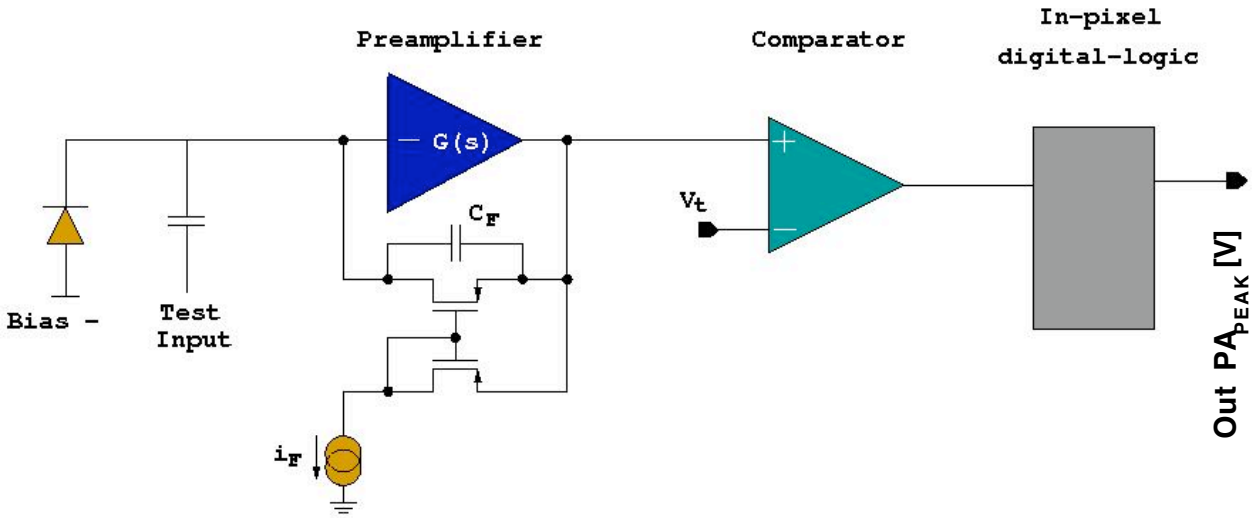
- Analog current ≈ 2uA/pixel => minimize AVDD drop
Analog power ≈ 0.1W/cm^2
Power consumption for digital section dominates ~ 1W/cm2

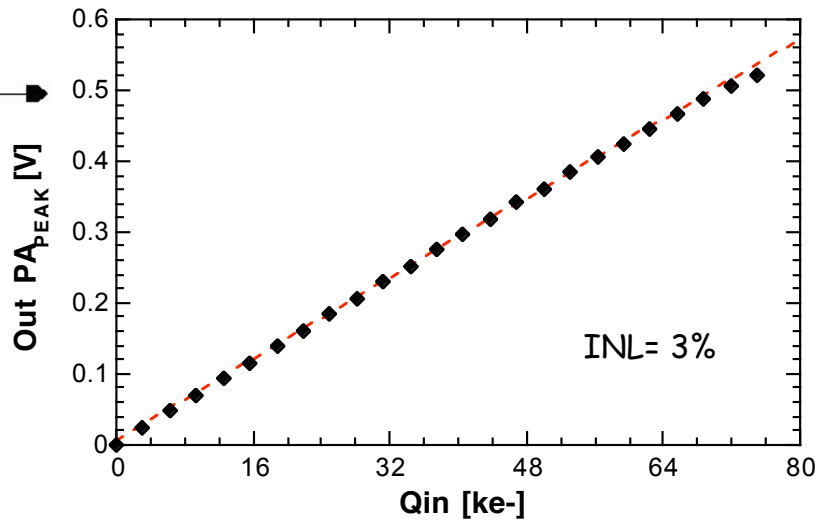


- Pixel capacitance ≈ 100fF
- I_{leak} ≈ 200fA
- Shaping time ≈ 100ns (return to baseline < 3us => minimize dead time during which the cell is blind)
- Charge/pixel (MPV) ≈ 16000-4000 e-/pixel
- S/N ≈ 25 for minimal charge (S=4000e- => ENC≈160e-)
- Analog channel + in-pixel digital-logic + structures for testing FE chip w/o sensors in 50x50um^2
- STM 130nm CMOS technology
- 6+1 metal layers
- No MIM CAPs allowed



Analog cell for Hybrid Pixel Sensors: Main design features and simulations

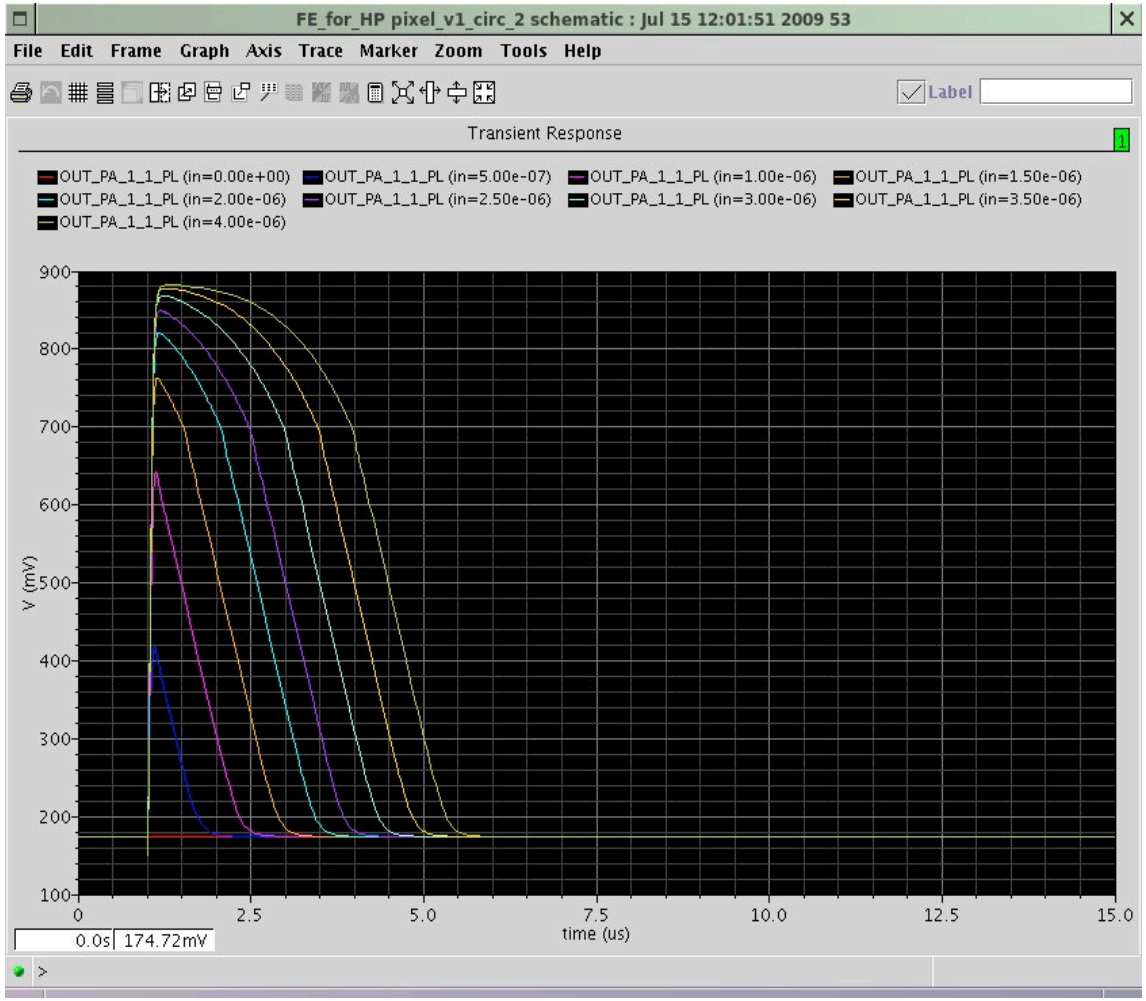




- I_{AVDD} ≈ 2.1 uA, power dissipated ≈ 2.5uW/ch
- Charge sensitivity ≈ 50mV/fC
- Fast peaking time ≈ 100ns
- ENC=150e- @ C_D=100fF (170e- @ C_D=150fF, 200e- @ C_D=200fF)
- Threshold dispersion ≈ 350e- (190e- from the PA, 290e- from the discriminator)
- The recovery time increases linearly with the signal amplitude
- Cinj for external calibration (no internal pulser) included
- High frequency noise contribution has been reduced limiting the PA bandwidth

Return to the baseline of the analog output

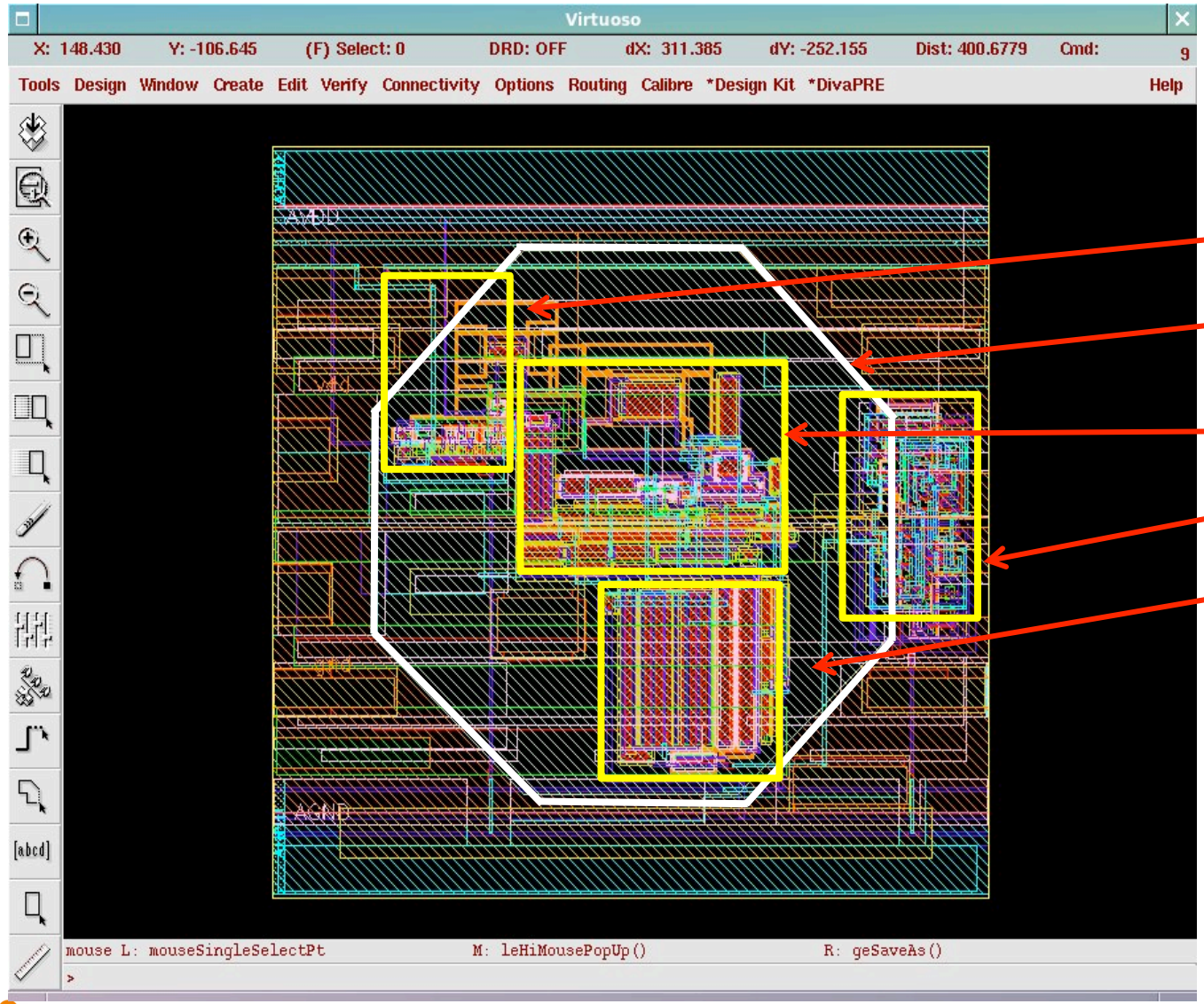
Fast return to the baseline to minimize the dead time of the pixel



Qin [ke-]	ΔT [us]
30	≈ 1
60	1.4
80	1.7
90	≈ 2
120	2.4
150	2.8
180	3.2
200	3.6

Simulated with reference V_{feed} integrated in the cell

Cell layout



Kill inject mask + Cinj

Bump bond pad

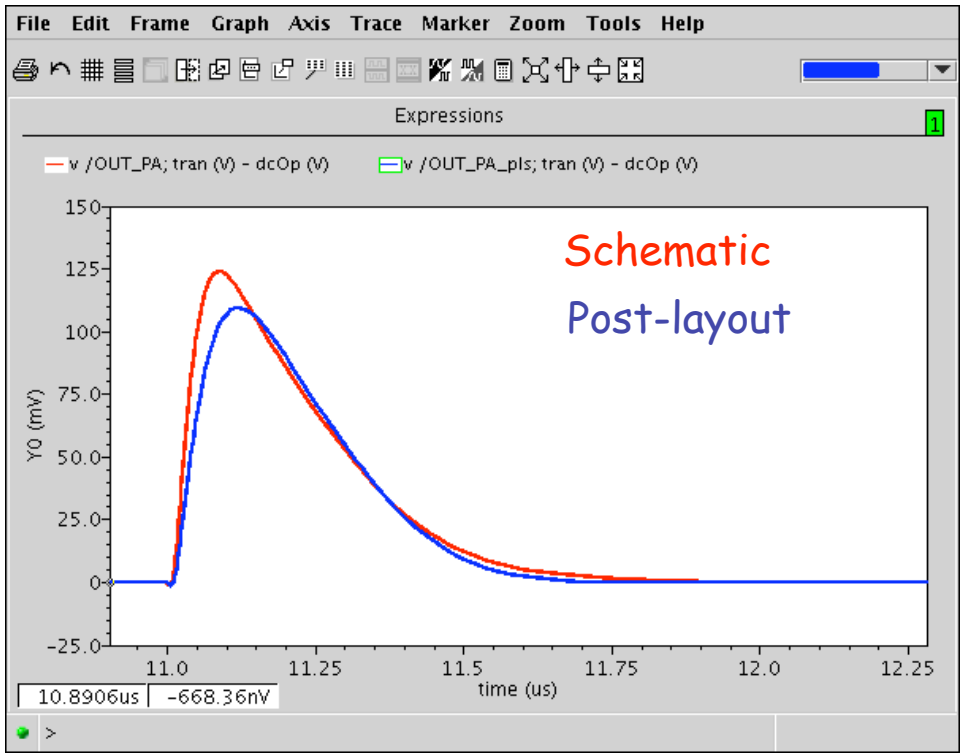
PA

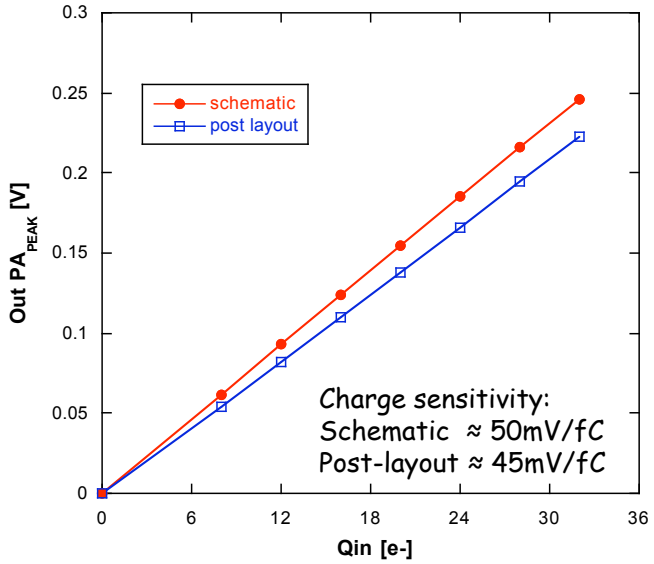
In-pixel logic

Comparator

Room for local fine-adjusting circuits of the comparator threshold is available (implementation in the next prototype is possible)

Post-layout simulations





C_D [fF]	ENC [e- rms] Schematic simulations	ENC [e- rms] Post-layout simulations
100	150	170
150	170	200
200	200	220

Parasitic capacitance extraction

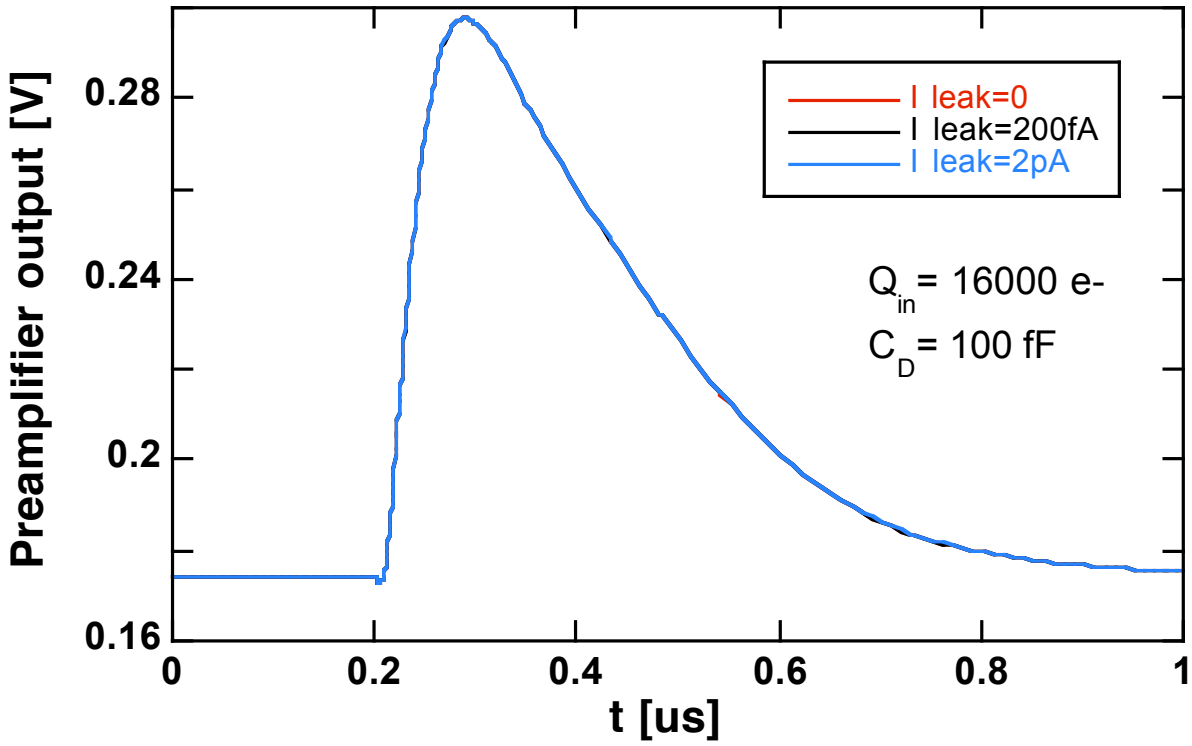
Digital signals toward IN	Parasitic cap. [aF] StarRCXT	Parasitic cap. [aF] Raphael
$LATCH\_ENA_d$	89.6	12
$INJ\_MASK\_OUT<7>_d$	52.2	40
PIX_DATA_d	14.4	-
$LN\_FAST\_OR_d$	14	-
$INJ\_MASK\_OUT<0>_p$	40	52

Leakage current effects

Leakage current foreseen ≈ 200fA

Baseline offset @ 2pA ≈ 0.02mV

Noise increase @ 2pA ≈ 2-3 e-



Performance wrt temperature

Temperature [°C]	ENC [e-] @ C_D=100fF	Charge sensitivity [mV/fC]	Baseline PA [mV]	Analog power [μW]
27	150	48	174.3	2.55
40	165	47.3	158.6	2.94
50	178	47	146.4	3.22

- The threshold voltage falls with increasing temperature. The slope is usually in the range of -0.5mV/°C to -4mV/°C.

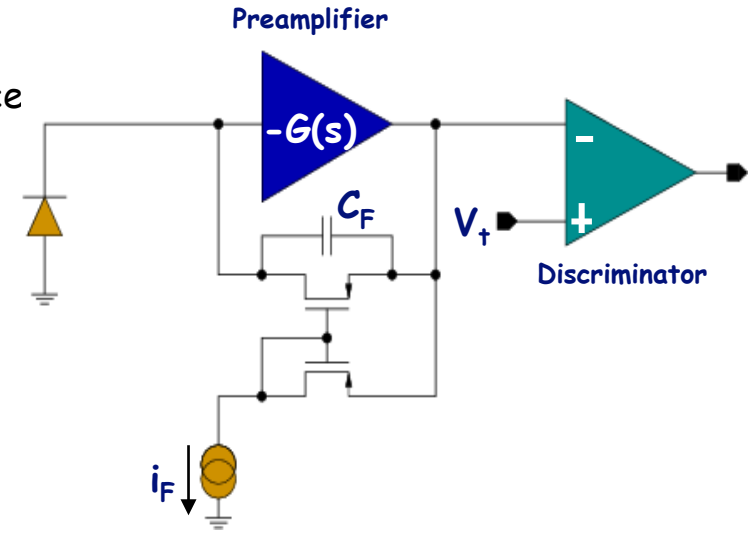
Apsel5T

Motivations

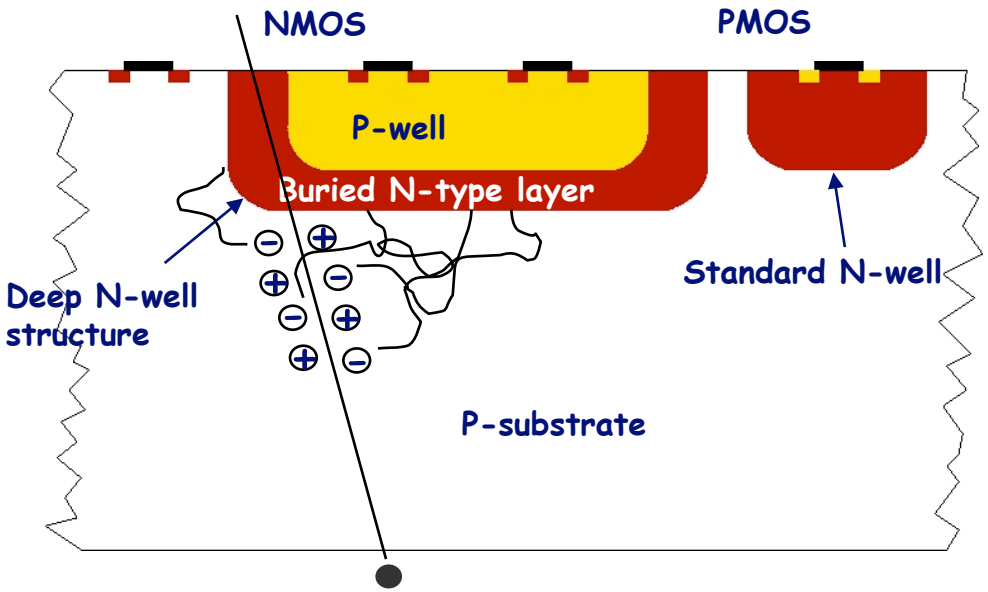
- Scaling to larger matrix size (128x128 or 320x80) dictates to remove the shaper stage to make room for additional macropixel private lines
- Shaper less front-end makes it possible to reduce the pixel pitch (from 50x50um^2 to 40x40um^2)
- Optimized cell with satellite N-wells surrounding PMOS competitive N-wells in APSEL5T ⇒ Efficiency ~ 99% (from TCAD simulations). Beam test results of APSEL4D show a ~90% efficiency, which agrees very well with TCAD simulations
- Metal shielding between analog and digital voltages improved and made compatible with a large matrix

Main design features

- Charge sensitivity (PLS): 750mV/fC. Very small feedback capacitance Single stage (considering the analog buffer 680mV/fC)
- Equivalent noise charge (ENC) (PLS): 28e$^-$ (sensor 1), 31e$^-$ (sensor 2)
- Threshold dispersion 24e$^-$ (with a charge sensitivity of 750mV/fC)
- t_P≈ from 410ns @ Q_{in}=200e$^-$ to 620ns @ Q_{in}=2400e-
- Analog power: 21uW/ch ≈ 1.3W/cm^2
- M3 and M4 for power distribution and digital activity shielding



Deep N-Well CMOS MAPS



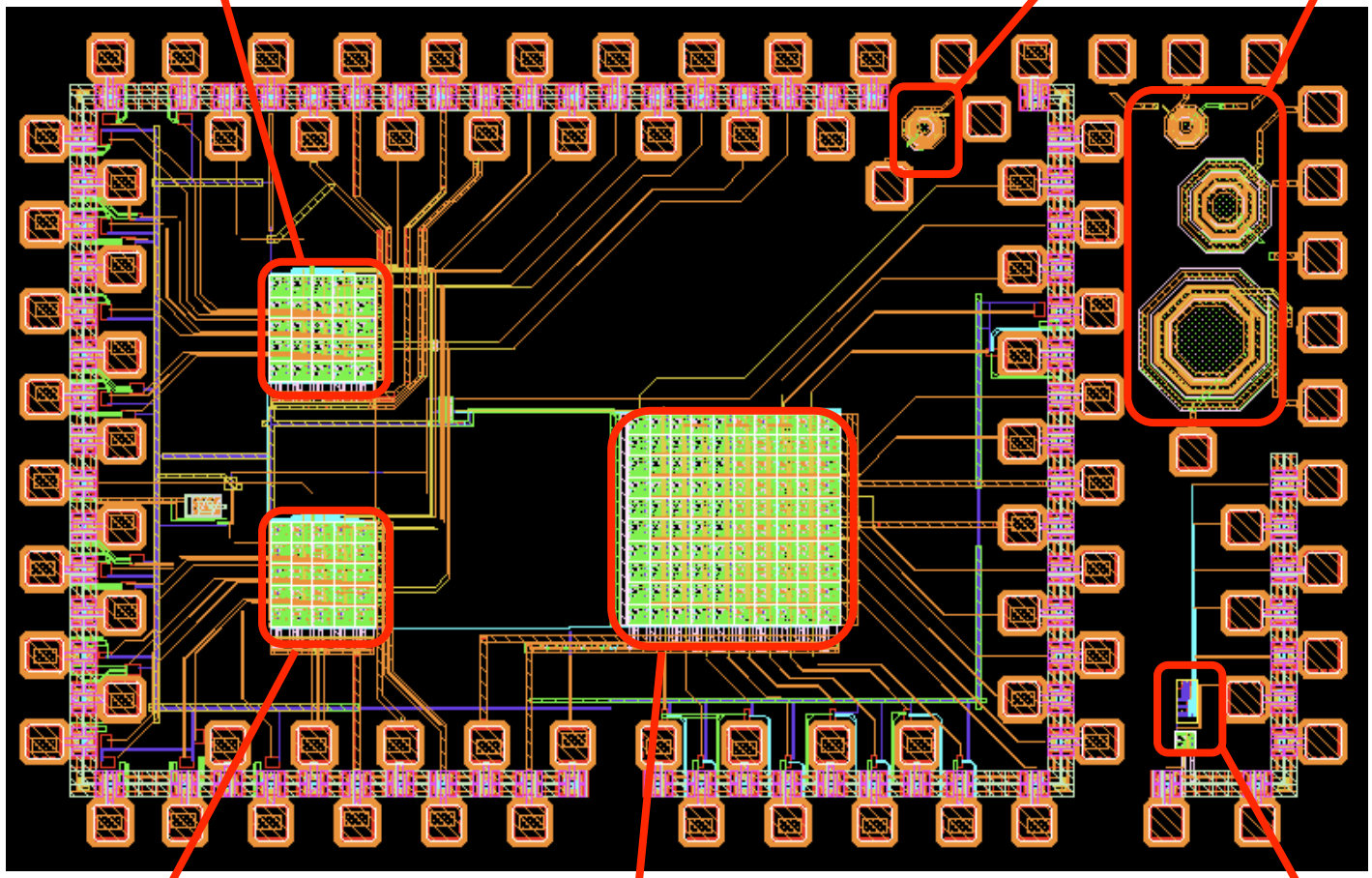
- In triple-well CMOS processes a deep N-well is used to shield N-channel devices from substrate noise in mixed-signal circuits
- DNW MAPS is based on the same working principle as standard MAPS

- Classical optimum signal processing chain for capacitive detector can be implemented at pixel level
- The collecting electrode (DNW) can be exploited to obtain higher single pixel collected charge
- A charge preamplifier is used for Q-V conversion → gain decoupled from electrode capacitance
- DNW may house NMOS transistors and using a large detector area, PMOS devices may be included in the front-end design → charge collection efficiency depends on the ratio between the DNW area and the area of all the N-wells (deep and standard)

Apsel5T

M1: 3x3 matrix with all the analog outputs available, injection capacitance for the central pixel, sensor layout version 1.

4 NW-P-int. NW-pepi diode for radiation hardness tests. 3 different geometries implemented.



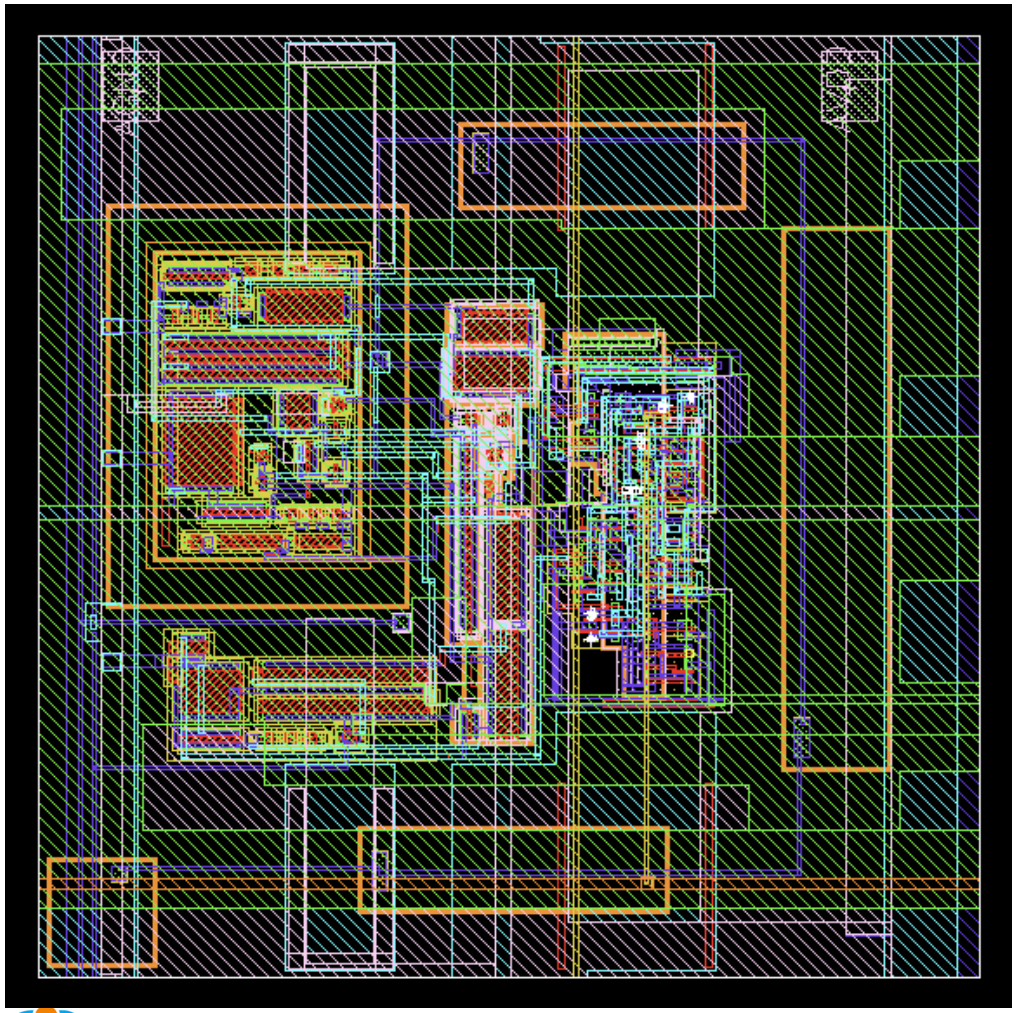
M1: 3x3 matrix with all the analog outputs available, injection capacitance for the central pixel, sensor layout version 2.

M3: 8x8 matrix with a row-by-row sequential readout. Injection capacitance and analog output available on pixel 17.Sensor layout version 1 in the left 8x4 matrix and version 2 in the right 8x4 matrix.

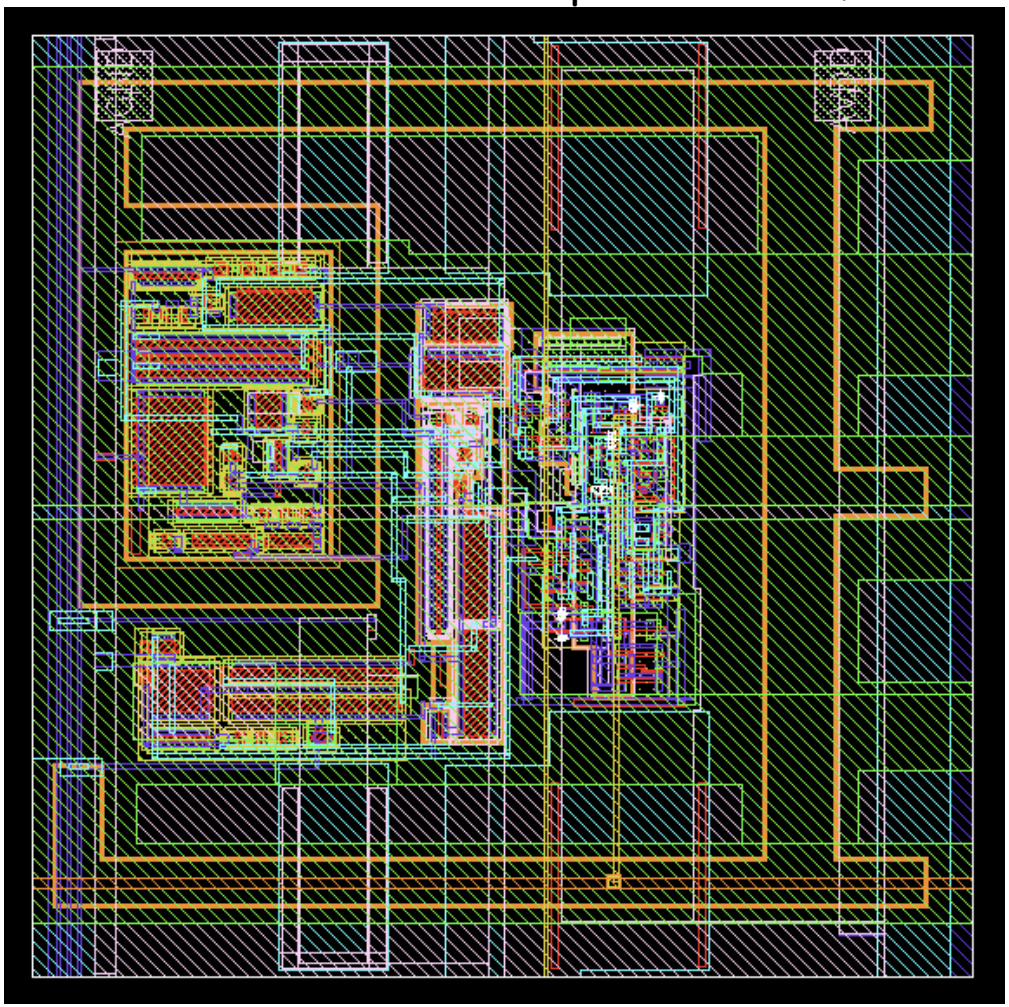
5 bit DAC

Pixel layout

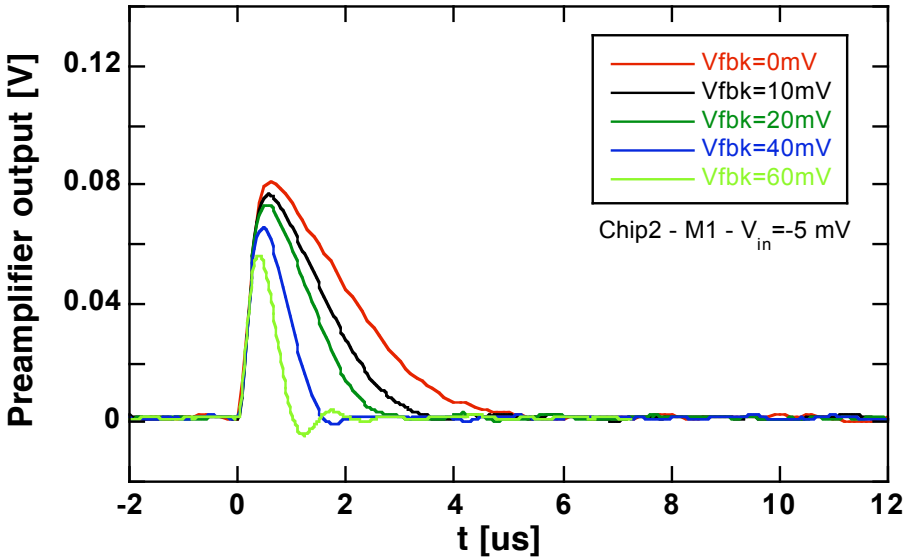
Area sensore: 410um2
Area NW-PMOS: 70um2
Fill Factor: 0.85
Cap. sensore ≈ 220fF

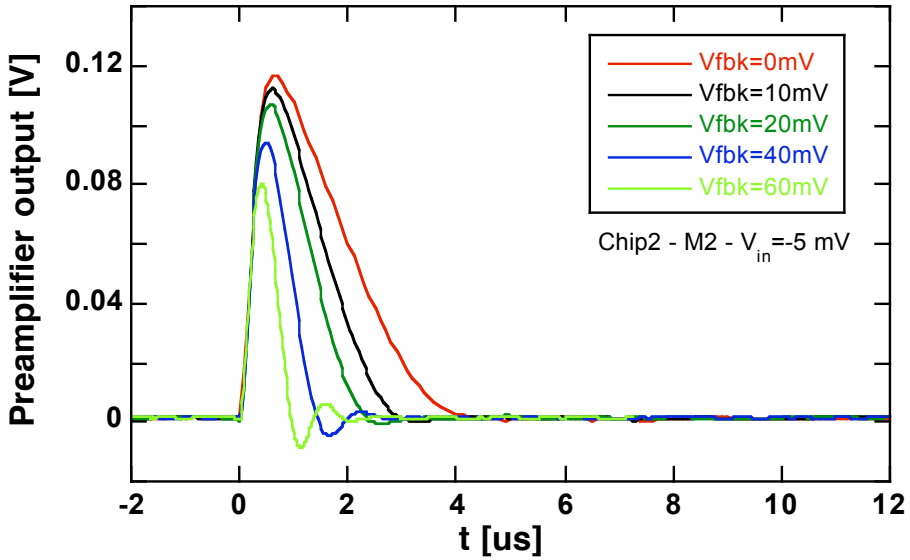


Area sensore: 480um^2
Area NW-PMOS: 70um^2
Fill Factor: 0.87
Cap. sensore ≈ 270fF



Vout vs Vfbk, Noise and Charge Sens. Measurements





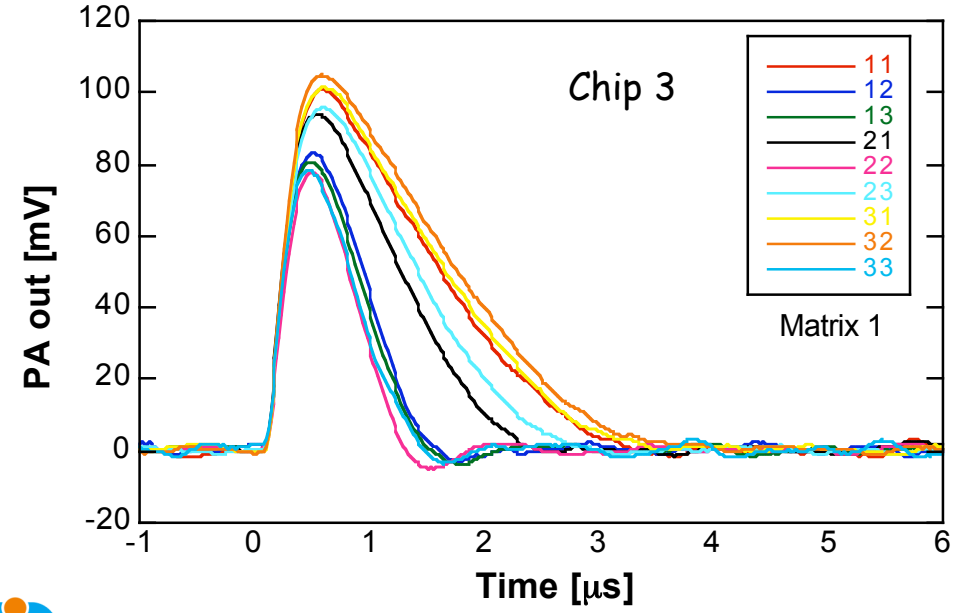
Pixel	Chip 2 – ENC [e-]	Chip 3 - ENC [e-]
22 M1	99	45
22 M2	55	53
17 M3	60	53

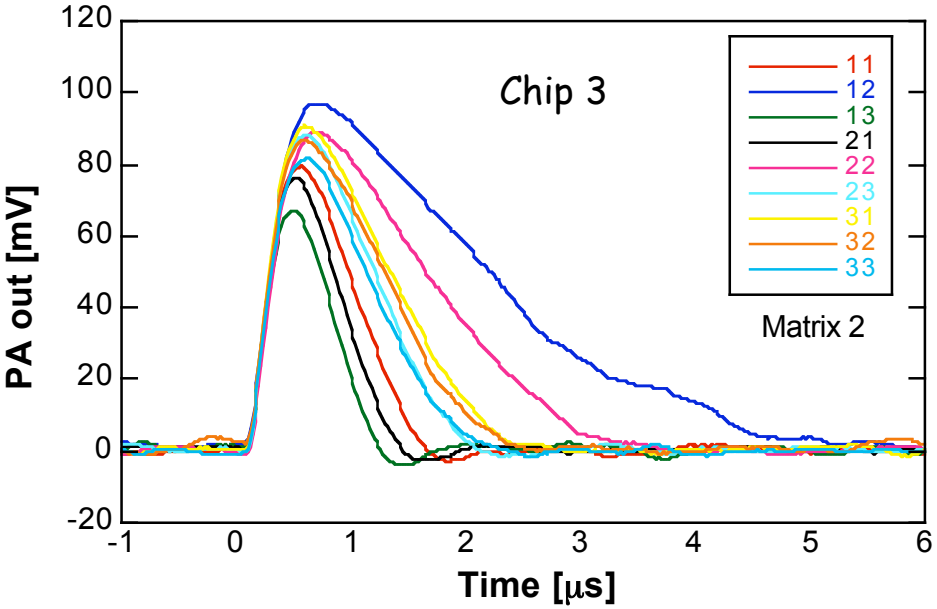
Pixel – chip2	Charge sens. [mV/fC]
22 M1	755
22 M2	820
17 M3	585

Pixel - chip3	Charge sens. [mV/fC]
22 M1	540
22 M2	790
17 M3	605

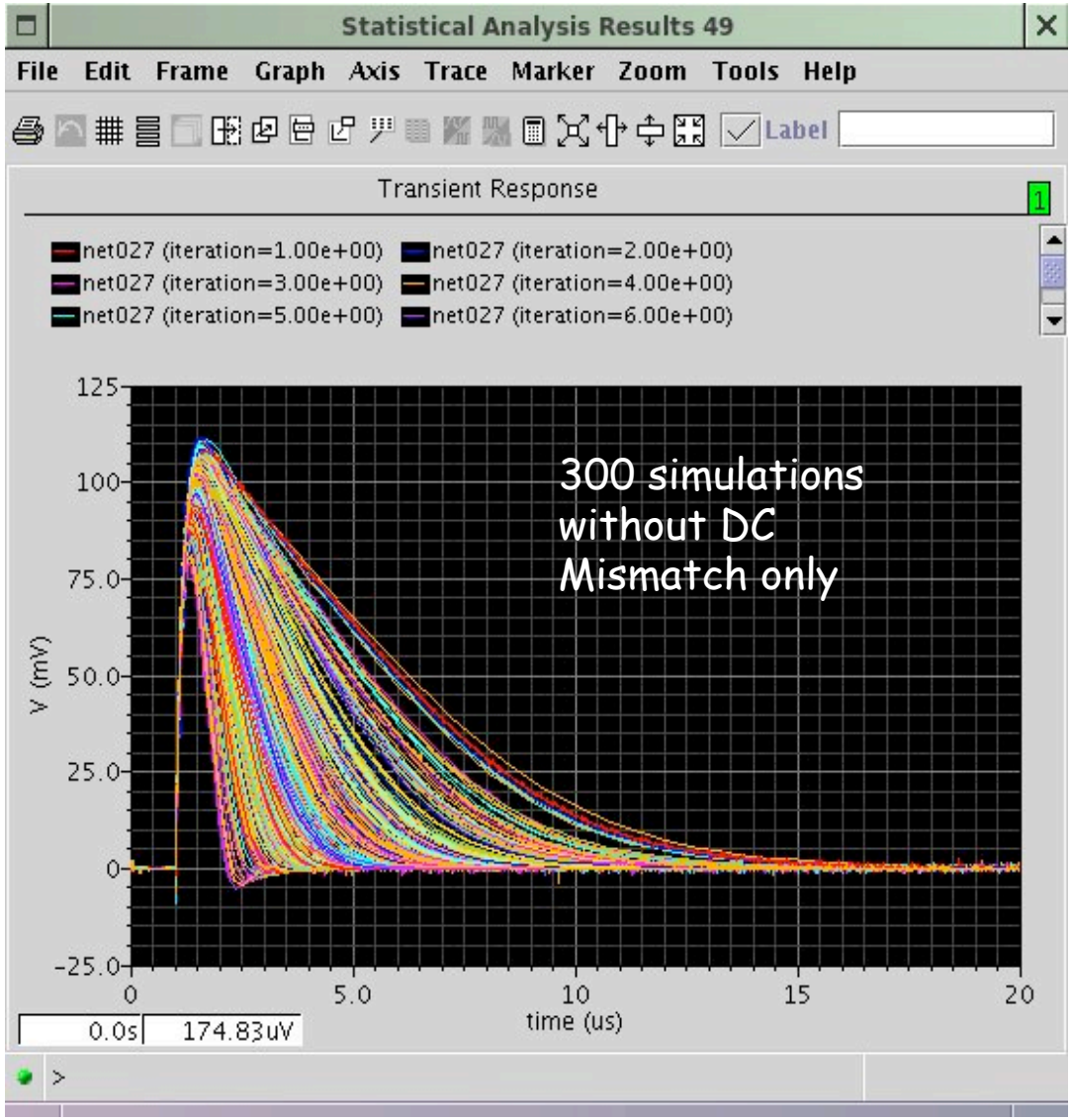
Laser measurements

- Response of the preamplifier outputs of the 3x3 matrices (the position of the laser is such to obtain the maximum amplitude)
- As shown in the previous slide there is a wide variation in the peak amplitude and in the return-to-baseline time
- Variations of the process parameters of the feedback network transistors could explain this effect





Monte Carlo simulations



Apsel5T submitted

M26, W/L=0.15/0.4

M27, W/L=8/0.18

feedback transistors

Peak value

Mean: 98mV

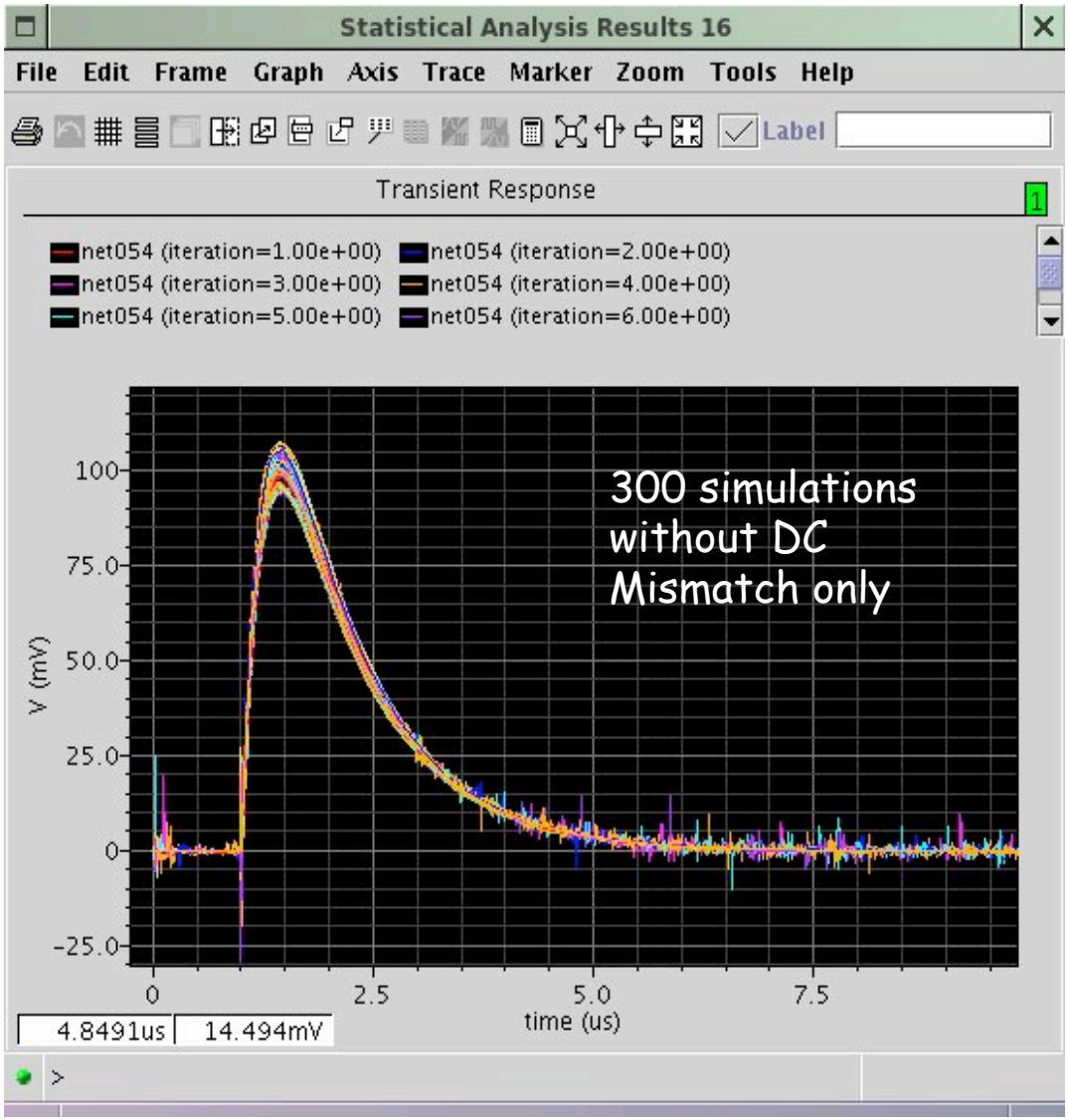
Std dev: 6.4mV

Width @ 25mV

Mean: 2.77us

Std dev: 1.43us

Monte Carlo simulations



Ideal resistor in feedback

Output maximum value

Mean: 97mV

Std dev: 2mV

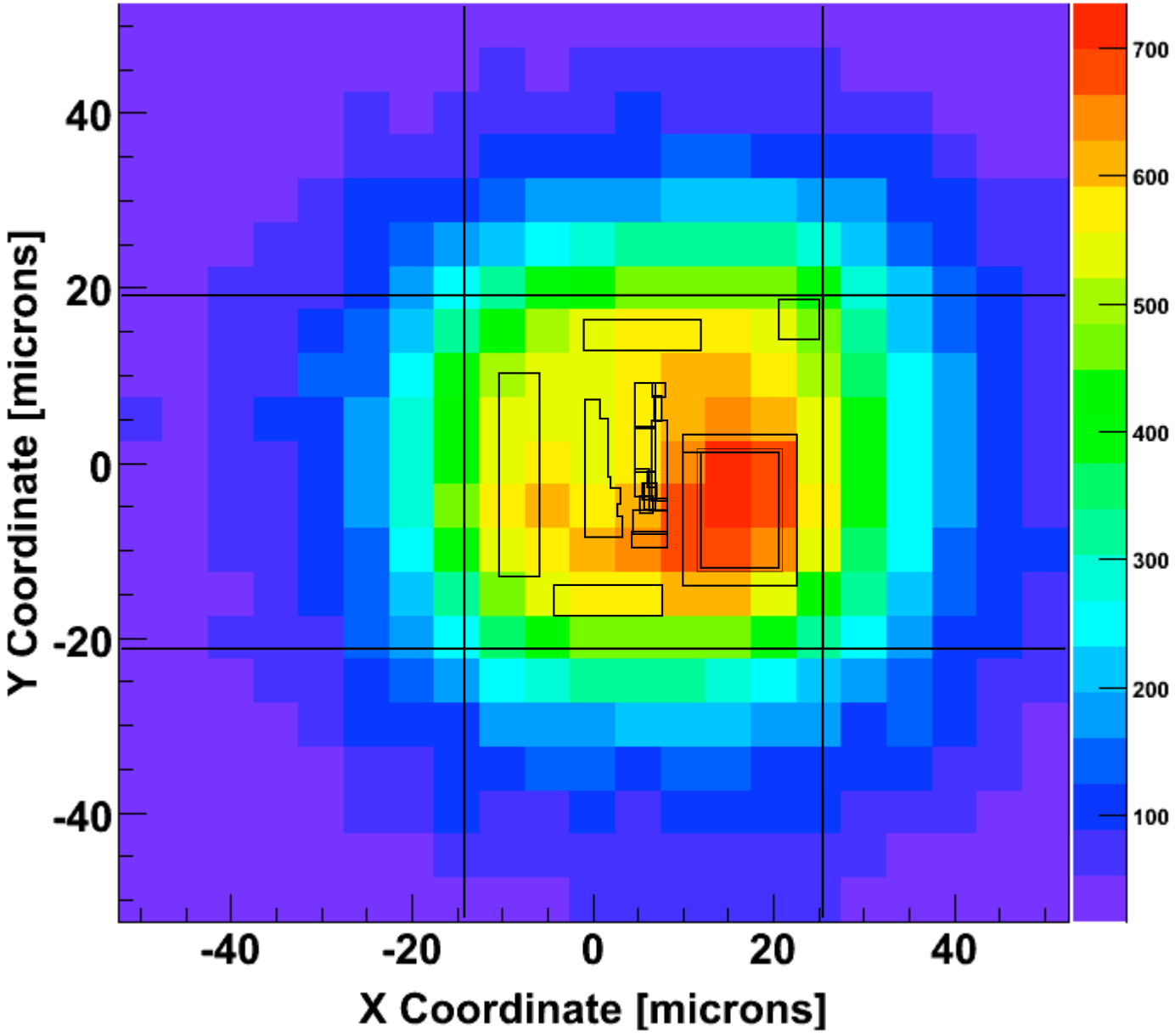
Width @ 25mV

Mean: 2.28us

Std dev: 0.05us

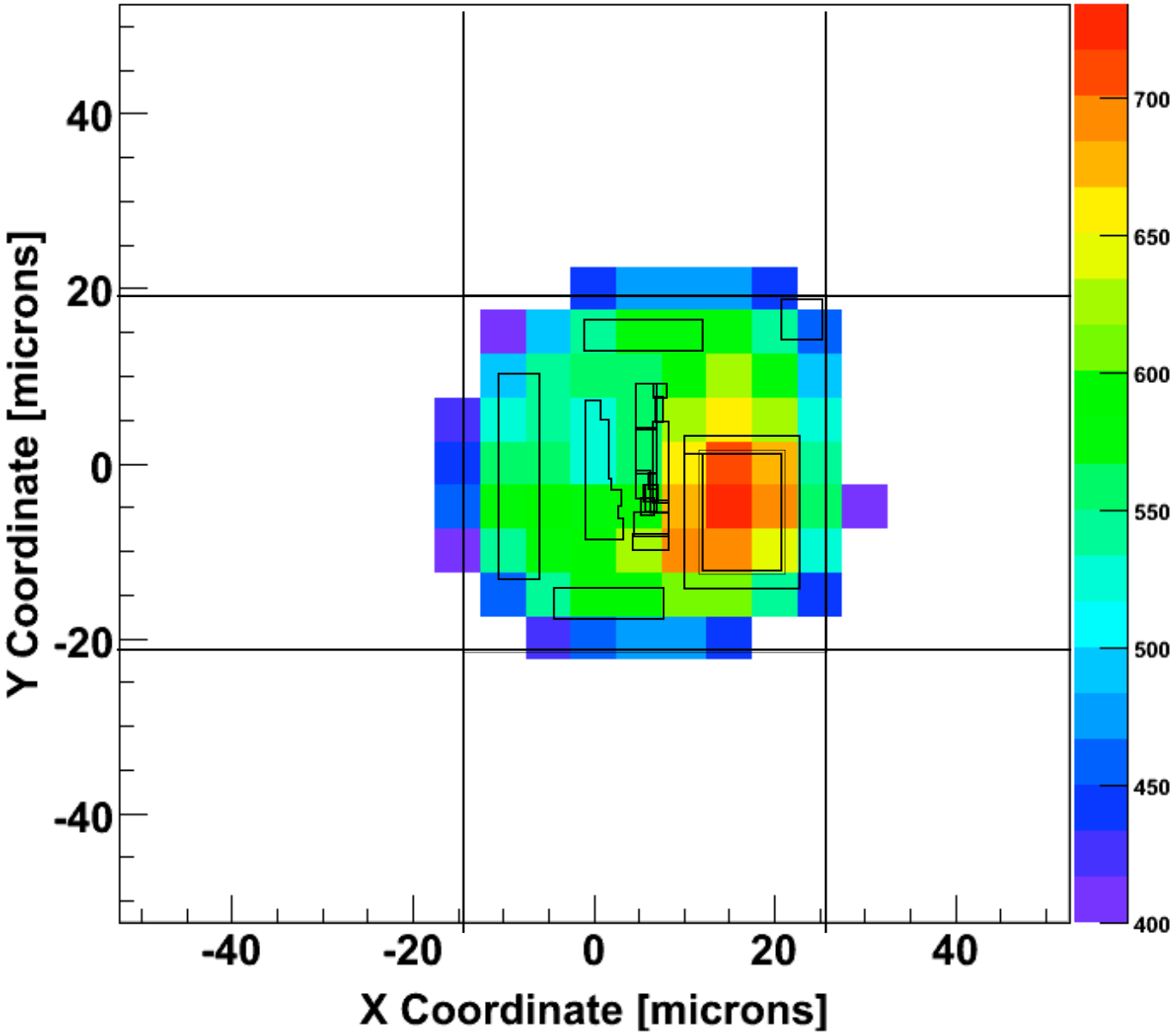
Laser scan: Matrix M1

- Charge collected by the central pixel of M1 matrix as a function of the laser position
- 5um step in X and Y
- The layout of the n-well layers and the dimension of the pixel pitch has been superimposed (exact position unknown)
- σ_{xy} of the laser ≈ 20um
- The amount of charge that is deposited has not been calibrated
- The main purpose of this measurement is to show the relative charge collection versus position



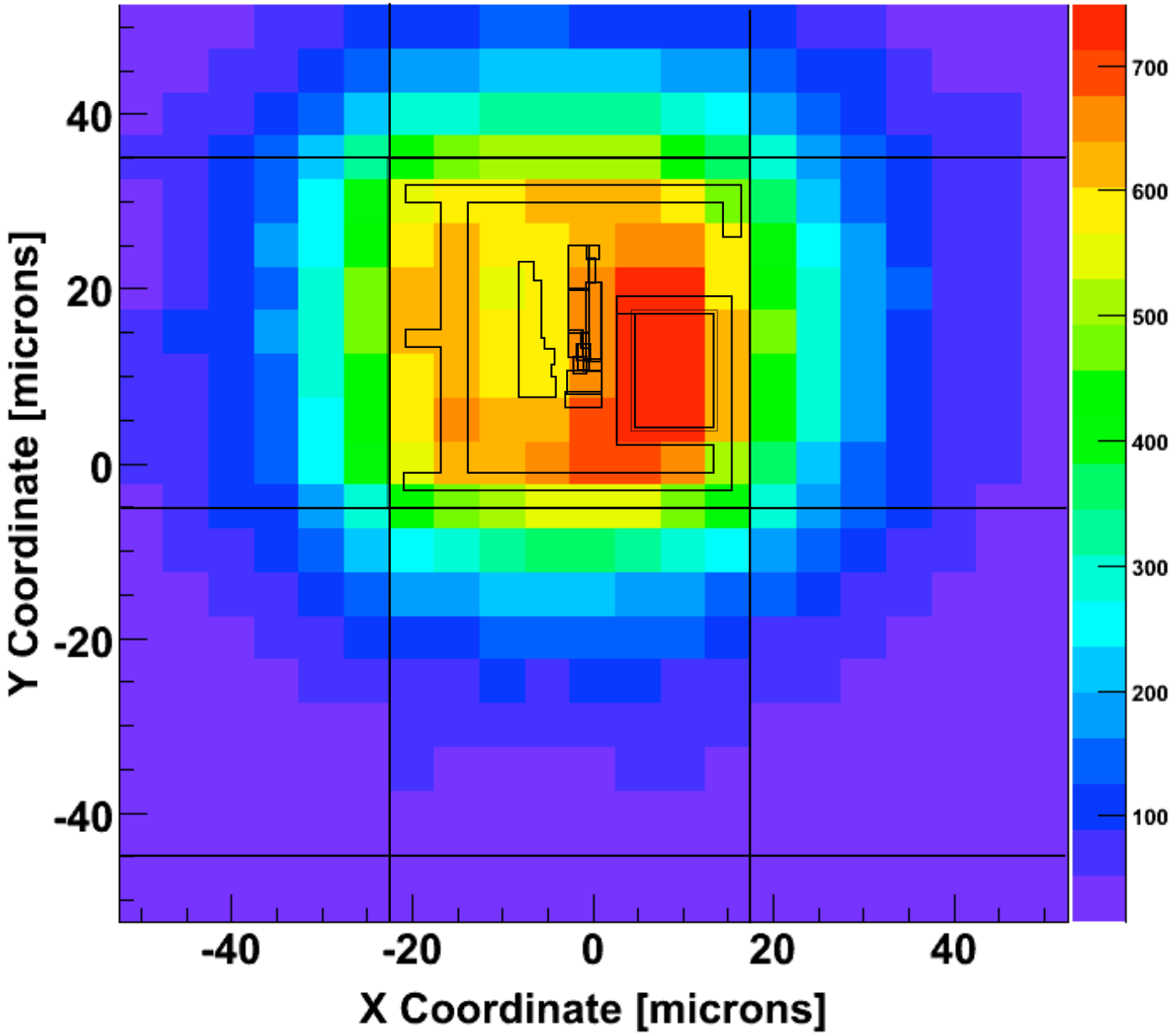
Laser scan: Matrix M1

- Same plot but with color palette between 800e- and 400e-
- Small reduction of the collected charge in the central region of the competitive n-wells
- White color for charge collected below 400e-



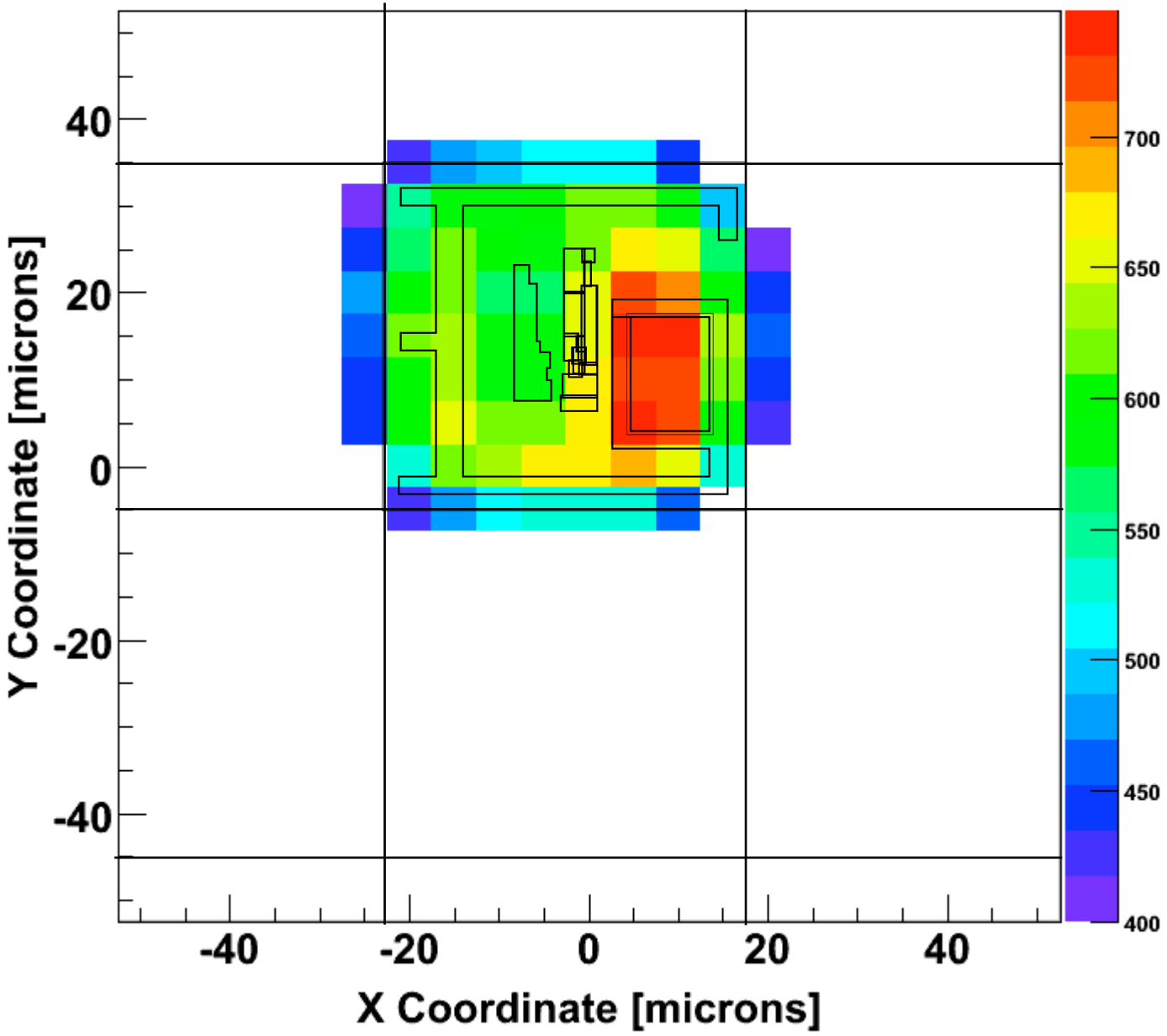
Laser scan: Matrix M2

- Charge collected by the central pixel of M2 matrix as a function of the laser position
- Yellow and red zone with square shape: larger than M1
- More than 500e- collected over about 40x40um2



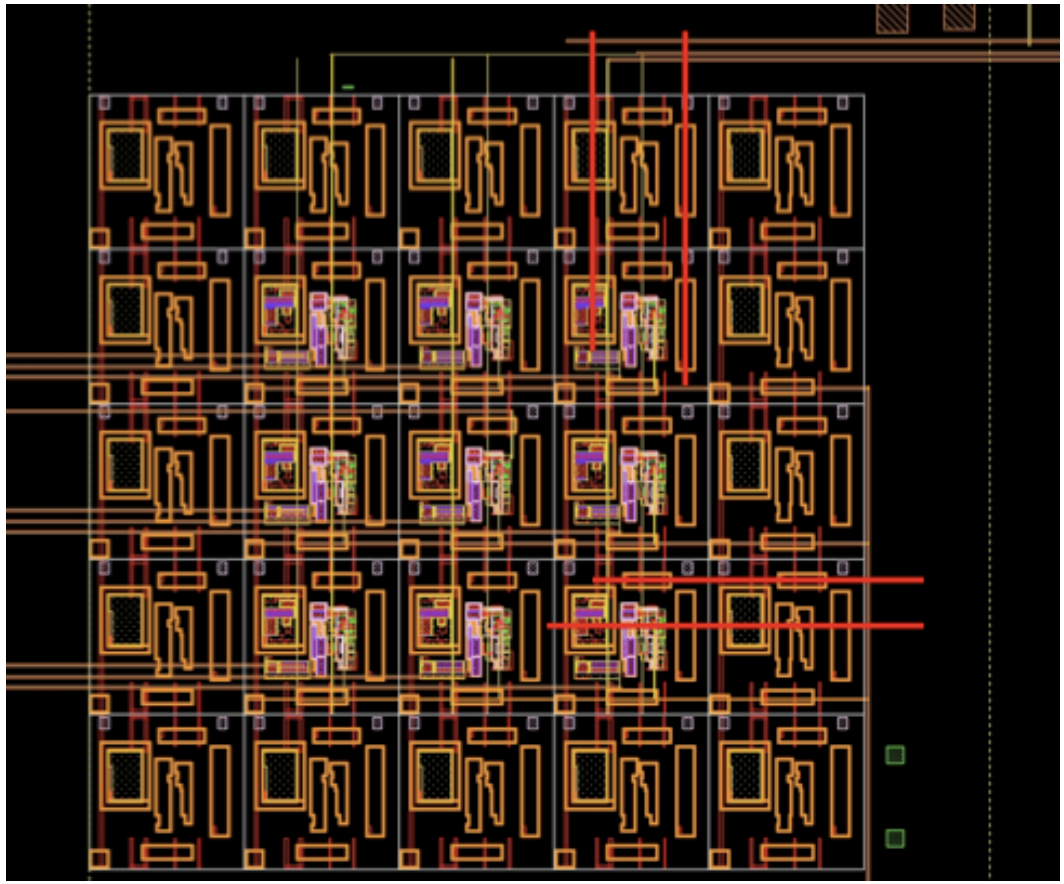
Laser scan: Matrix 2

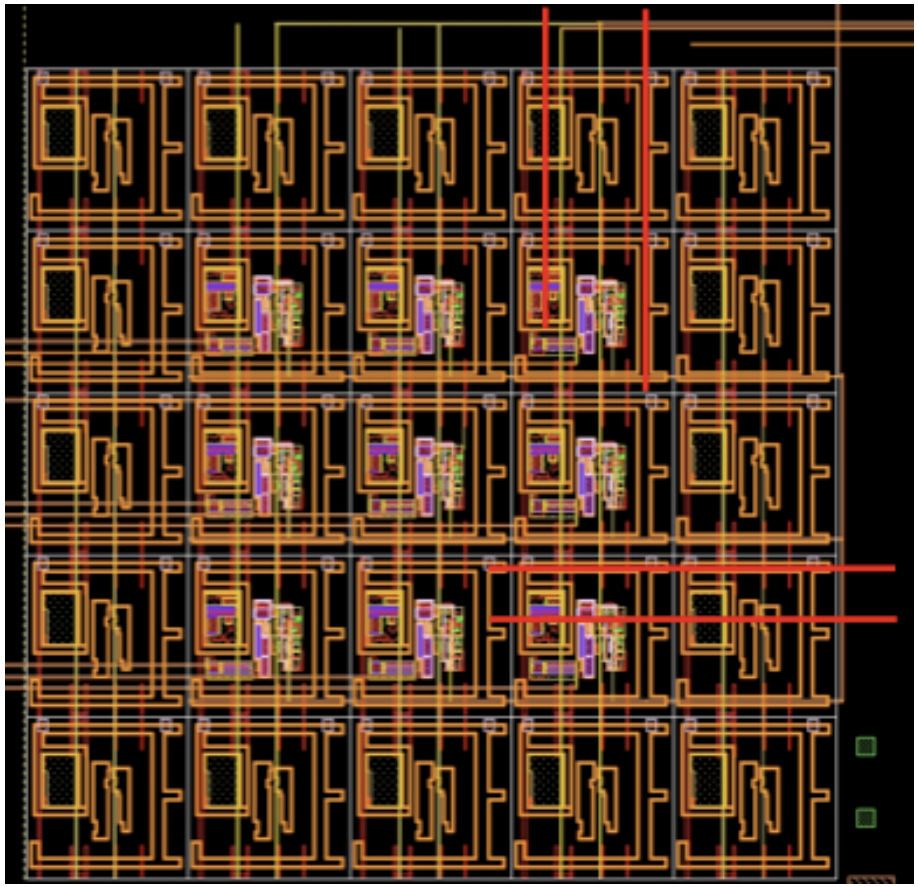
- Same plot but with color palette between 800e- and 400e-
- Yellow and red zone with square shape: larger than M1
- More than 500e- collected over about 40x40um2
- White color for charge collected below 400e-



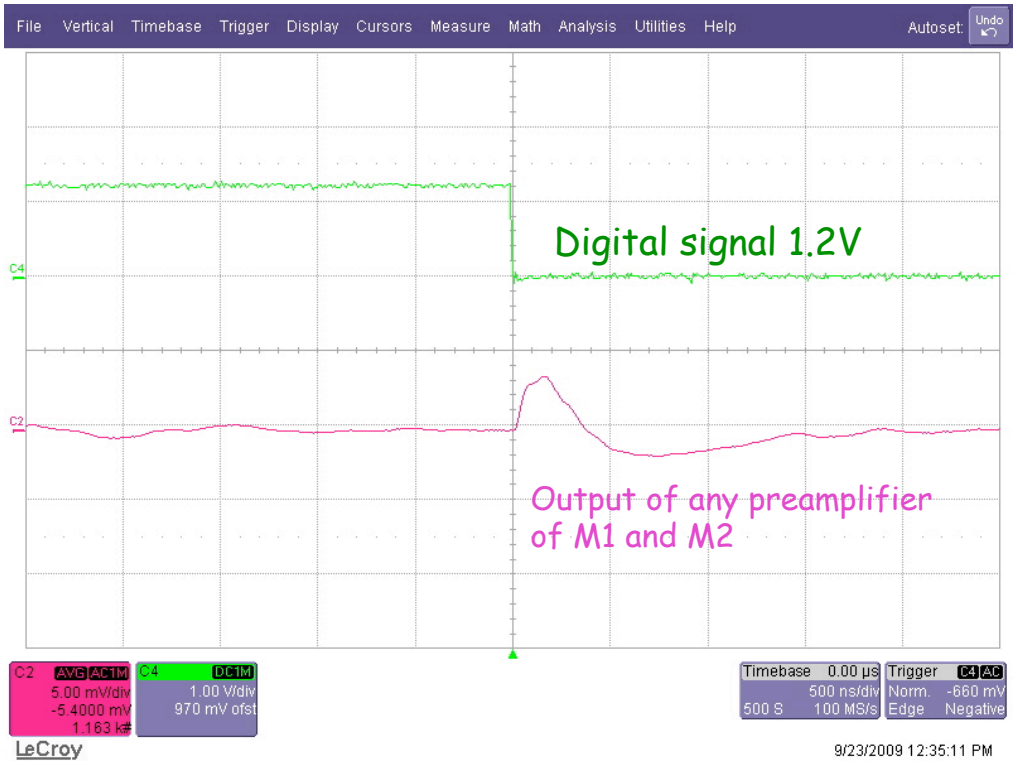
Metal3 and Metal4 shields

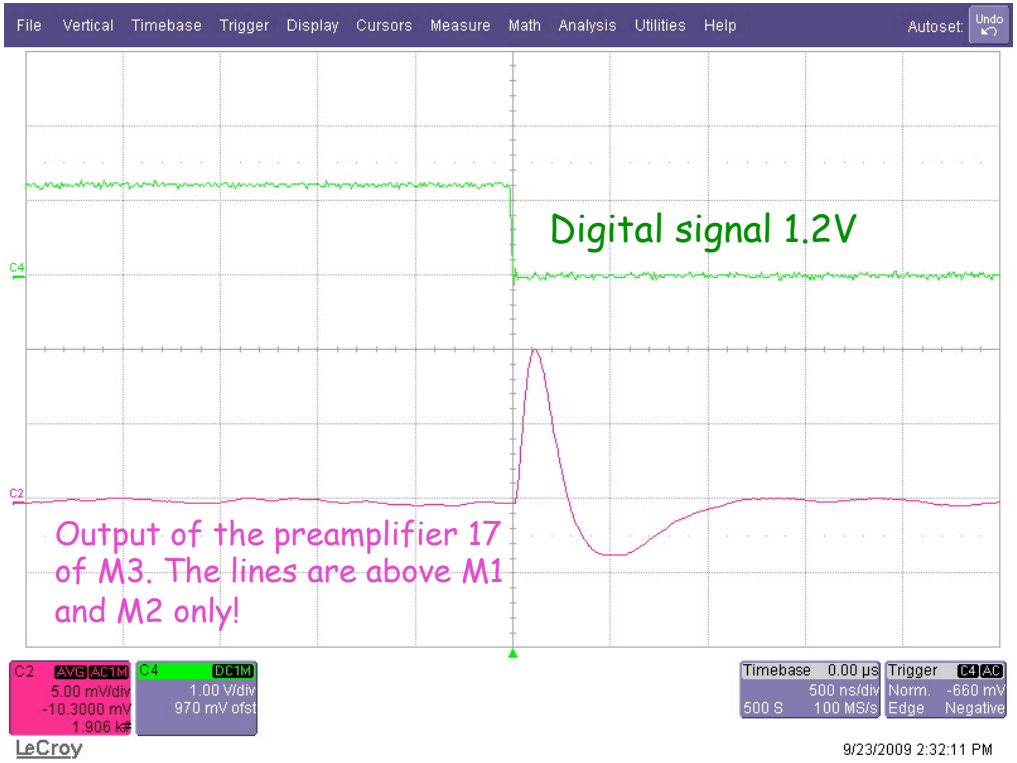
- We used M3 and M4 to distribute analog and digital power and to shield the sensor from the digital activity
- We routed M5 and M6 lines (as digital routing) above the sensor in different positions to test the shields



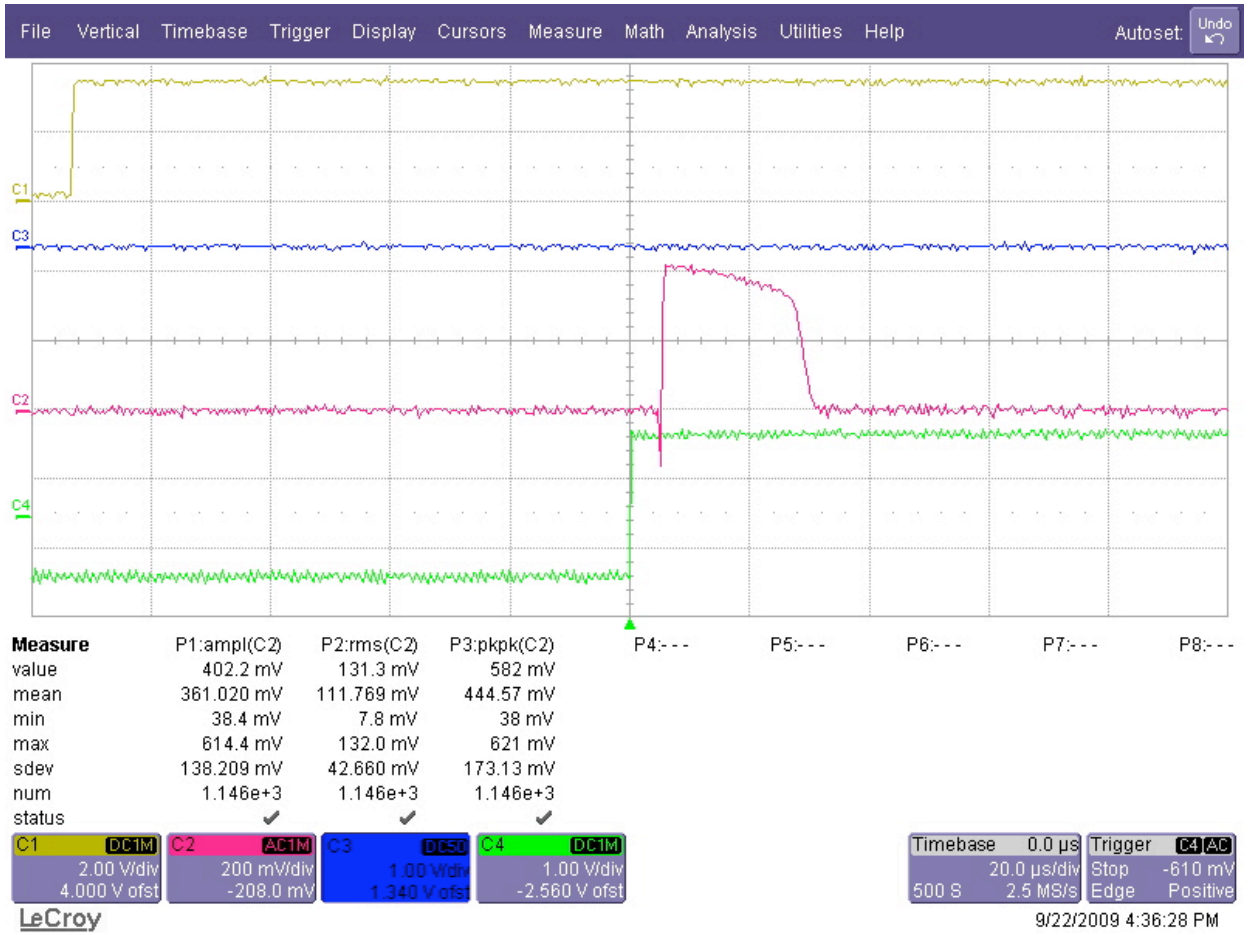


Metal3 and Metal4 shields





Cross-talk or something else



green: CLR_b di M3 of row_enable_x

red: out17_M3 (not dependent on LAT_EN of M3)

The red signal is present (in both chip2 and chip3) at all the analog outputs available of the chip (9 of M1, 9 of M2 and out17_M3)

It is not a capacitive coupled signal.

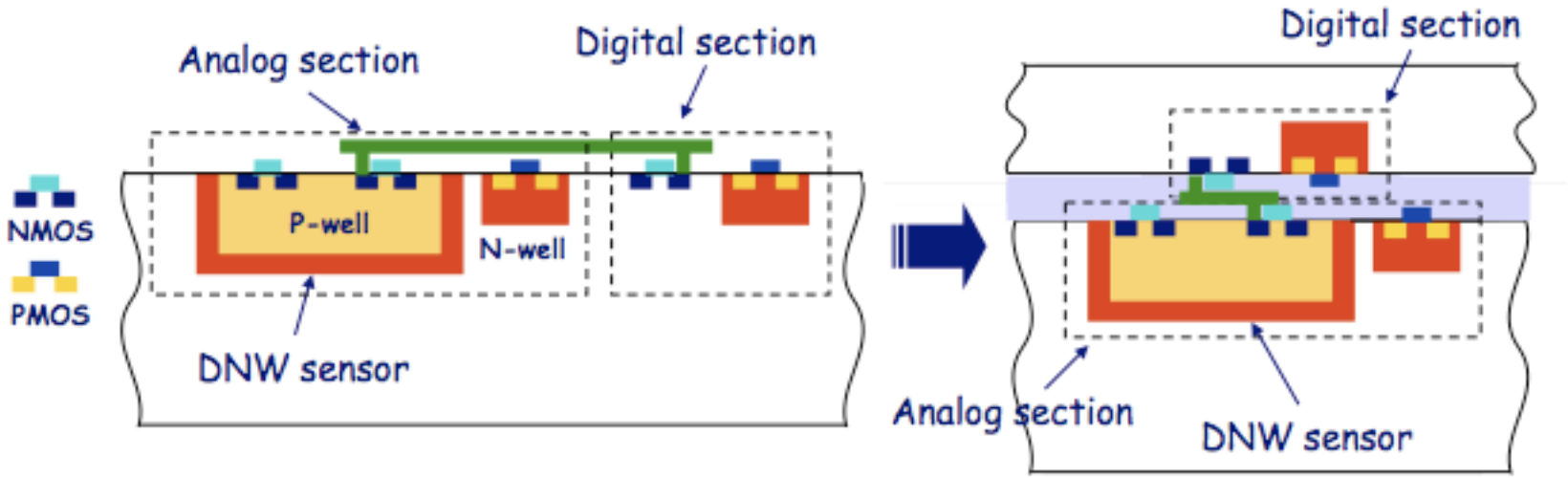
Dependent on the test set-up? Apsel5T has to be measured with a new test board.

Could be due to a drop of the analog ground.

5us delay with respect to CLR_b signal (not present at the falling edge of CLR_b). Not present every time there is CLR_b.

DNW MAPS in 3D CMOS technology

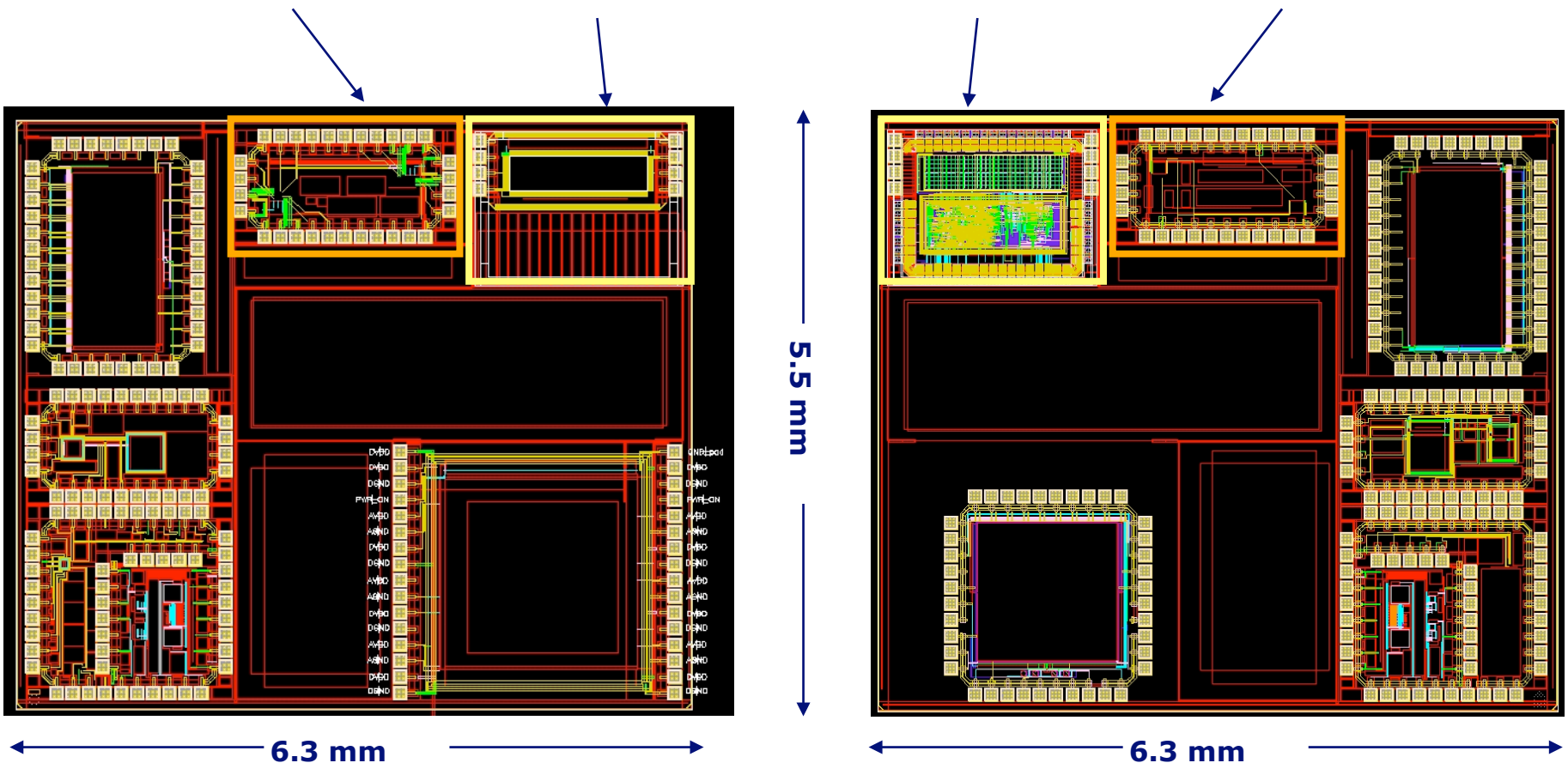
➢First guideline: separate analog from digital section to minimize cross-talk between digital blocks and sensor/analog circuits



➢Tier 1: collecting electrode (deep N-well/P-substrate junction) and analog front-end and discriminator

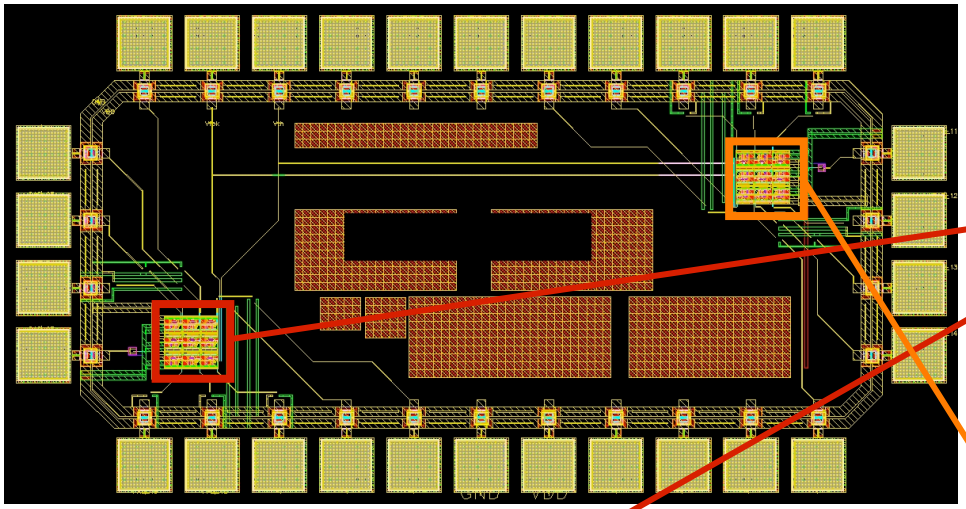
➢Tier 2: digital front-end (2 latches for hit storage, pixel-level digital blocks for sparsification, 2 time stamp registers, kill mask) and digital back-end (X and Y registers, time stamp line drivers, serializer)

Test structures chip layout: bottom and top tiers



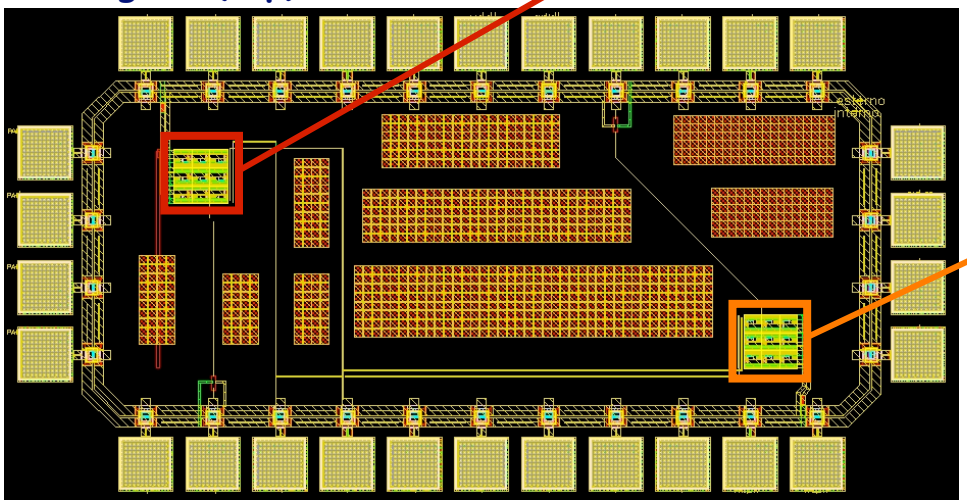
Small test structures

Analog (bottom) tier



3x3 matrix with all the analog outputs available, injection capacitance for the central pixel

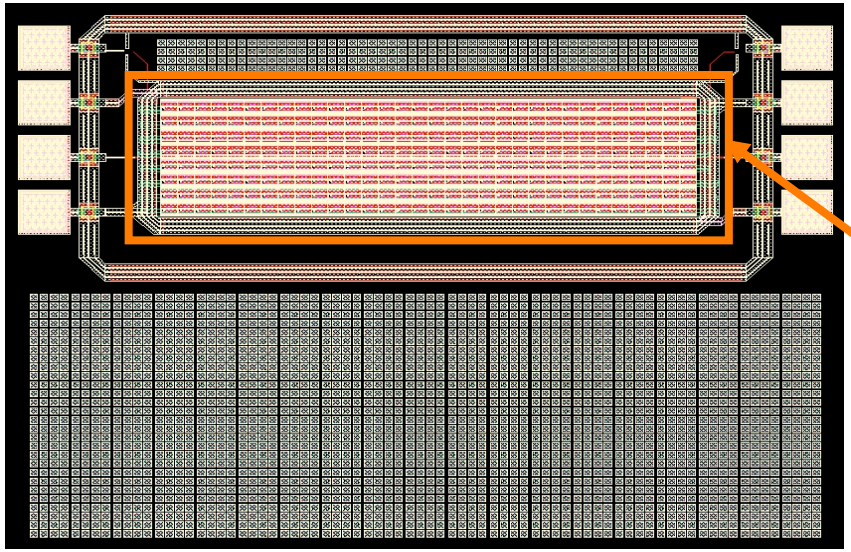
Digital (top) tier



3x3 matrix with all the analog outputs available, injection capacitance for the central pixel, enclosed layout transistors as input devices of the analog FE

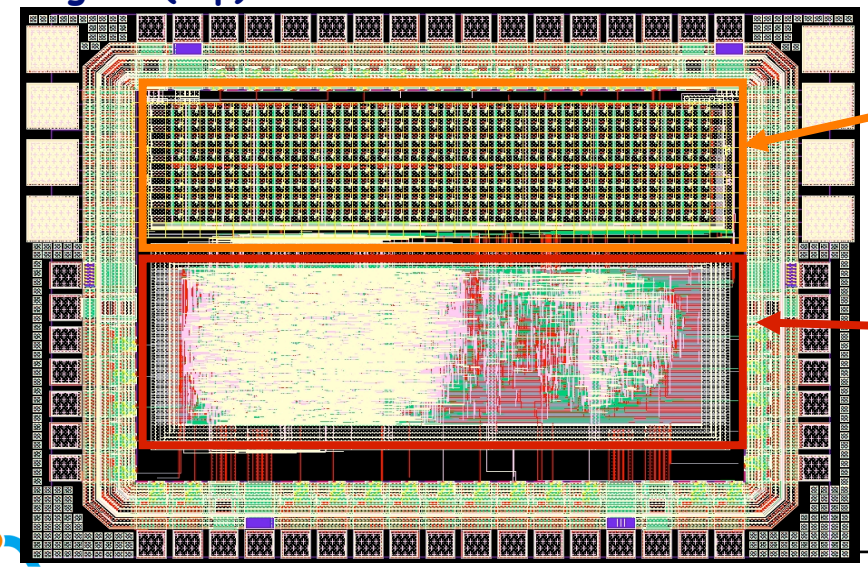
8x32 matrix with data driven readout

Analog (bottom) tier



Sensor and pixel-level analog front end

Digital (top) tier



Pixel-level digital front end

Digital readout electronics

From R. Yarema's talk (TWEPP 09, Sept. 21-25)

Timeline

- First Designers meeting held Dec 11, 2008
- Subsequent meeting in February, March, and May 2009
- All designs initially submitted by mid May
  - Continuous checking of designs by Tezzaron and Fermilab identified numerous problems
    - Inconsistent layer map tables between designs
    - Different DRC violations found with Assura, Calibre, and Magma
    - Non uniform bond interface across all subreticules
    - Via size confusion related to 2 top metals
    - Non mirroring of design in frame
    - Adding of high resistance poly option
    - Computer system crashes at Tezzaron
    - Problems with MicroMagic and Magma
    - Satisfying/answering all of Chartered's questions
  - Items changed during review process
    - Dummy fill program
    - Via density rule
    - Newer DRC versions uploaded.
- Masks started for 31 wafers
- 8 weeks for wafer fabrication.
- 4 weeks for 3D assembly

Topical Workshop on Experiments
for Particle Physics

Conclusions

In R&D activity for the Layer0 of SuperB three different approaches are being followed

- We have submitted a 32x128 matrix for hybrid pixel detector (fine pixel pitch 50x50um2) in a planar 130nm CMOS technology (STMicroelectronics)

- Latest version of Apsel family chip (Apsel5T) has been fabricated in a planar 130nm DNW CMOS technology (STMicroelectronics) and the characterization of the chips are in progress

- First prototype of an Apsel-like chip has been submitted for fabrication in a 130nm vertically integrated (3D) CMOS technology. The mask fabrication has started. Delivery of the chips is expected for December 2009. Test activity is planned for January 2010.