Hybrid pixel readout chip: FE4D32x128

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Outline

- Target operating conditions
- Matrix overview
- Readout architecture
- Slow control interface
- Simulations
- Efficiencies
- Test Chip

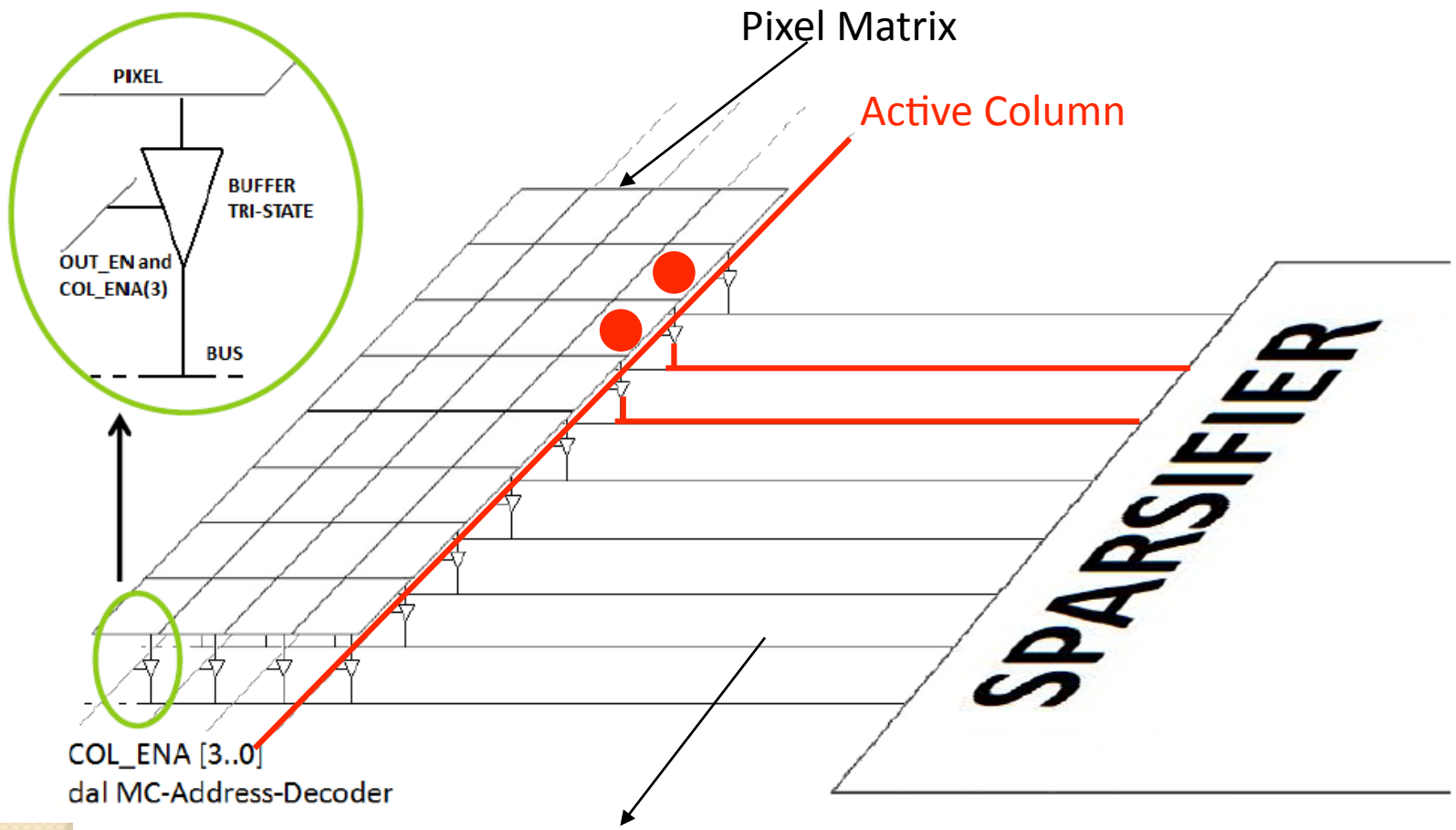
Target conditions

- 100 MHz/cm^2 hit rate

  (compatible with the rate foreseen in SuperB Layer0)
- 0.25 – 2.0 µs BCO clock:
  - Time Counter clock – event granularity
- 60-100 MHz Matrix Clocks
  - Two clocks – one fast at output queuing system
- 3 Gbit/s data bus bandwidth per chip

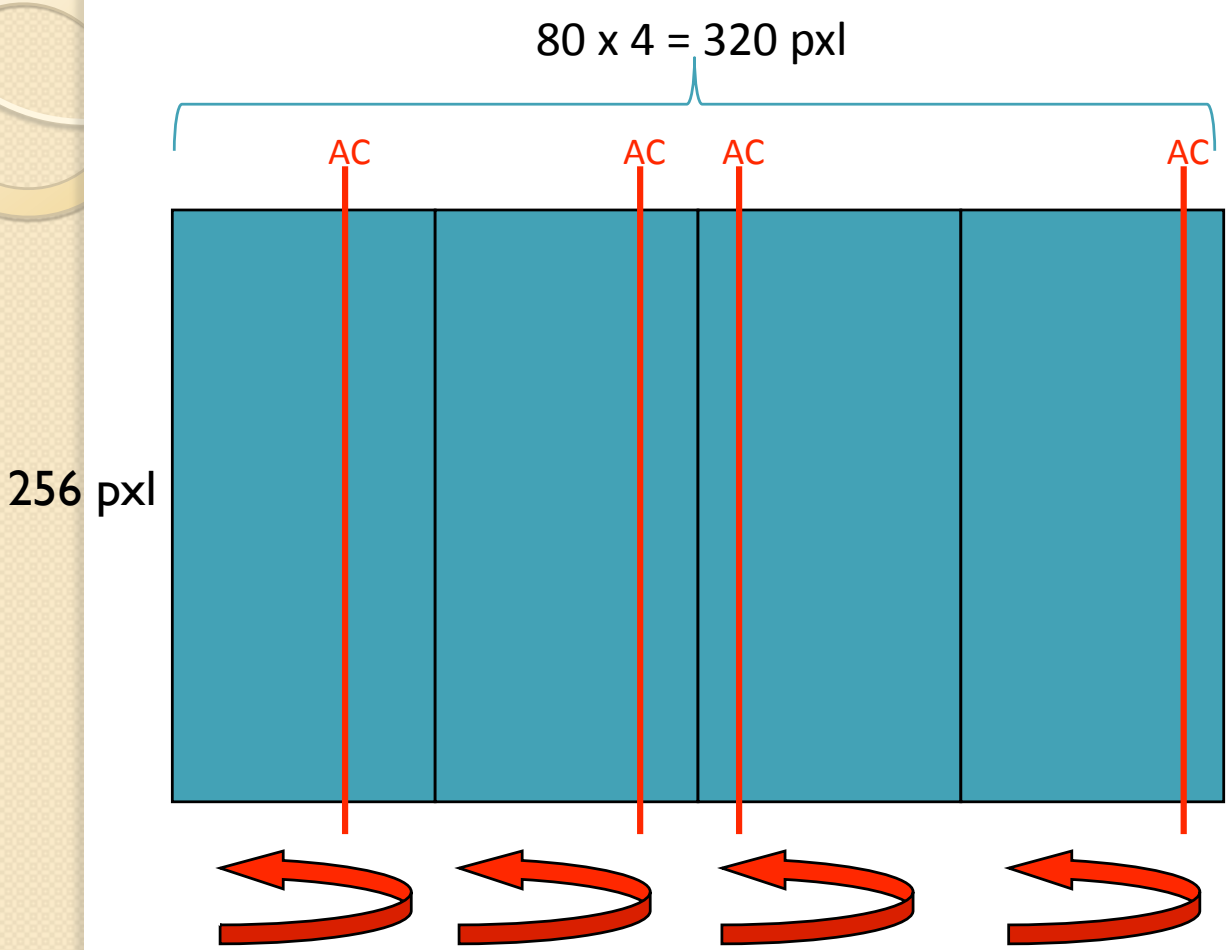
Matrix overview

- Binary **pixels matrix**
- Column-wide **shared data-bus**
- **One column read per clock cycle**



Common Pixel Data Bus – Active 1 column of pixel at a time

Foreseen matrix 320x256



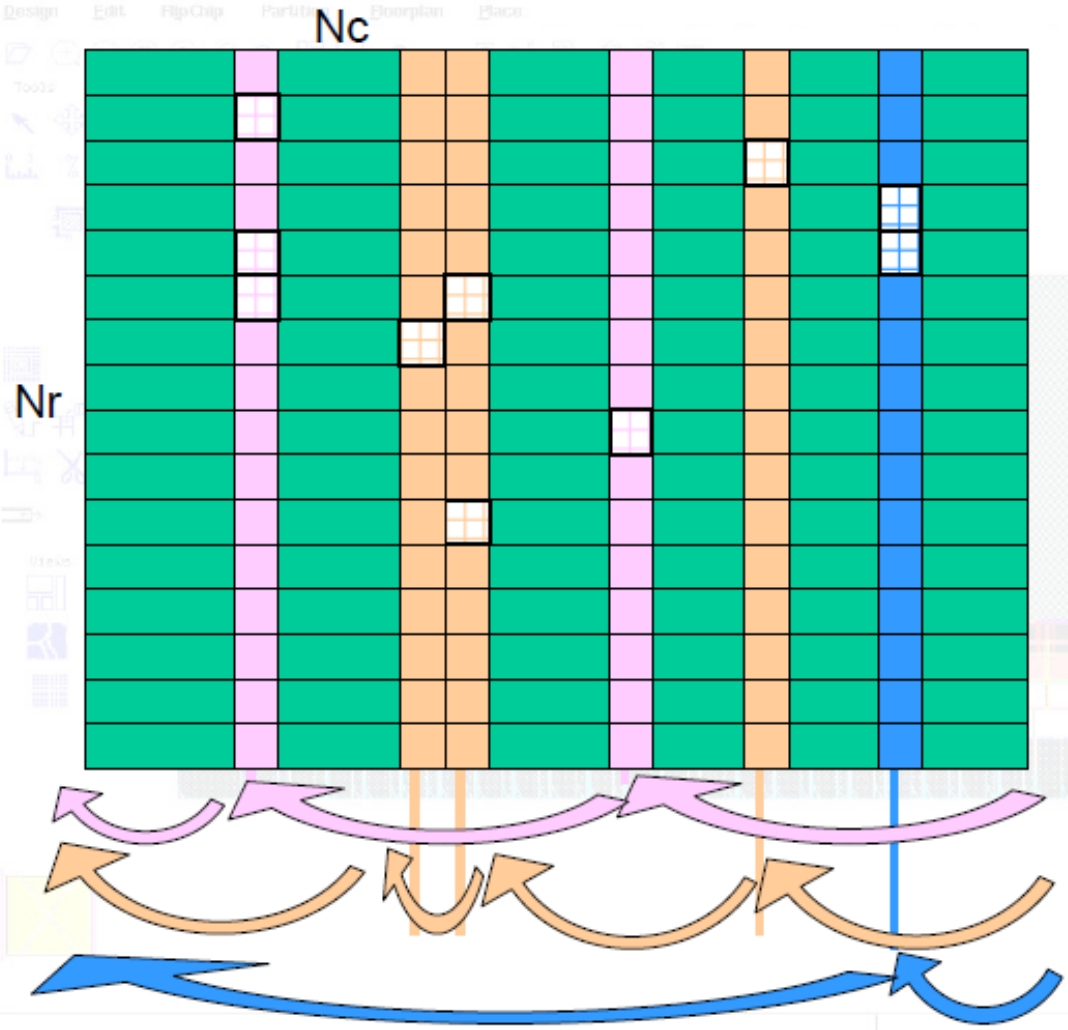
- 80K pixel matrix
- Total area ~ 1.3 cm²
- 130 Mhit/s

4 parallel submatrices

256 x 4 = 1 024 pxls/CLK
@50MHz → 50 Gpxl/s

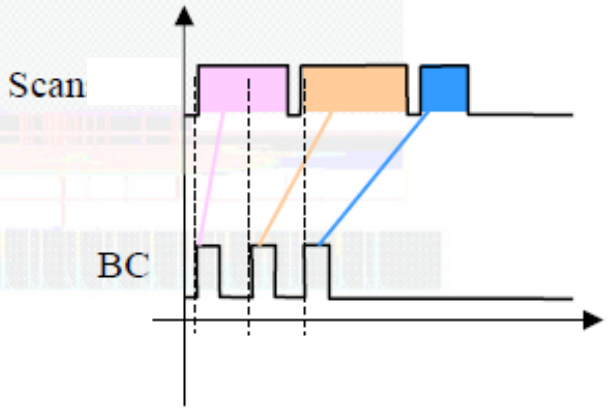
4 horizontal **parallel** scans for the Active Column
80 x 256 pxl, **40** μm pitch

Time-sorted data



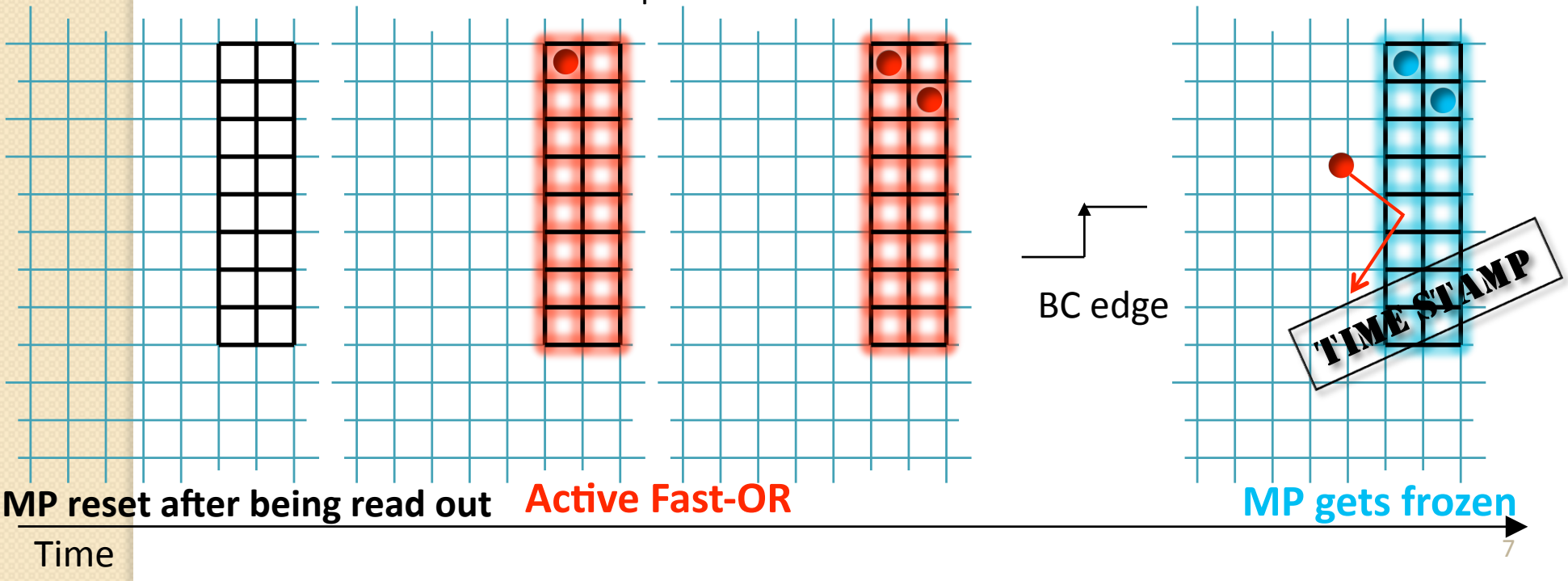
Hit-TS1
Hit-TS2
Hit-TS3

Column scan time oriented:
1 scan for each Time Stamp
→ The hits are time sorted



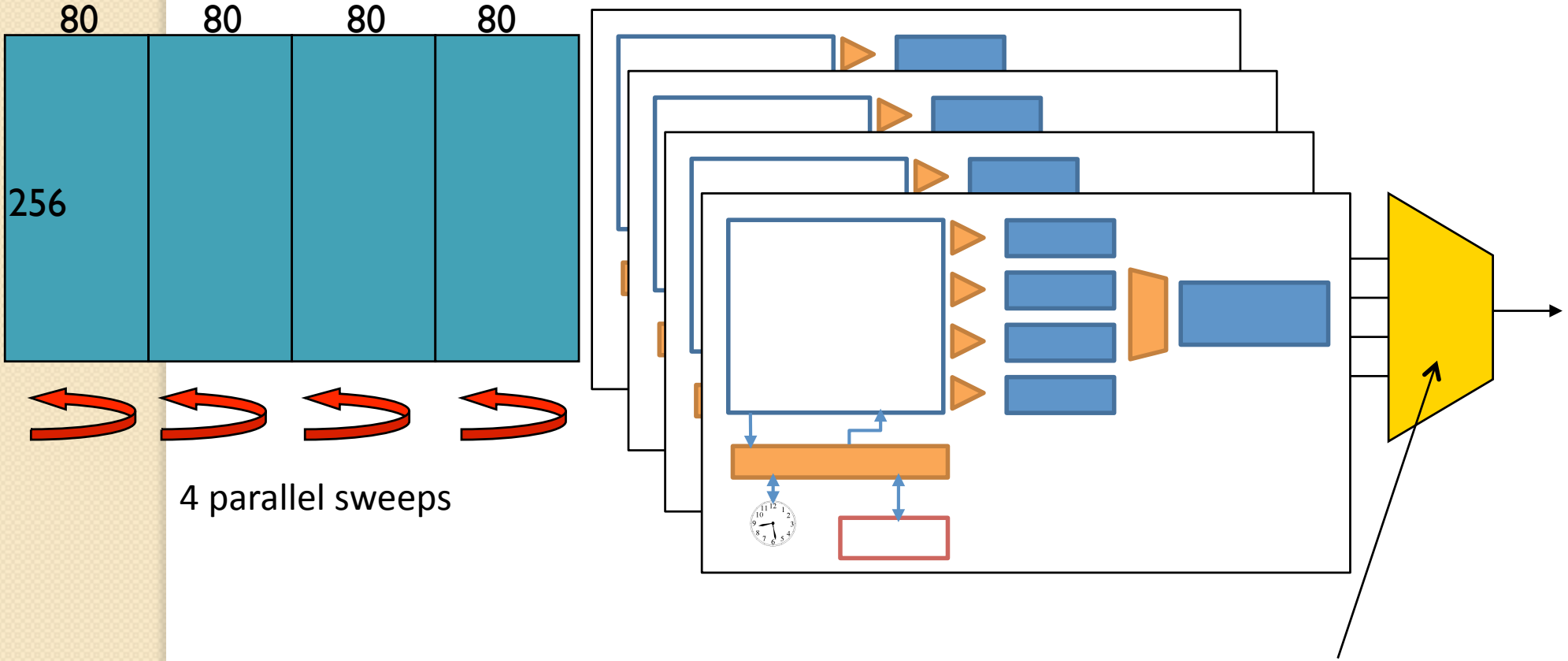
The Macro Pixels

- Matrix divided into MPs: **group of pixels** (2x8)
  - MP global lines:
    - **Fast-OR line:** (MP output) inclusive OR of all pixel latches.
    - **Freeze line:** (MP input) disable the reception of new hits.
  - On BCO time all MPs **with active fast-OR** :
    - Gets frozen
    - Are associated to the current value of BCO counter (Time Stamp)
    - read out and reset a.s.a.p.

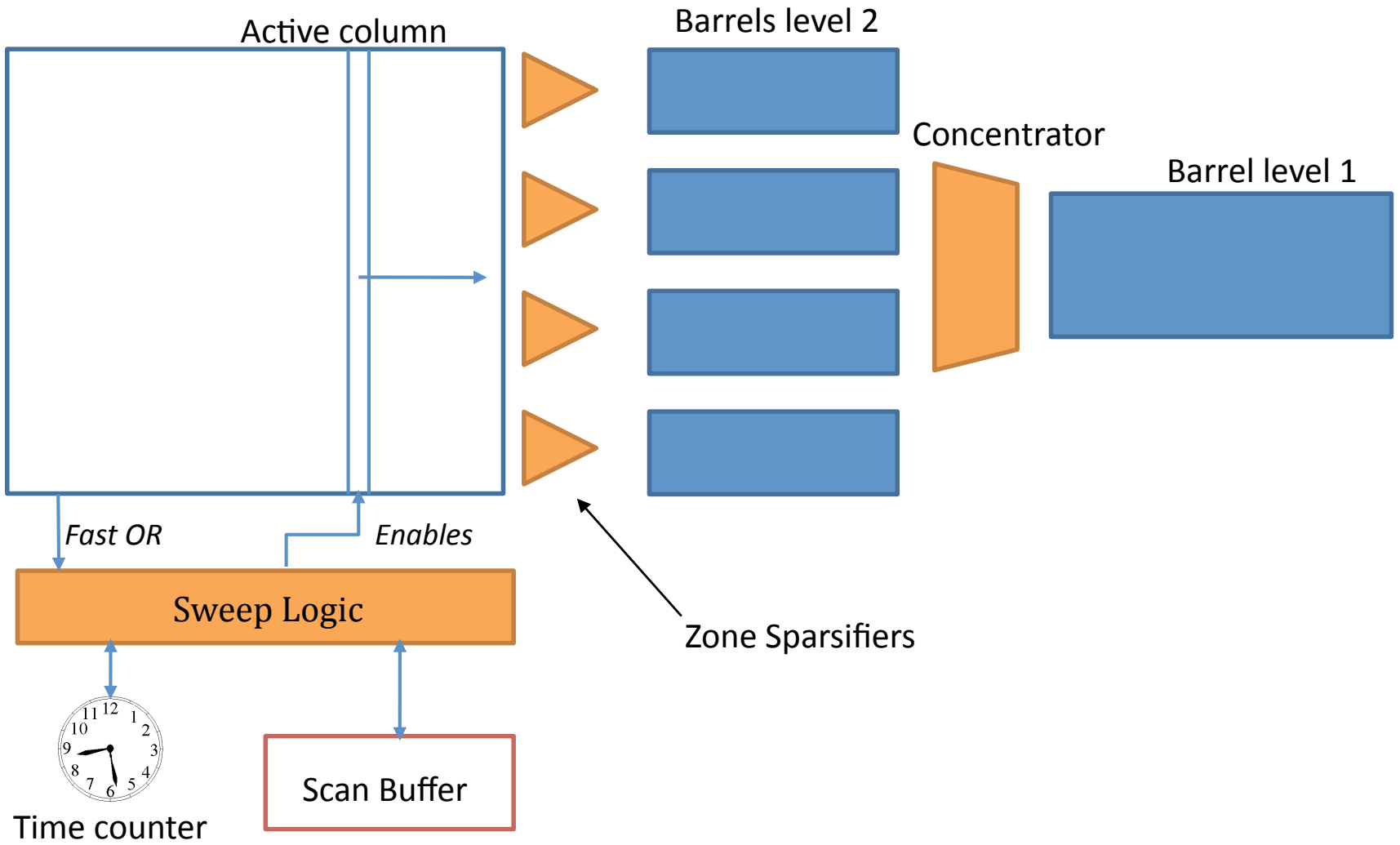


Matrix readout architecture

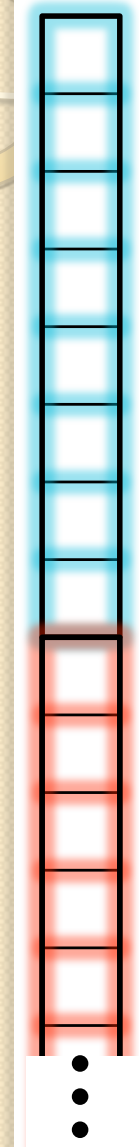
- Each sub-matrix scan has its own readout & scan logic
- All readout working in parallel
- Queuing output system



Sub-matrix readout architecture



Zone sparsification



- The **256 pixels** of the Active Column are **divided into 32 vertical zones (1x8 pixels each)**
  - HIT= (**Zone address**+ **Zone pattern**)
    - X zone address = Column address for 80 columns →7 bit
    - Y zone address : 32 vertical zones → 5 bit
    - Zone pattern: 8-pixel zone → 8 bit (not coded)

- **Time Stamp**: as the hits are time sorted, the relative TS word is stored at the beginning of each hit sequence

Output coded 20-bit data format

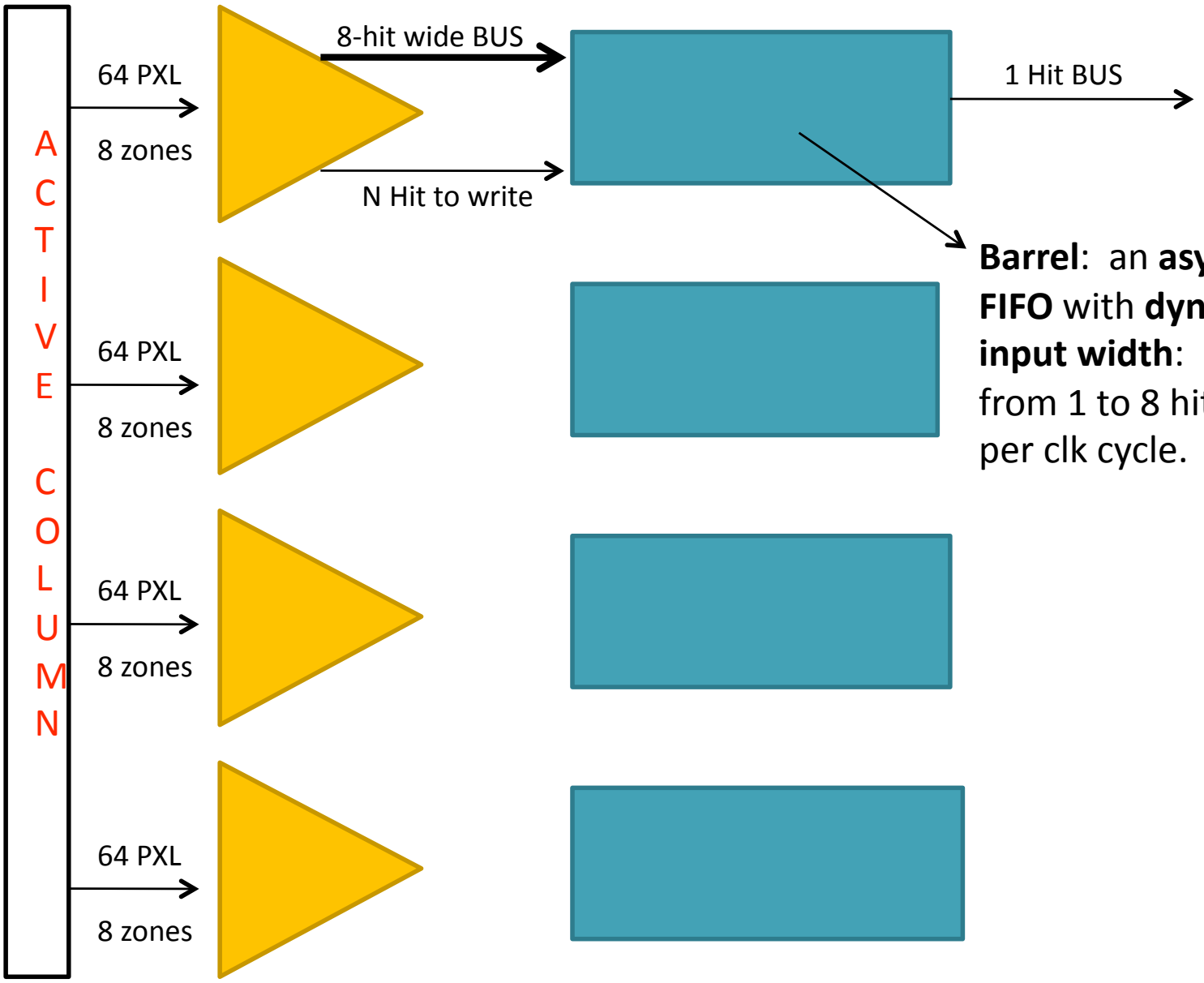
- A) "**Time stamp word**"
  - bit[19] = 1
  - bit[18:10] = XXXXXXXXX
  - bit[9:8] = submatrix address
  - bit[7:0] = time stamp

- B) "**Hit Word**"
  - bit[19] = 0
  - bit[18:17] = sparsifier address
  - bit[16:14] = Y zone address
  - bit[13:8] = X zone address
  - bit[7:0] = pattern of the zone (clear)

80310	**Time**
38380	Data
0CB01	Data
19340	
1D602	
49804	
09E04	
26208	
2AB20	
02E01	
1F508	
17620	
4FC01	
80010	**Time**
4C240	Data
04801	Data
0C910	
44C20	
28D01	
……	

Depending on the hit distribution a non space-time format reduces the bandwidth

The sparsifiers and circular barrels

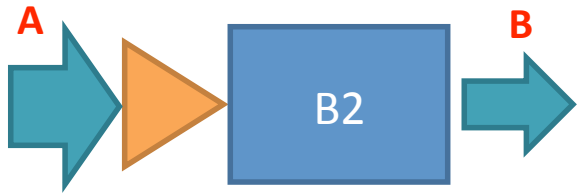


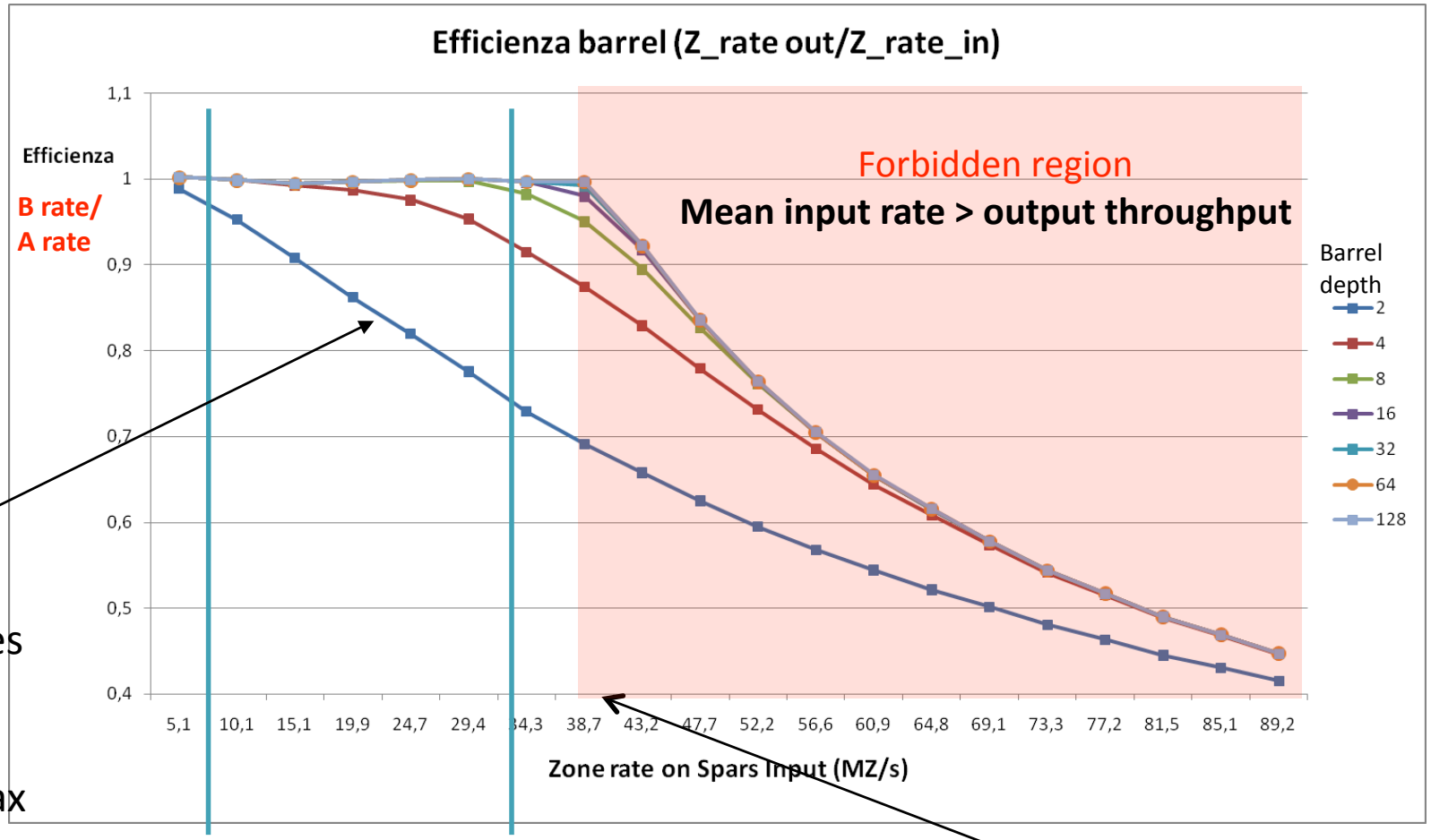
Barrel: an **asymmetric FIFO** with **dynamic input width**:
from 1 to 8 hits stored per clk cycle.

VHDL model simulations

- Parameterized VHDL model
  - expected working conditions (hit rate, clock frequency …)
  - Barrels depth
  - Zone width
- Efficiencies estimation

Study on Barrel Depth (hit cluster)





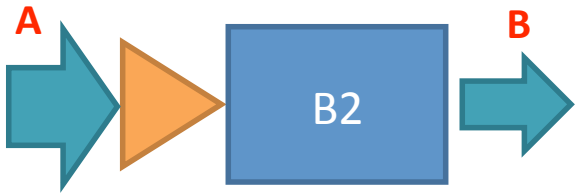
Barrel inefficiencies due to fluctuation over the max throughput

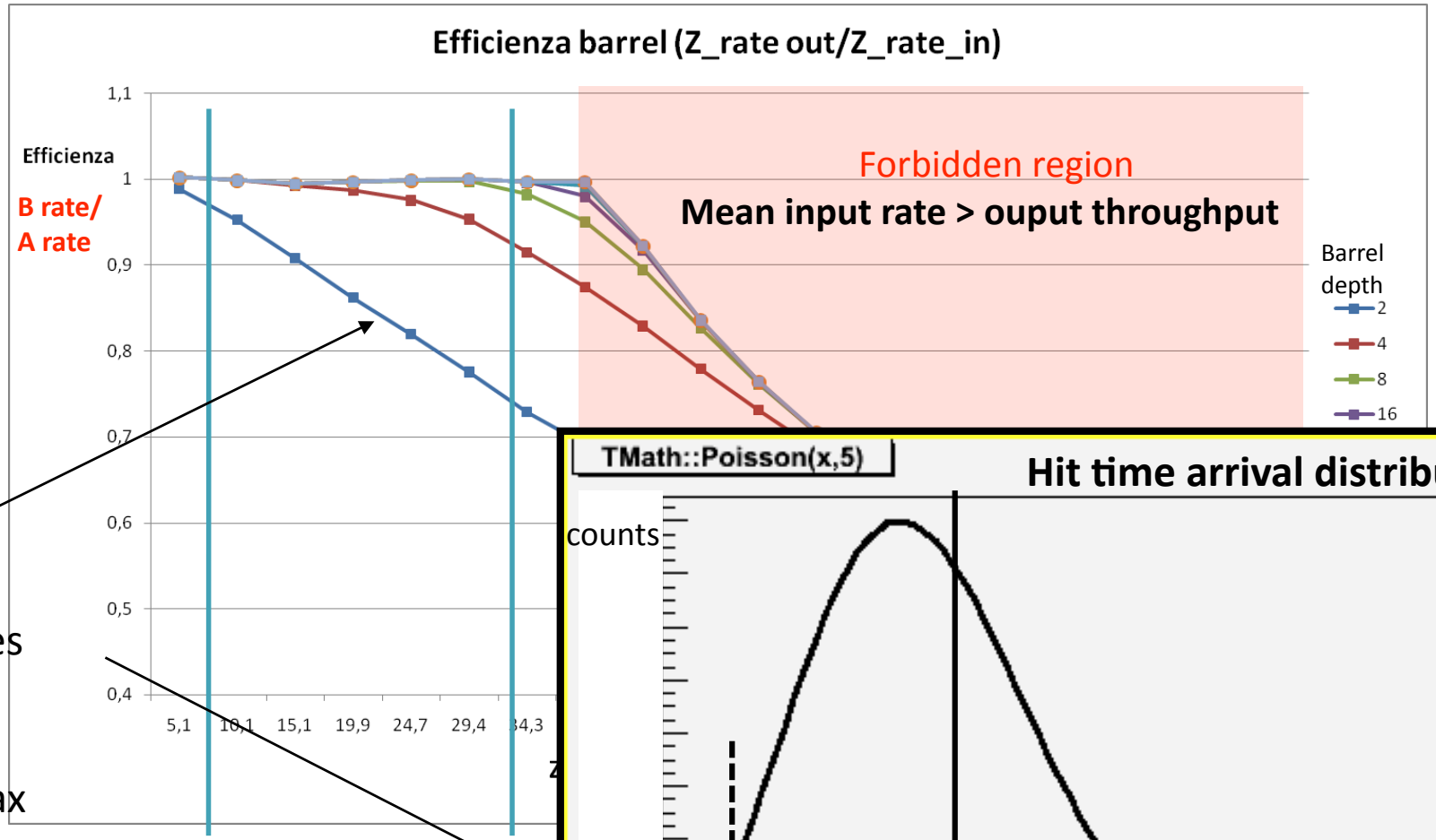
Expected rate @**B2**: 8,2 MPxl/s

Expected rate @**B1**: 32,8 MPxl/s

Barrel clock 40 MHz

Study on Barrel optimal Depth:





Barrel inefficiencies due to fluctuation over the max throughput

Expected rate @**B2**:
8,2 MPxl/s

Expected rate @
32,8 MPxl/s

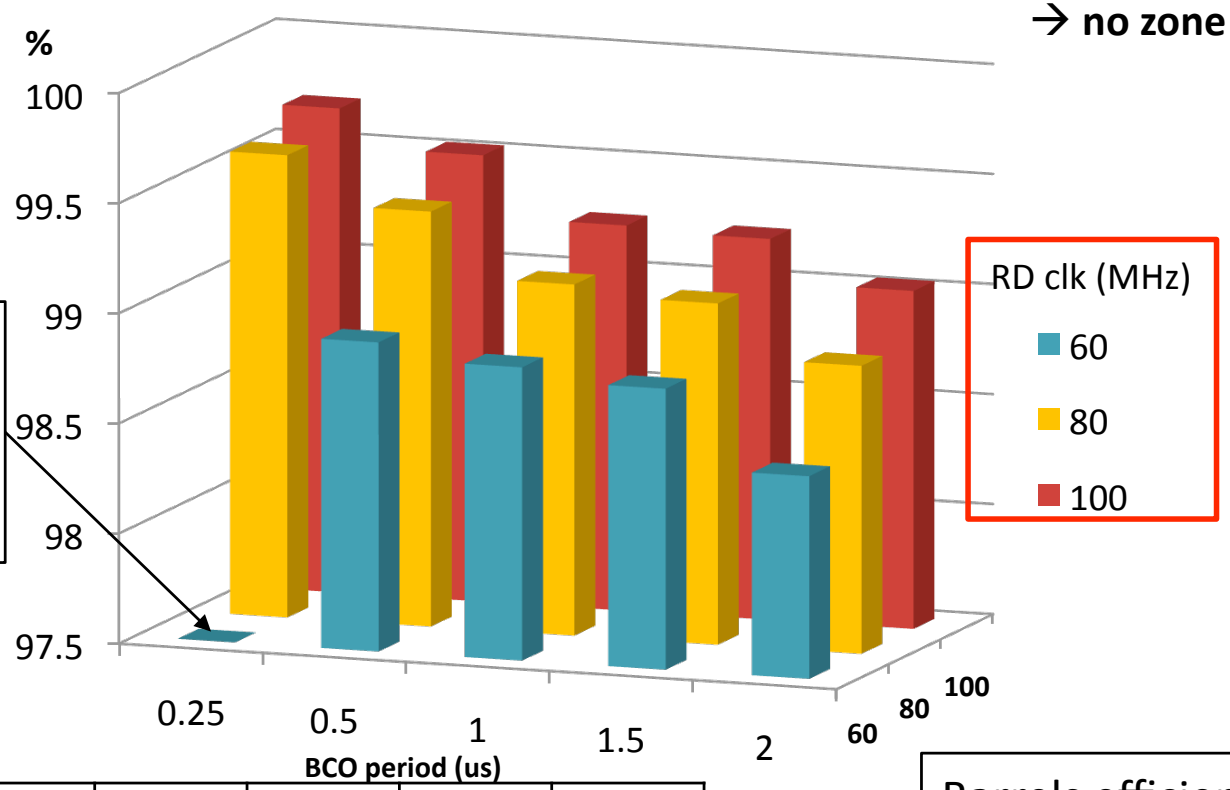
Efficiencies

- Two sources of inefficiency due to digital readout:
  - **Frozen MP inefficiency**: hits generated on a frozen MP are lost.
  - **Overflow B2-1 inefficiencies:** buffer full

Frozen MP Efficiency @ 100 MHz/cm^2

(1 sub-matrix readout instance)

(Random and no clusters → **no zone benefits** at this rate)



Efficiency drop induced by the overflow of *Scan Buffer*: Longer freezing time

frozen effi.						
				BCO (us)		
		0,25	**0,5**	**1**	**1,5**	**2**
	100	99.7	99,5	99,3	99,2	99,0
Rd_clk (MHz)	**80**	99,6	99,4	99,1	99,1	98,8
	60	97,5	98,9	98,8	98,8	98,4

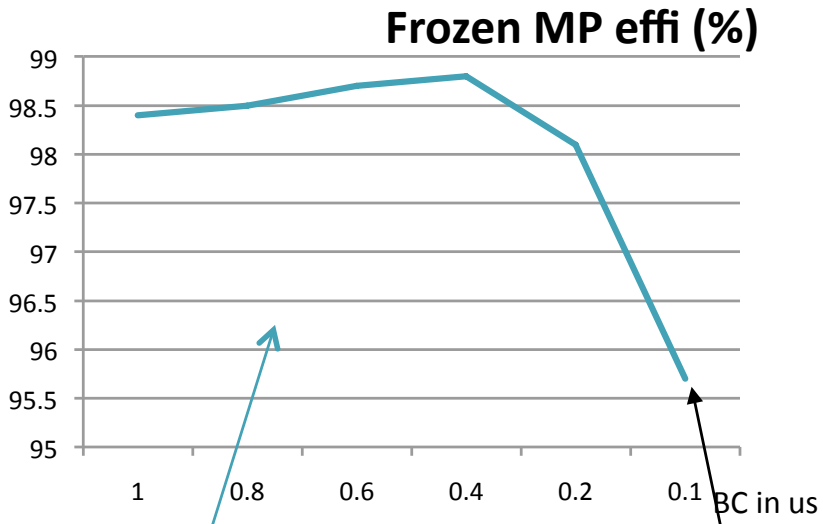
Barrels efficiency **100%**
No barrel overflow
(B2 and B1)

Fast read clock and narrow BC edges

200 MHz/cm^2, Read clk 80MHz, BC=1 us → efficiency 97.6%

Efficiency of whole readout

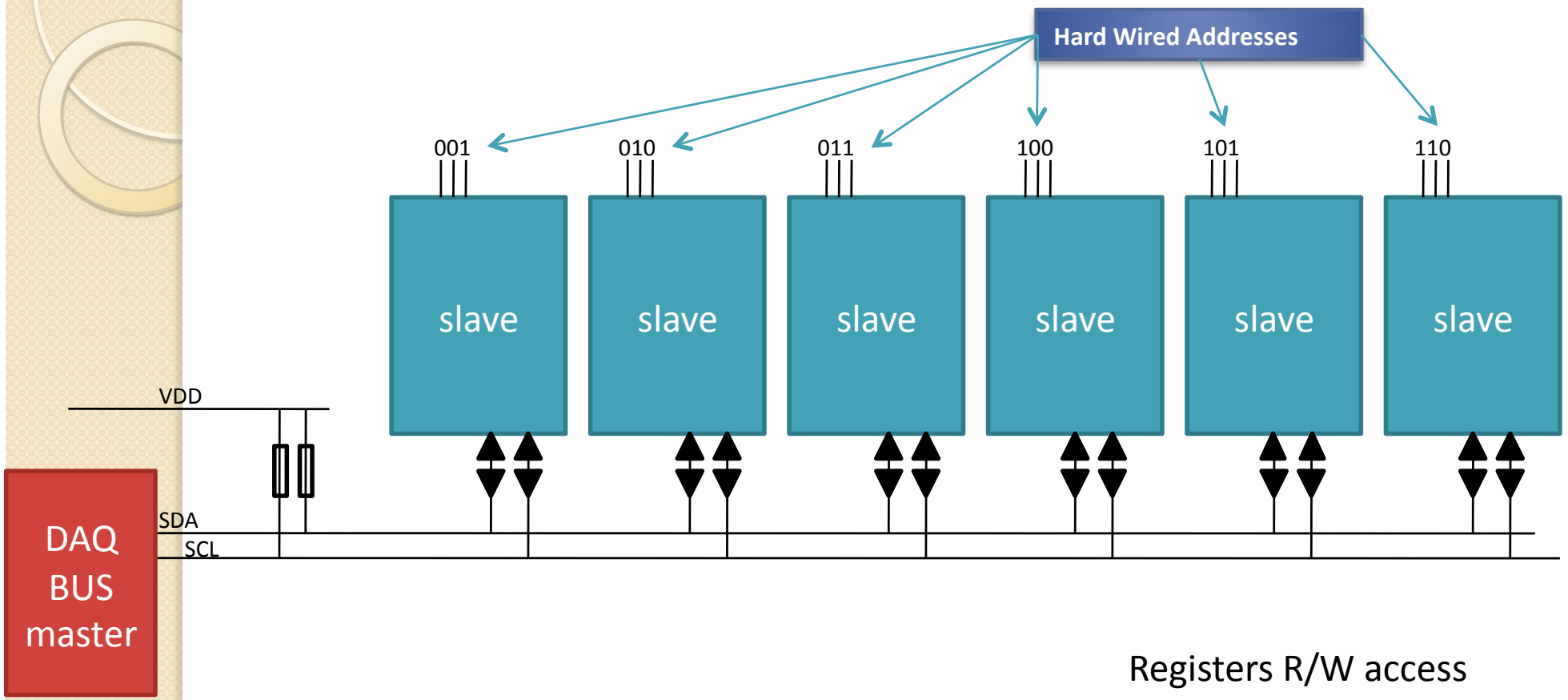
- **4 sub-matrices** & 4 readouts in parallel
- Frozen MP eff. estimated with **faster BC clk** and increased capacity of scan buffer
- RDclk 67 MHz (spars. & matrix scan)
- FastClk 200 MHz (BUS out)
- Scan buffer depth **= 8 and 16**
- rate on area 1,1 MHz/mm2



Run #	sim DURATION (ms)	RDclk (MHz)	BCO (us)	Mean Sweeping time (us)	global hit rate (MHz)	rate on area (MHz/ mm2)	B2 depth	B1 depth	Scan buffer depth	Scan buffer overflow	Frozen MP effi (%)	Overflow effi B2 (%)	Overflow effi B1 (%)
288	1	**67**	**0,8**	0,54	33,8	1,1	8	128	8	0	**98,5**	**100**	**100**
289	1	**67**	**0,6**	0,45	33,8	1,1	8	128	8	0	**98,7**	**100**	**100**
290	1	**67**	**0,4**	0,33	33,8	1,1	8	128	8	0	**98,8**	**100**	**100**
291	1	**67**	**0,2**	0,18	33,8	1,1	8	128	8	3	**98,1**	**100**	**100**
292	1	**67**	**0,1**	0,12	33,8	1,1	8	128	8	**8991**	**95,7**	**100**	**94**
						Increased Scan Buffer depth							
293	1	**67**	**0,2**	0,18	33,8	1,1	8	128	16	0	**98,1**	**100**	**100**
295	1	**67**	**0,15**	0,14	33,8	1,1	8	128	16	4	**95,5**	**100**	**100**
294	1	**67**	**0,1**	0,11	33,8	1,1	8	128	16	**5314**	**92,6**	**100**	**96**

Scan buffer overflow & barrel 1 overflow

The Slow Control bus: I²C-like system



Registers R/W access communication type

I²C : two bidirectional open-drain lines.

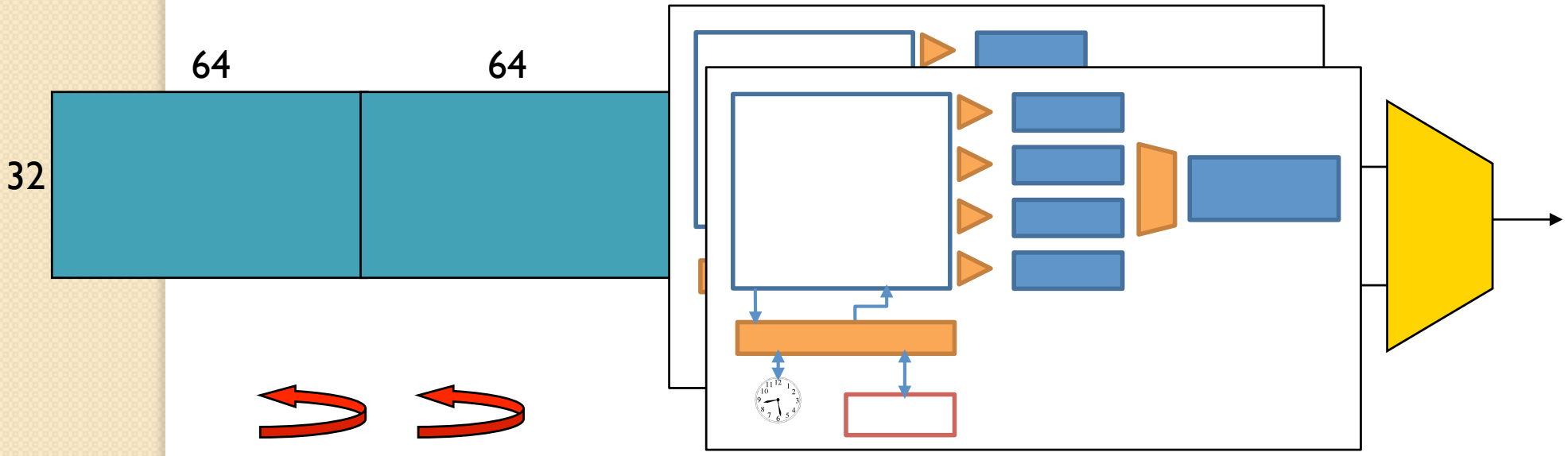
- Serial Data (SDA)
- Serial Clock (SCL), pulled up with resistors.

Slow Control

- 1 Set of Read/Write registers
  - Chip settings
  - MP masks
- 1 set of Read Only registers
  - Acquisition flags
  - Rate counters
  - Error flags

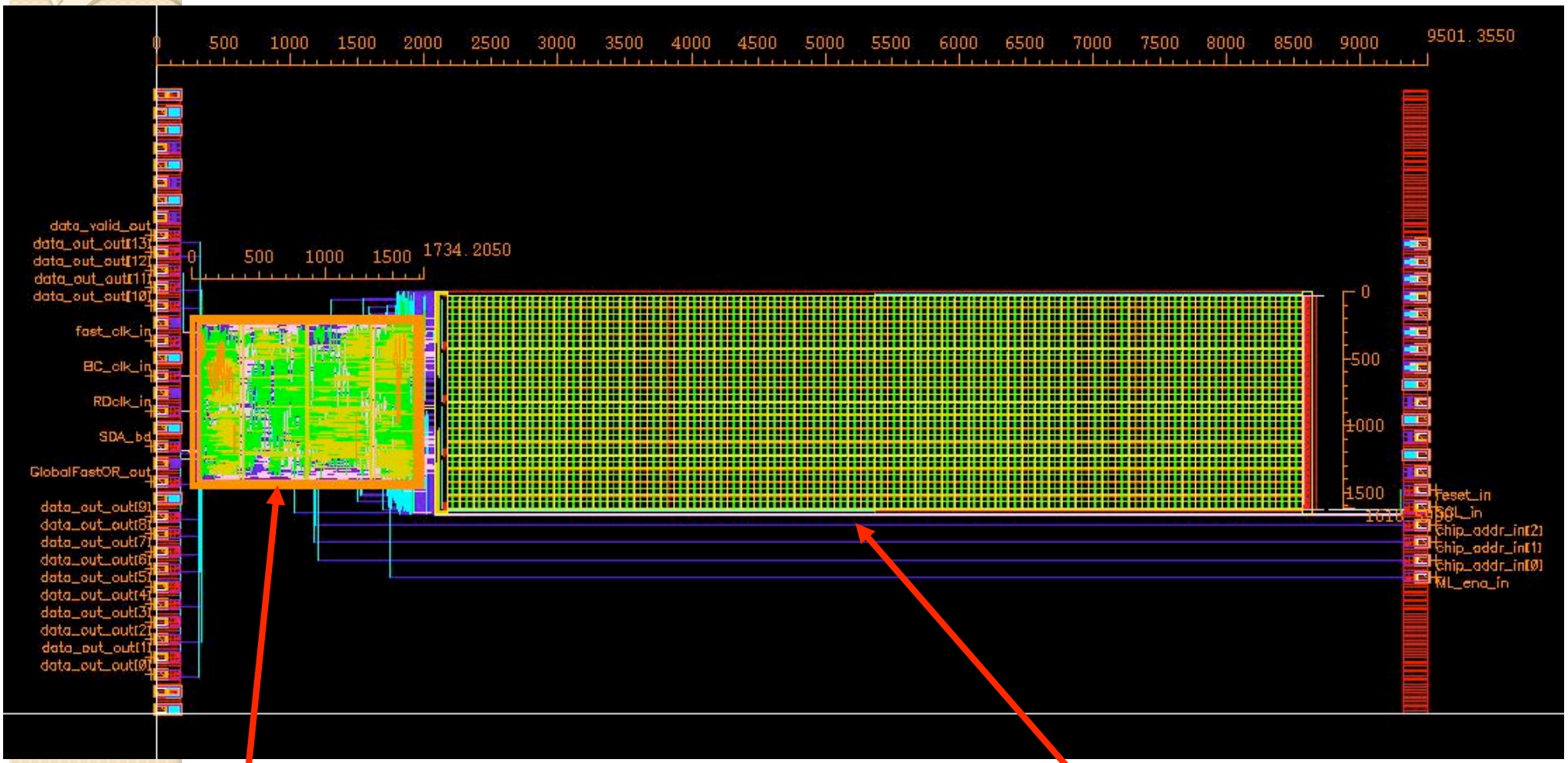
The Test Chip (APSEL family)

- Under submission
- Technology STM 130 nm
- Hybrid Pixels Matrix 128x32 pixels, 50 µm pitch (**1/20** of the target matrix area)
- 2 readout blocks implemented



The Test Chip layout – ST130nm

(VHDL – Synopsys – SoC Encounter – ModelSim – Verilog - SimVision)



Readout

- TOT 60 kGates
- Area < 2 mm^2
  Does not scale with the matrix

Pixel matrix 128x32
Area ~ 10 mm^2

Conclusions

- Design & Development for challenging target conditions
- Optimization of the architecture in several directions:
  - High performance: 100 Mhit/cm^2 rate, processed 50 Gpxl/s
  - High efficiency: 98-99%
  - Bandwidth cost per chip: clusters optimization and time-wise scan halves down the bandwidth
- Test Chip under submission