PID I

- Status and results for the 100 ps TDC (SNATS)
  - Slides from Vanessa's talk at TWEPP (Paris 2009)
- Evolution of SNATS for SuperB
- Test board: hardware and firmware status

We have two different systems to design for the PID.

- For the forward: ~ 10 ps resolution. Analog memories seem the only possible option. Two solutions are under study: G. Warner's boards are already under test and Dominique's board will be introduced tomorrow, first on Jerry's test bench and later on on the telescope.
- For the Barrel:
  - Time resolution: ~100 ps for the electronics
  - Charge measurement foreseen for all the channels ?

    => both for physics and for timing correction .
  - Can the trigger rate (MHz per channel ?) be compatible with a TDC structure, especially the readout

We want to lead the two different studies in parallel.

For the forward PID: the development on analog memories is not "SuperB-dependent ".

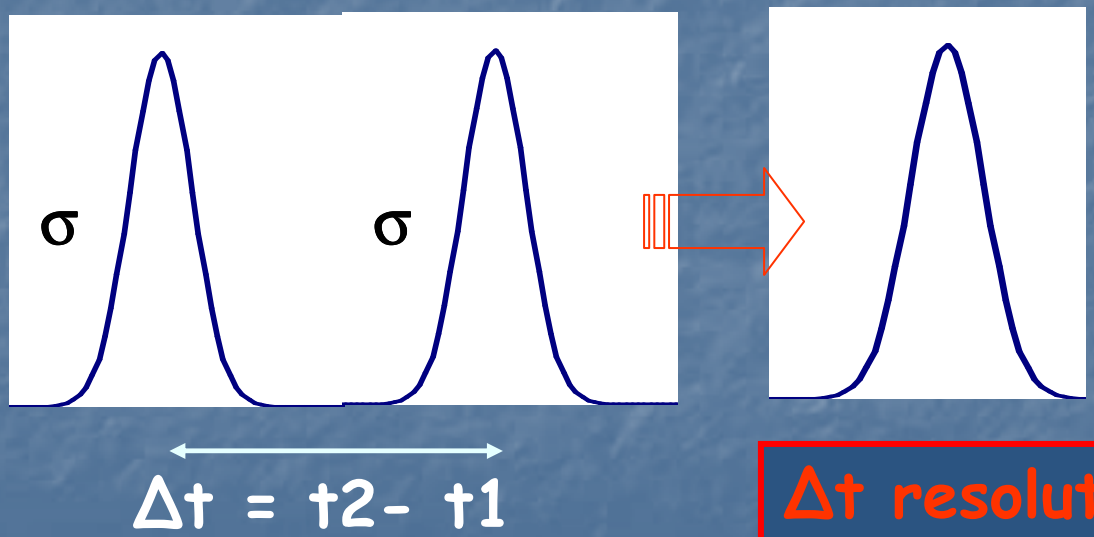
For the barrel : the current technique is quite mature. The development is specific for SuperB even if this new TDC could interest a large community concerned by time measurement

- We propose to design a TDC based on the SNATS developed for SuperNemo experiment: does the performance of the current chip match our requirements ?
- Before preparing a specific version we have to agree on the evolutions we propose.
- We have designed a test board for SuperNemo. Can we adapt it to the telescope setup and can we learn something with it ?

Time stamper vs TDC

- TDC: time measured between a Start & a Stop
- Time Stamper: absolute time measurement

SuperNemo experiment: 2 events will be stamped ⇒ $\Delta t = t2 - t1$

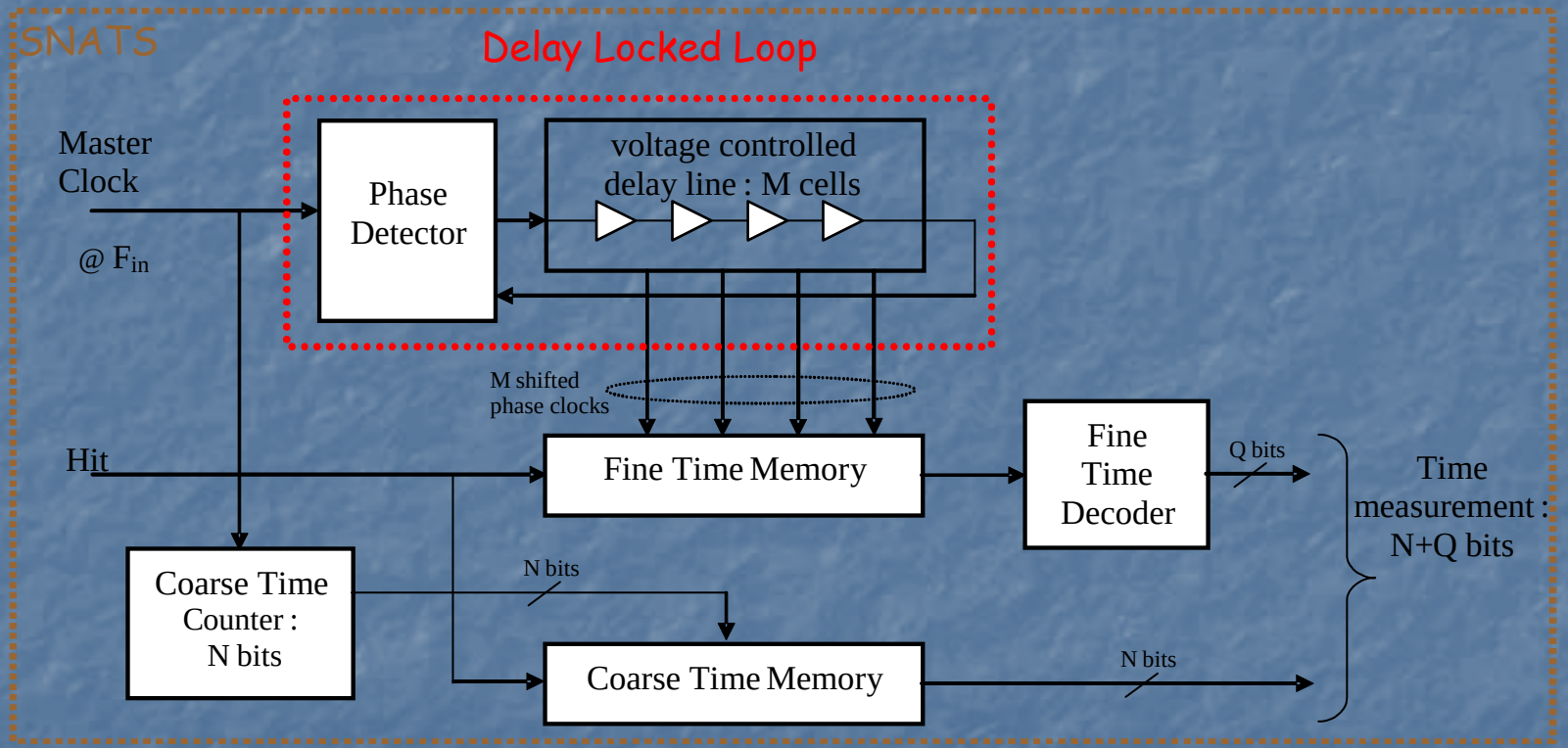


$\sigma_t = \sigma \sqrt{2}$

Δt resolution degraded by a factor of √2

SNATS: principle

One fine time measurement (high resolution) ⇨ DLL
One coarse time measurement (range) ⇨ N-bit counter

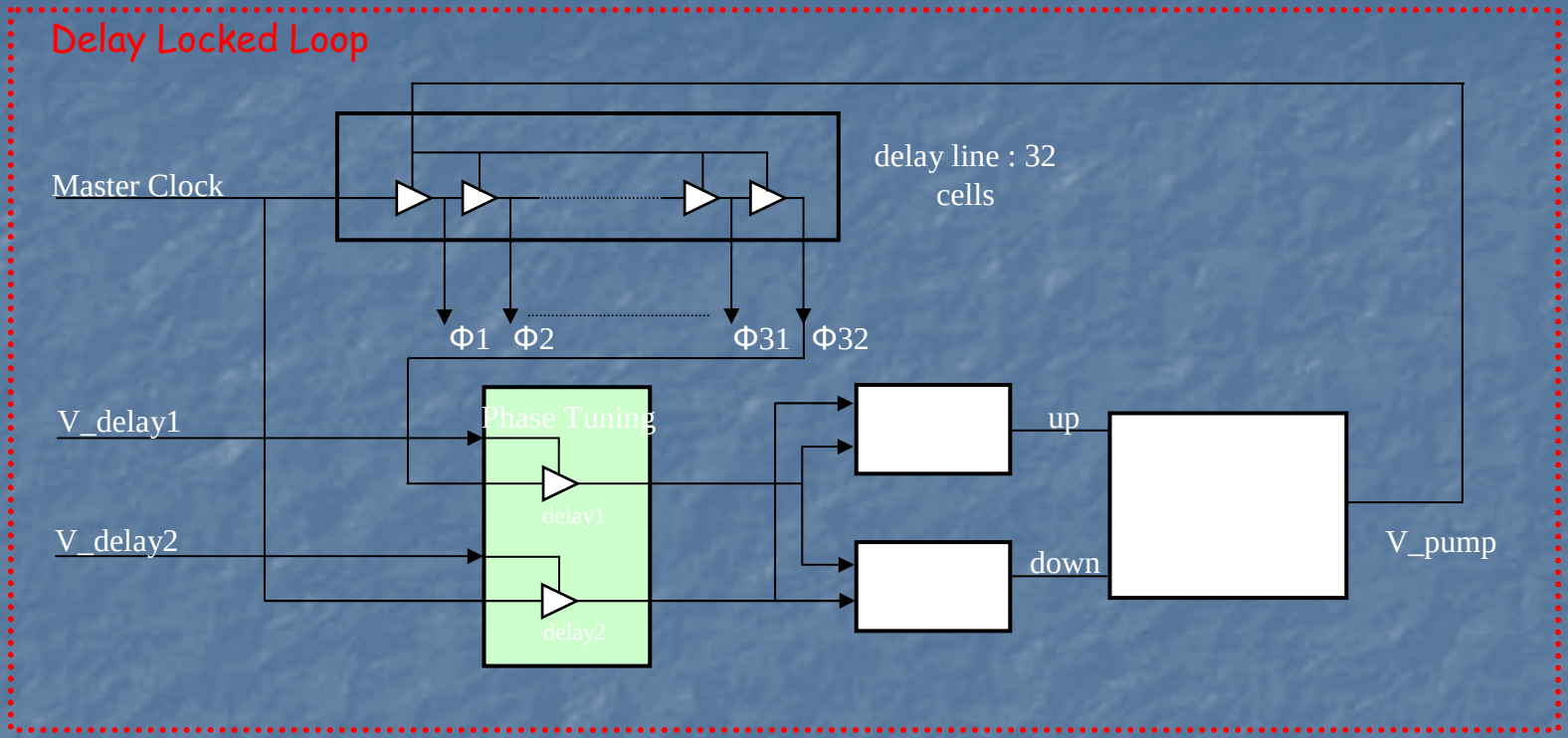


SNATS target performance summary

- Technology Process: AMS CMOS 0.35µm
- Clock Frequency: 160MHz
- Number of cells: 32 (limited by the INL)
- Dynamic Range: 53 bits
  - 48 clock counter bits
  - 5 interpolator bits
    - Time coverage: 20 days
- LSB = 200 ps
- DNL < 10% of the LSB
- Channels per chip = 16
- Readout dead time per channel: 400ns => 16 *400 for 16 channels
- Production: shared run as for Babar. Cost: 67 Euros / chip based on a recent production of ~500 chips .
- Not " naturally " protected against SEL => need of a radiation test of SNATS in beam

SNATS challenges

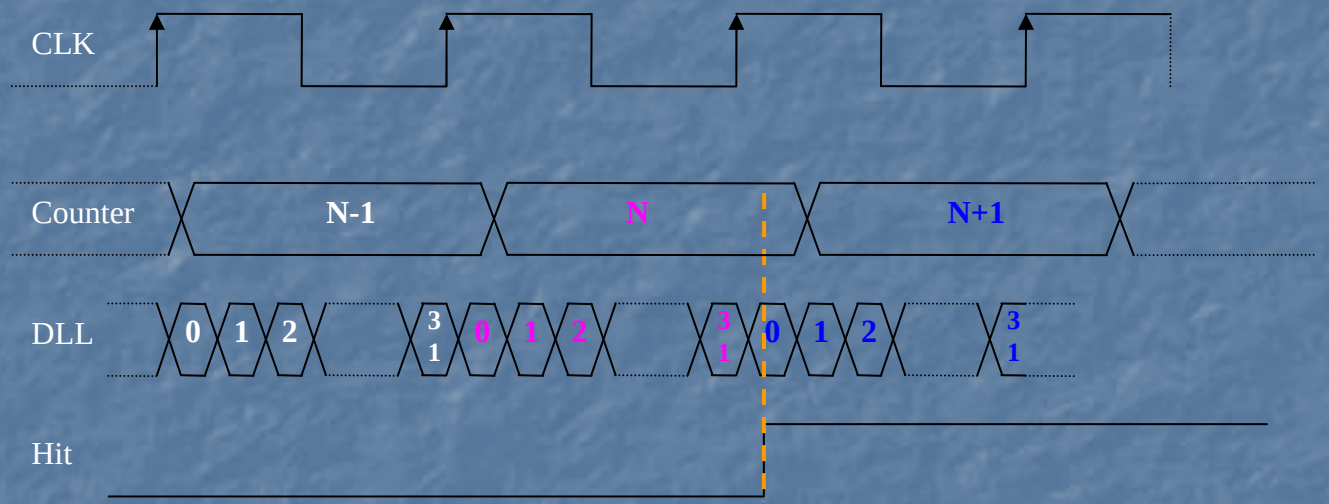
Temperature and process variation



↳ **Phase error < 20ps**

SNATS: Fine & Coarse measurement matching

Pb : DLL and counter are synchronous but not in phase!

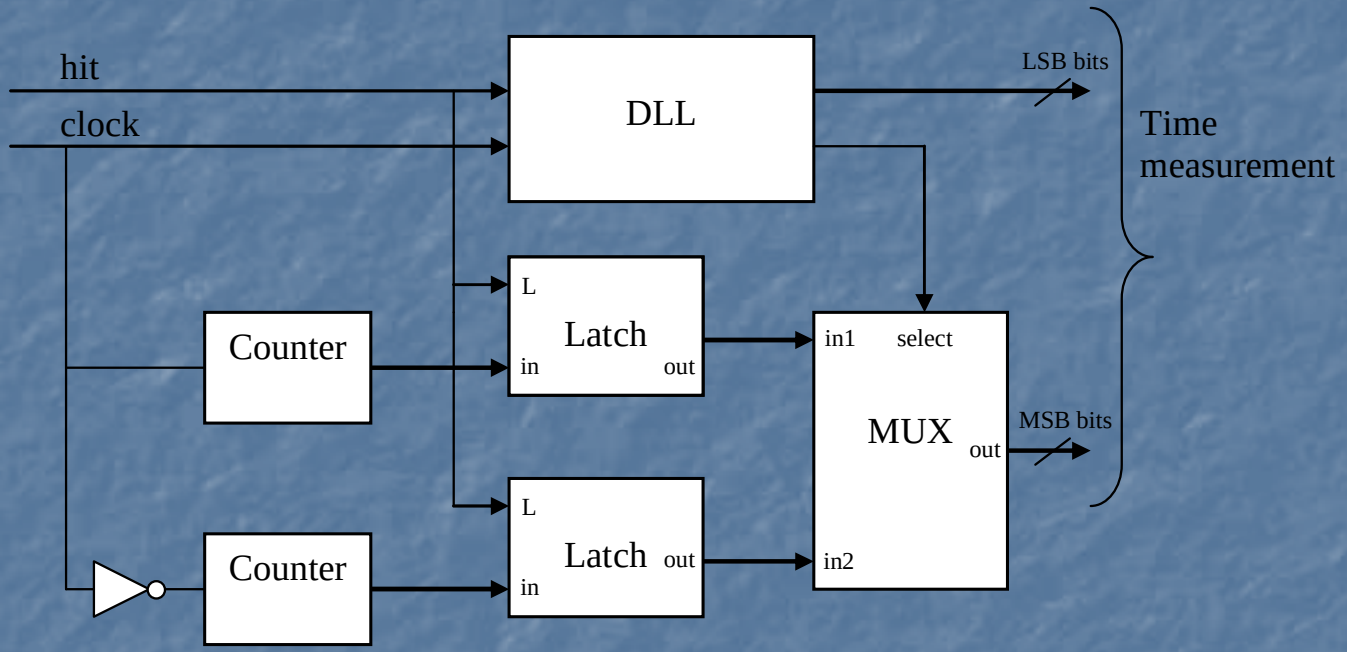


DLL code memorized : 0
Counter code memorized : N instead of N+1

} Error of one clock period

SNATS : Fine & Coarse measurement matching

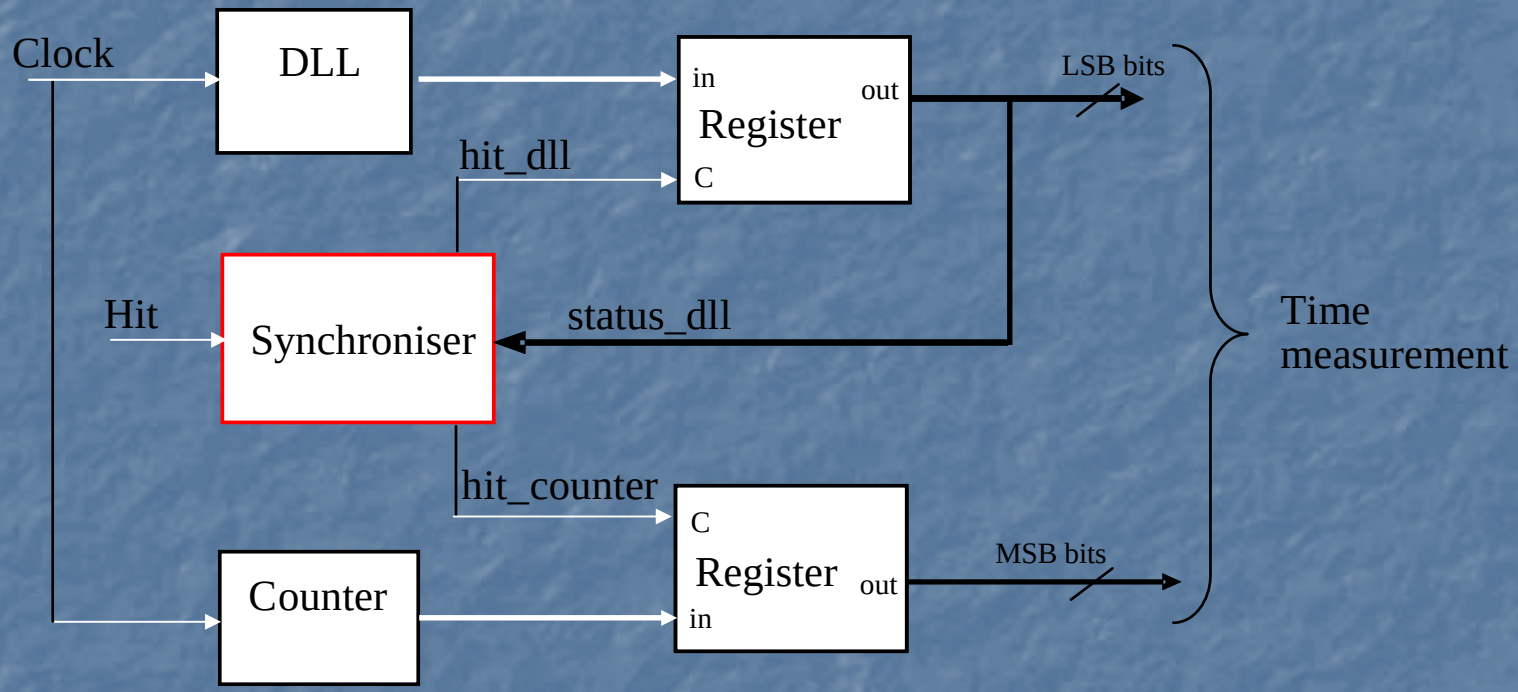
Usually, a dual counter structure is used:



Disadvantages:

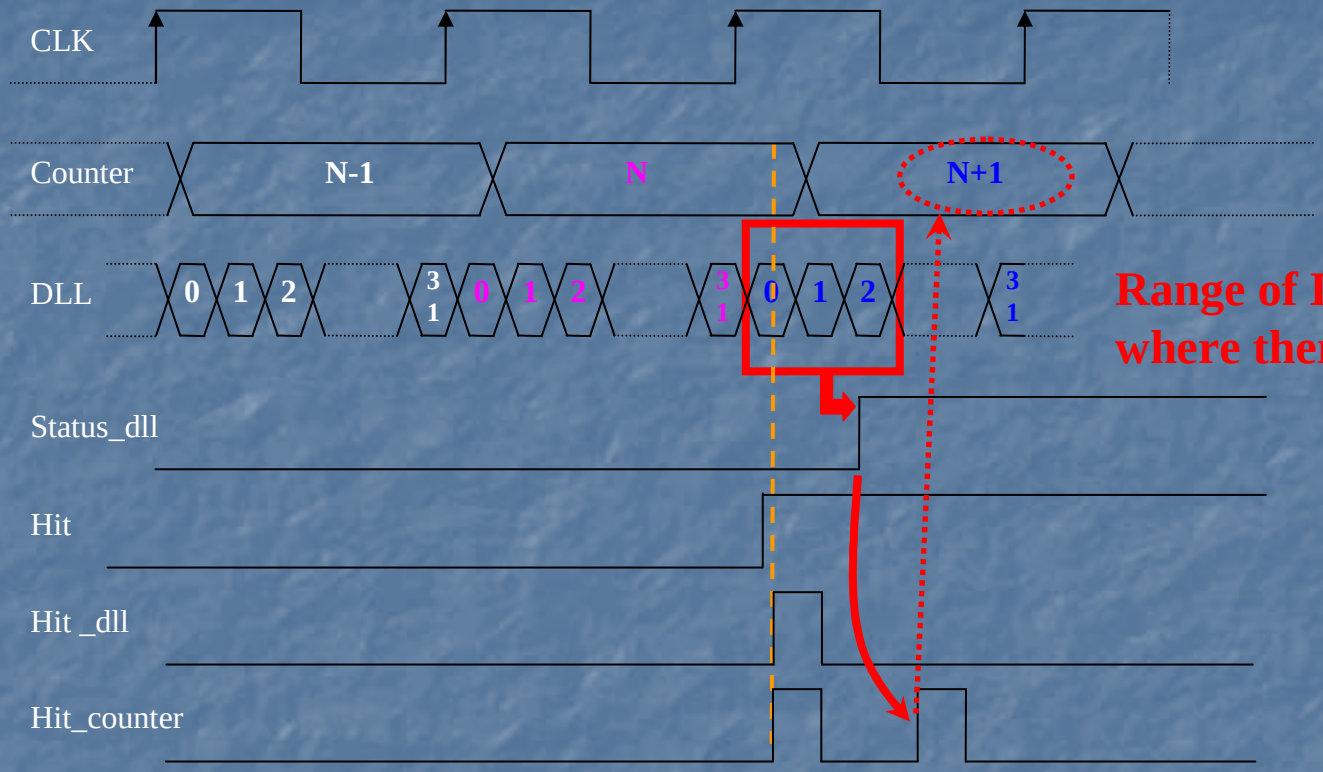
- ↗ silicon area (2 counters + multiplexer)
- ↗ power consumption

Principle: production of a 'DLL last cells' flag to delay the latching of the counter



SNATS: junction between DLL and counter

Event with correction:



Range of DLL code values where there is an ambiguity

DLL code memorized : 0
Counter code memorized in function of DLL code : N+1

Code is correct

SNATS: 48-bit GRAY counter

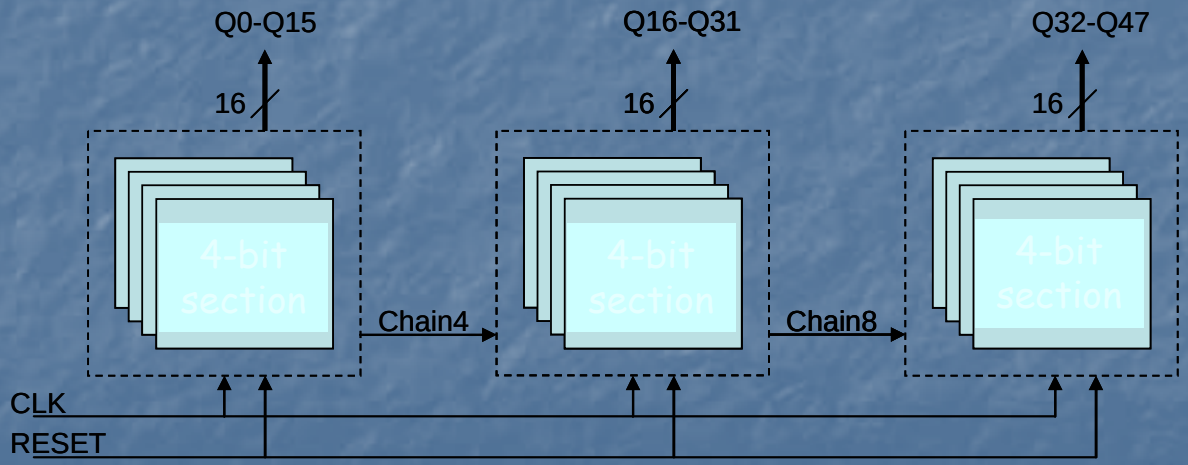
Requirements:

- Operating frequency : 160MHz
- Range : 48 bits (20 days)
- Low consumption
- No transient state

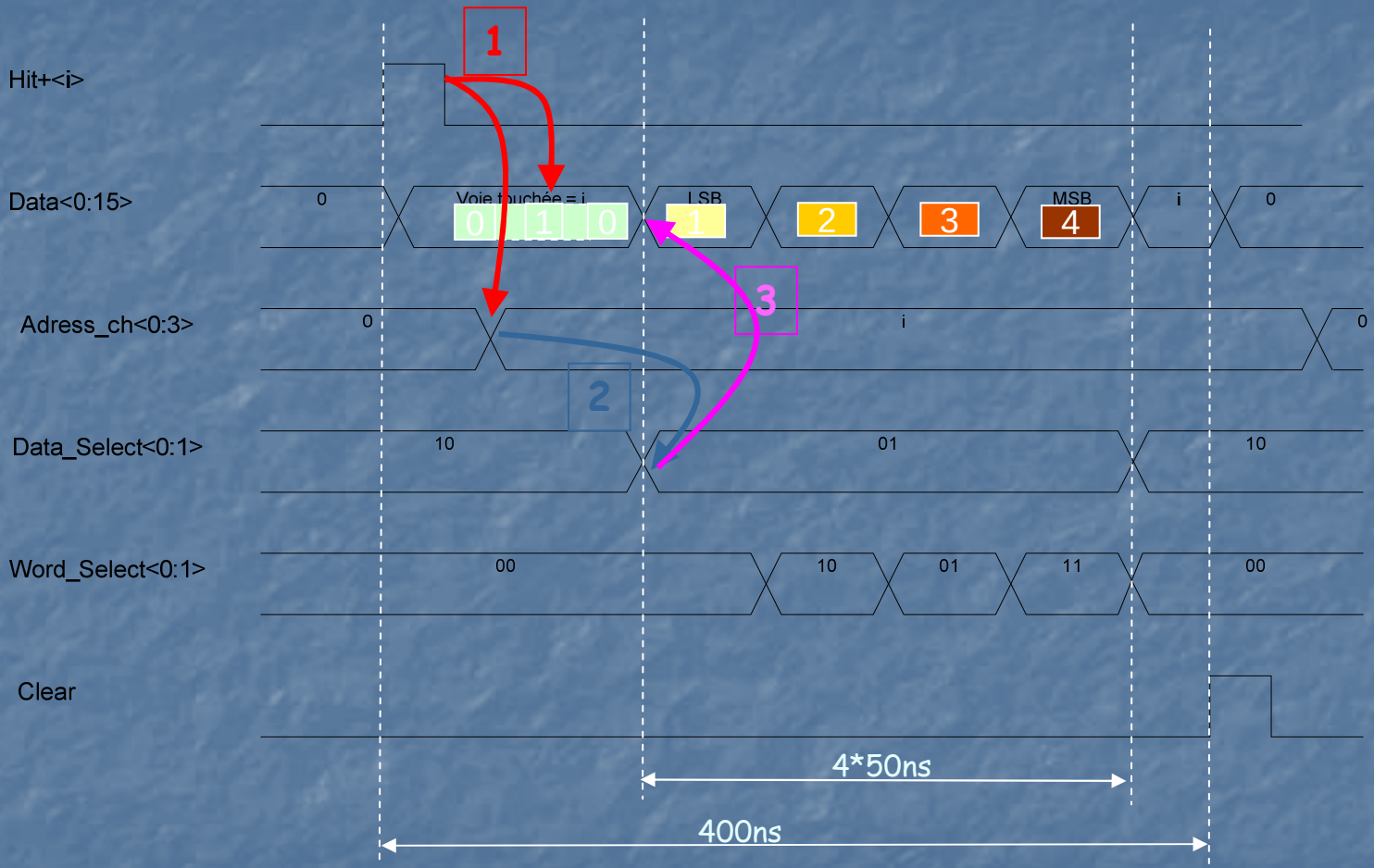
} Code Gray

Optimization between complexity / performance:

- counter made of 3 blocks of 16 bits each consisting of 4 sections of 4 bits



SNATS: readout sequence



SNATS: Electrical Characteristics

Consumption:

- 3.3V supply
- 10mA/DLL + 35mA for the rest
- For 8 DLLs: 115 mA ⇨ P= 380 mW

Clock signal:

- LVDS or single input
- Frequency: 160MHz
- Low jitter: a few ps RMS

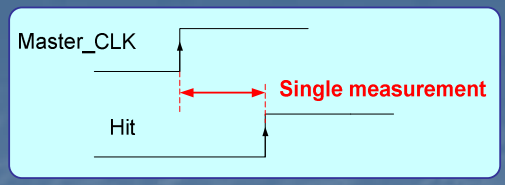
Hit signal :

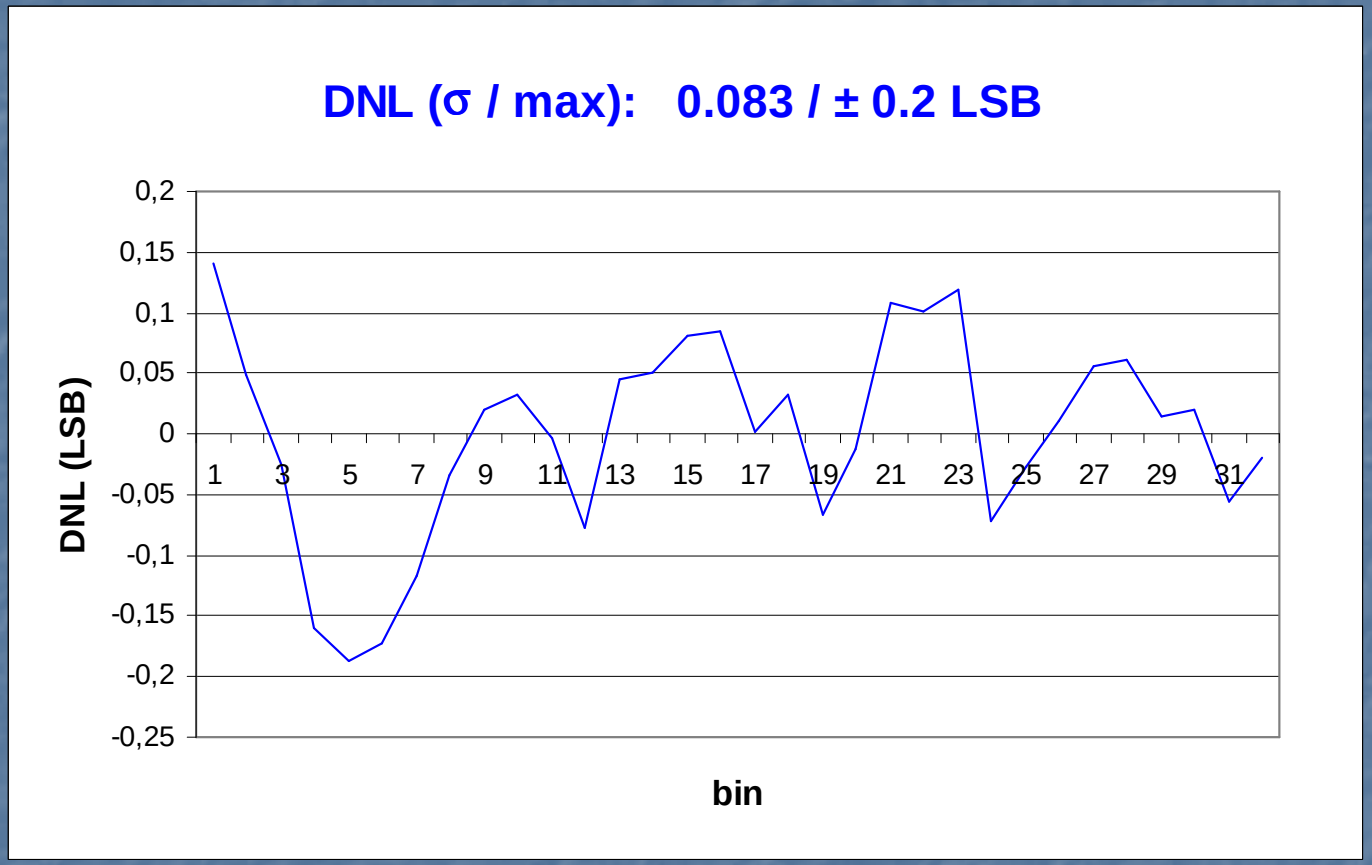
- Input level between 1V and 3.3V
- Trigger on rising edge

Readout and control signals:

- 3.3V CMOS Standard

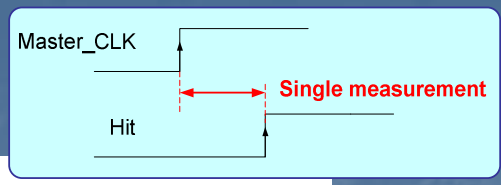
Differential Non Linearity (DNL):

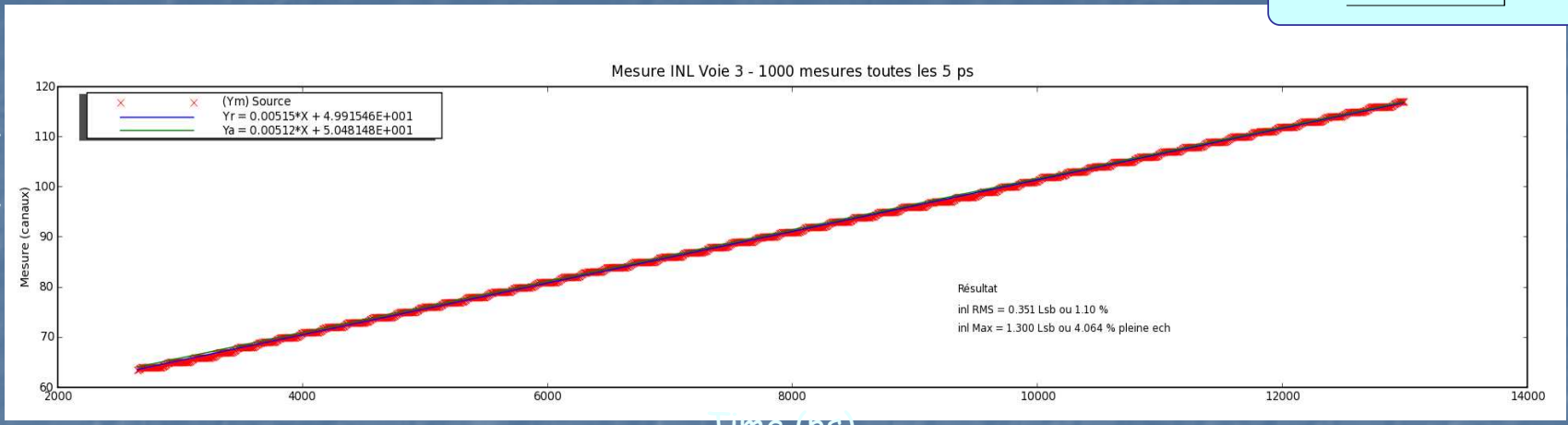




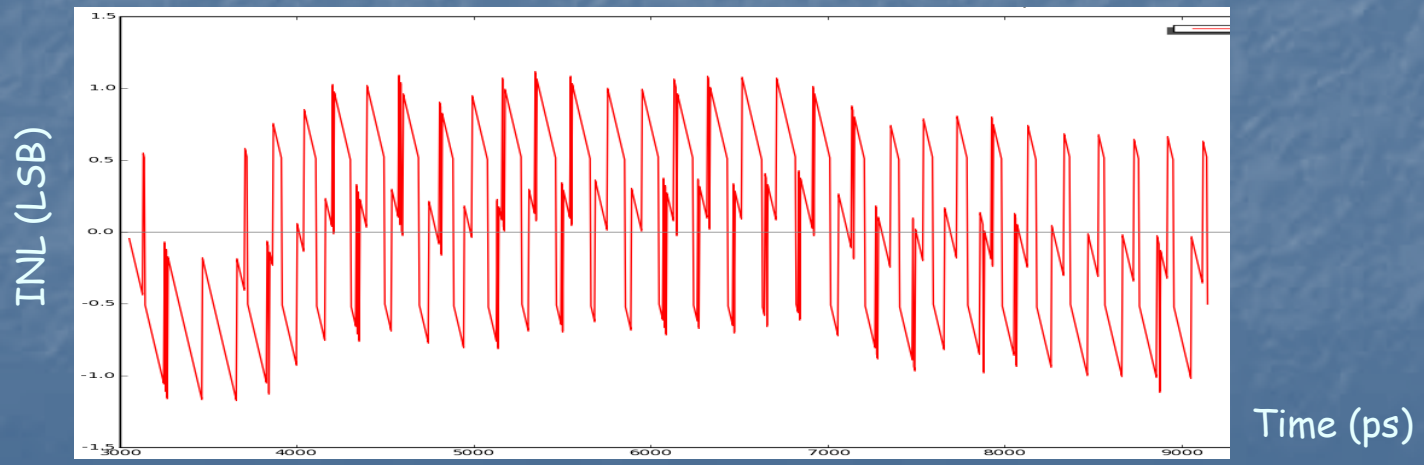
Single channel measurement

Transfer function:



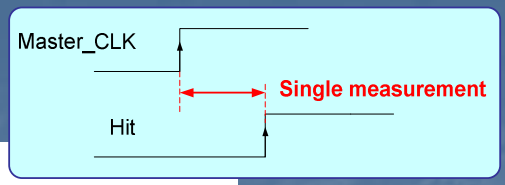


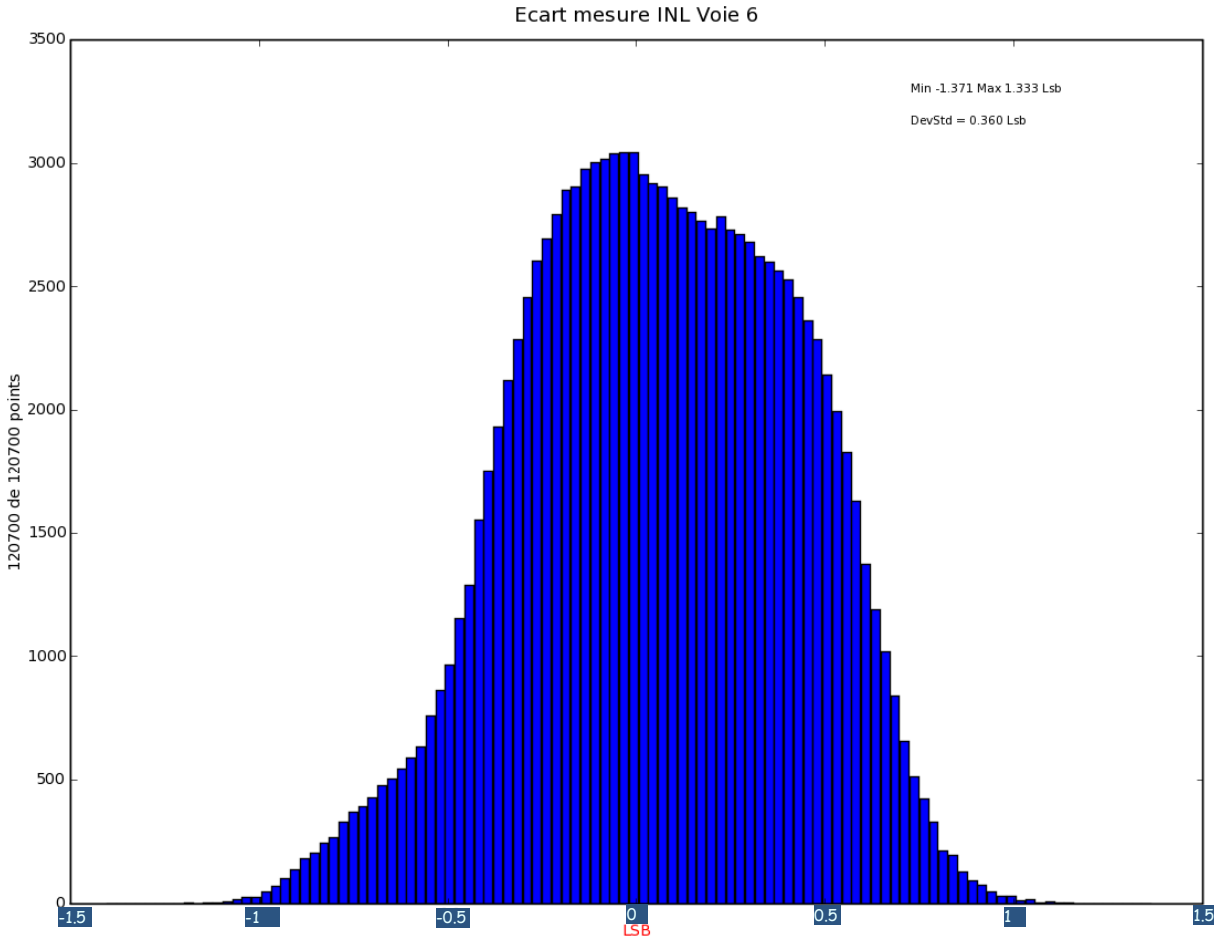
Integral Non Linearity (σ / max): 0.36 / ± 1.3 LSB



Single channel measurement

Resolution: σ = 71 ps





SNATS: conclusion

Timing characteristics:

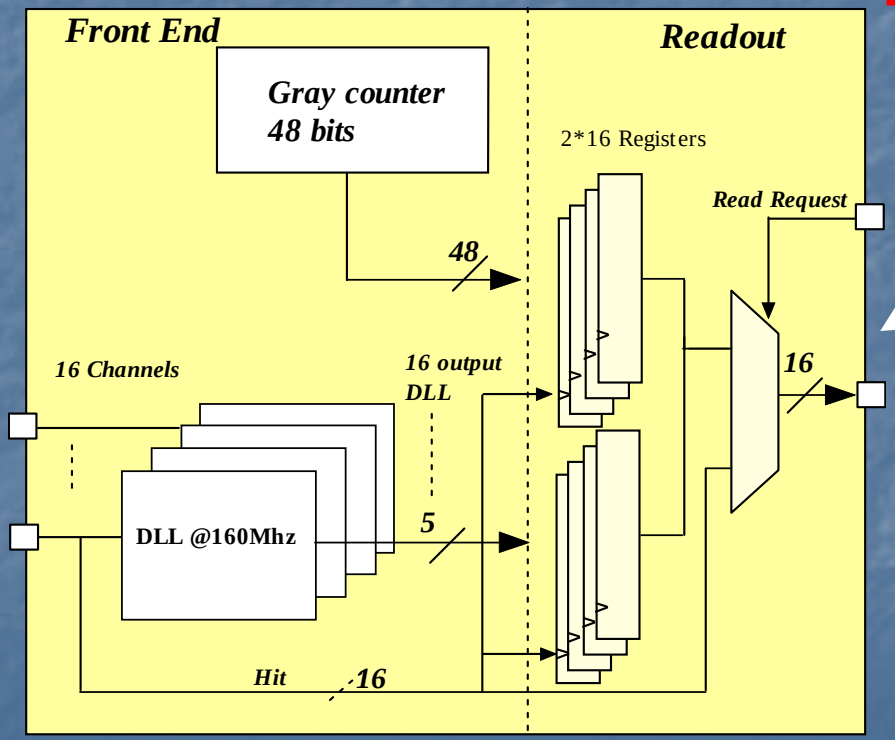
Bin size (LSB)	195.3ps	
Clock frequency	160 MHz	⇨ **Dynamic range** ~20 days
	Single pulse mode	**Dual pulse mode**
Resolution	70ps RMS	101ps RMS
DNL (σ / max)	0.083 / ± 0.2 LSB	0.024 / ± 0.08 LSB
INL (σ / max)	0.36 / ± 1.3 LSB	0.514 / ± 1.8 LSB
Crosstalk	< ±1 bin (layout mistake)	

DNL for single pulse mode is high and must be corrected
↳next submission in 2010

Stake: high count rate detectors

- INL, DNL, resolution … : same requirements.
- Increase the input data rate up to the Mhz level per chip.
  - SNATS: 2.5MHz per channel but ~150 kHz per chip

Need to reduce dead time due to readout protocol between ASIC and PGA = 50 ns per 16 bit word

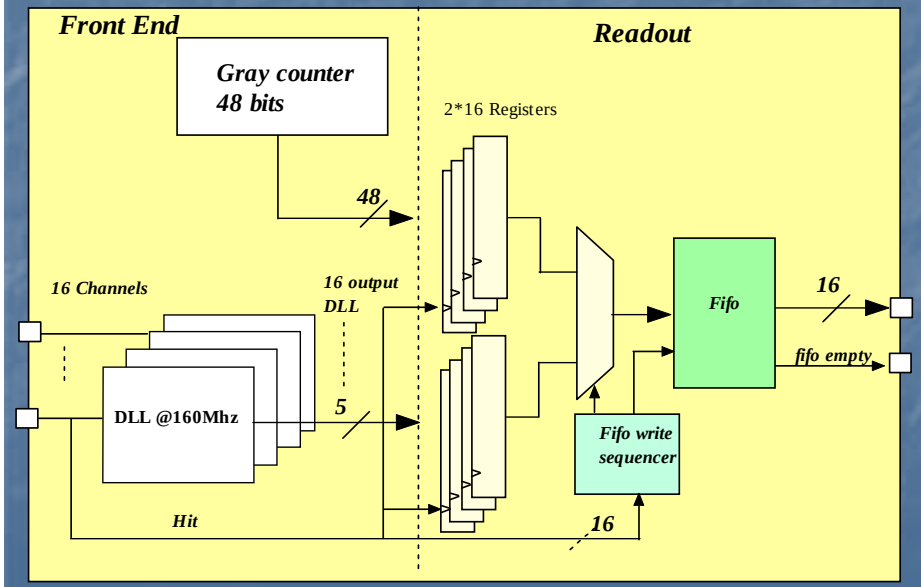


SNATS: Evolution & Perspectives

2 options (among many others …)

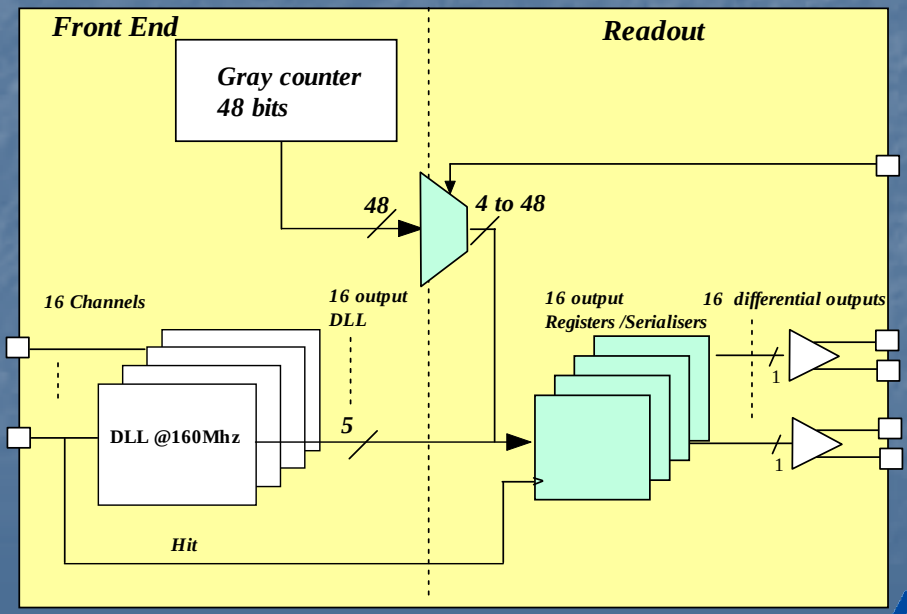
- Keeping almost the same design and just adding a FIFO at the output.
  - ➪ it increases the input channel rate in burst mode but keeps the average readout rate like the previous version.
  - ➪ The FIFO size is costly.

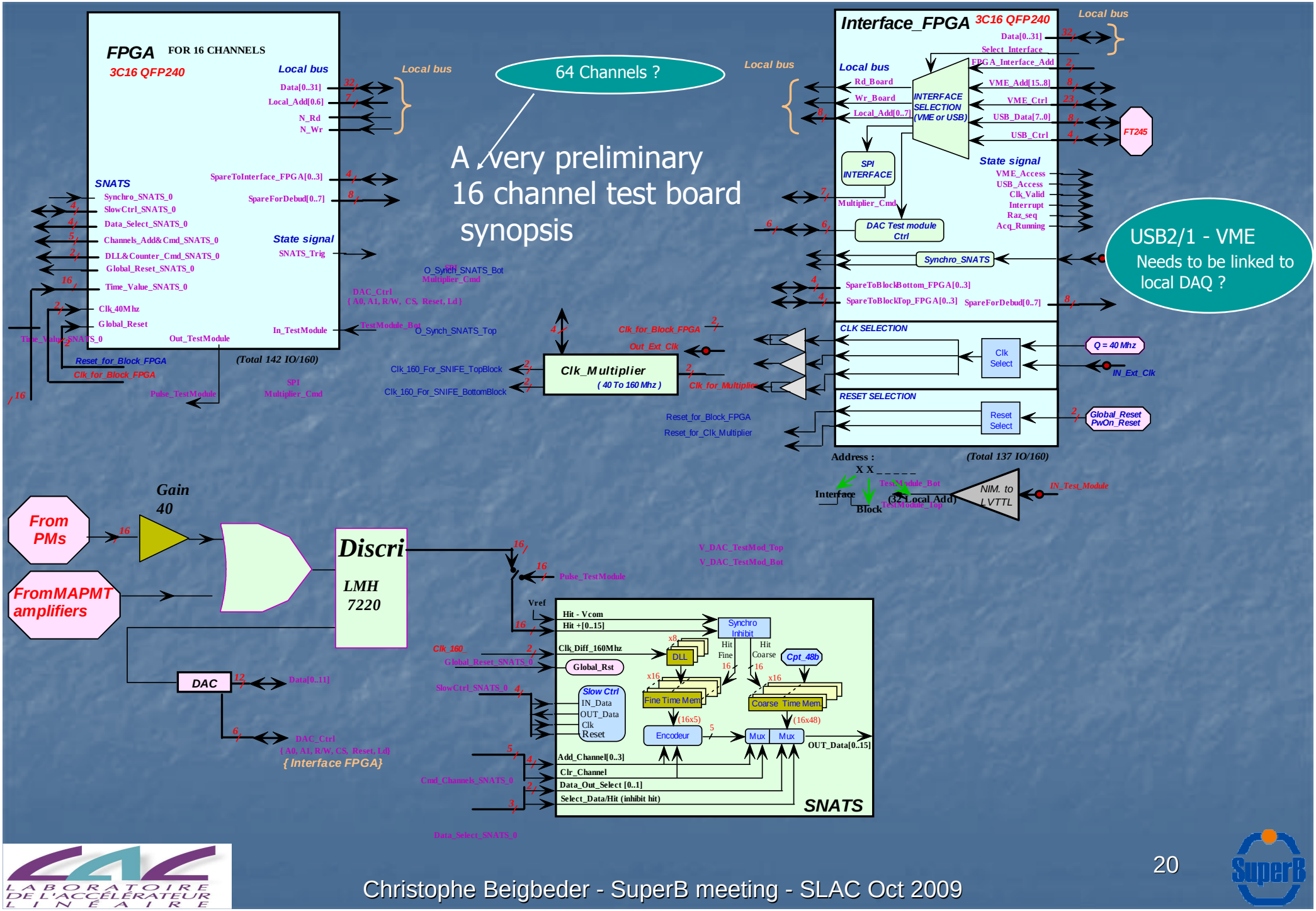
- Max performance :
  - ➢ Mhz/channel in burst mode but limited by the size of the FIFO.



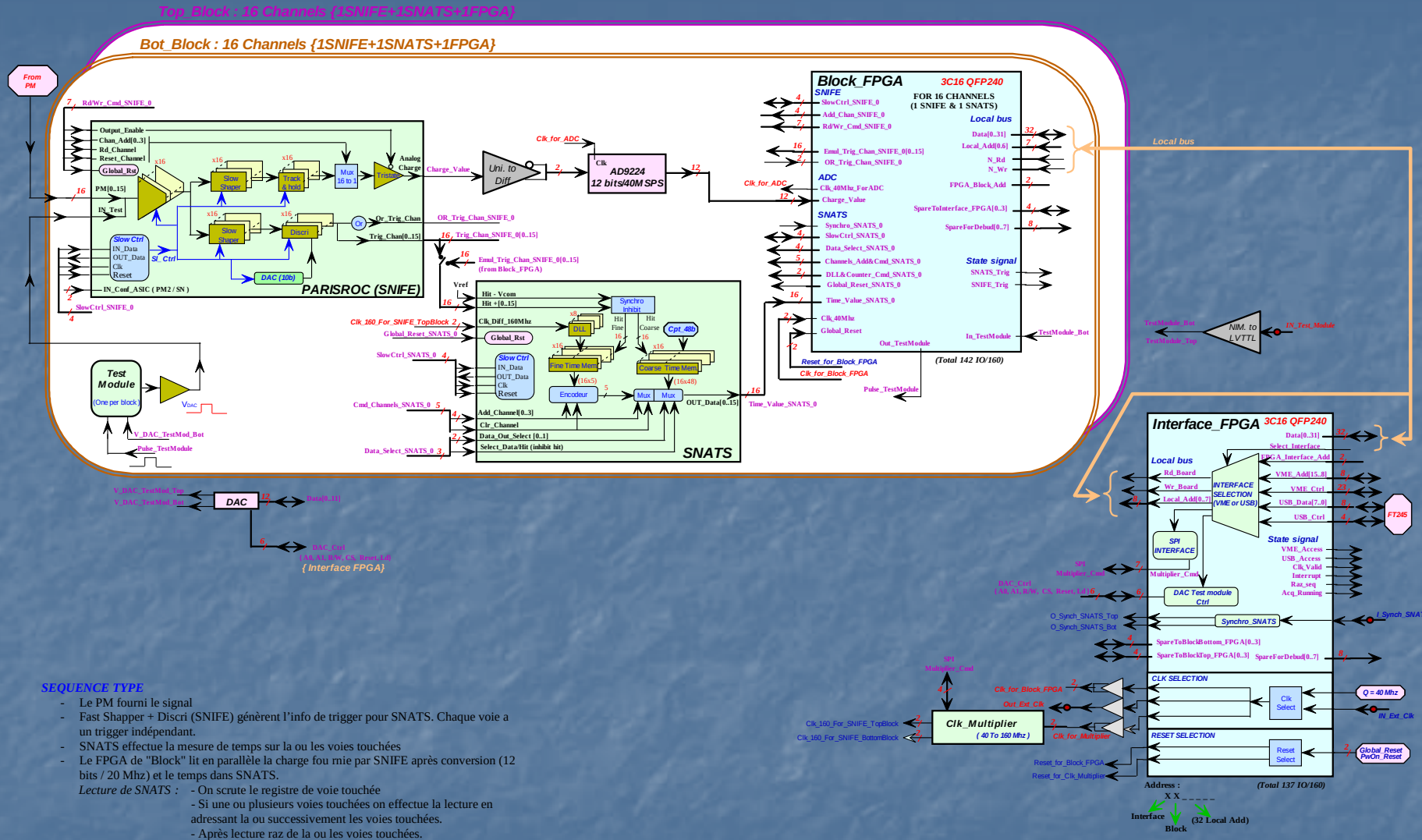
- Keeping the Gray counter inside the ASIC with an output bus width set by user in order to reduce the amount of data to be transferred. The Gray counter is duplicated inside the associated PGA.
  - ➪ The serial output is synchronous to the clock to ensure the matching between the 2 counters.
  - ➪ 16 differential output channels @ 80 Mhz (160MHz?).

- Max performance
  - ➢ 5 DLL bits + 4 Gray bits + start bit = 10b @ 80 Mhz = 8Mhz input rate !
  - ➢ Linked to performance of the readout acquisition




FPGA FOR 16 CHANNELS
3C16 QFP240
Local bus
Data[0..31]
Local_Add[0.6]
N_Rd
N_Wr
SNATS
Synchro_SNATS_0
SlowCtrl_SNATS_0
Data_Select_SNATS_0
Channels_Add&Cmd_SNATS_0
DLL&Counter_Cmd_SNATS_0
Global_Reset_SNATS_0
Time_Value_SNATS_0
Clk_40Mhz
Global_Reset
Out_TestModule
In_TestModule
SpareToInterface_FPGA[0..3]
SpareForDebud[0..7]
State signal
SNATS_Trig
(Total 142 IO/160)
Reset_for_Block_FPGA
Clk_for_Block_FPGA
Pulse_TestModule
SPI Multiplier_Cmd
64 Channels ?
A very preliminary 16 channel test board synopsis
Interface_FPGA 3C16 QFP240
Local bus
Rd_Board
Wr_Board
Local_Add[0..7]
INTERFACE SELECTION (VME or USB)
SPI INTERFACE
Multiplier_Cmd
DAC Test module Ctrl
FPGA_Interface_Add
VME_Add[15..8]
VME_Ctrl
USB_Data[7..0]
USB_Ctrl
FT245
State signal
VME_Access
USB_Access
Clk_Valid
Interrupt
Raz_seq
Acq_Running
Synchro_SNATS
SpareToBlockBottom_FPGA[0..3]
SpareToBlockTop_FPGA[0..3]
SpareForDebud[0..7]
CLK SELECTION
Clk Select
Q = 40 Mhz
IN_Ext_Clk
RESET SELECTION
Reset Select
Global_Reset PwOn_Reset
(Total 137 IO/160)
Address : X X _ _ _ _ _
Interface Block
(32 Local Add)
NIM. to LVTTL
IN_Test_Module
USB2/1 - VME
Needs to be linked to local DAQ ?
DAC_Ctrl { A0, A1, R/W, CS, Reset, Ld }
O_Synch_SNATS_Bot
O_Synch_SNATS_Top
TestModule_Bot
Multiplier_Cmd
Clk_160_For_SNIFE_TopBlock
Clk_160_For_SNIFE_BottomBlock
Clk_Multiplier (40 To 160 Mhz)
Clk_for_Block_FPGA
Out_Ext_Clk
Clk_for_Multiplier
Reset_for_Block_FPGA
Reset_for_Clk_Multiplier
Gain 40
From PMs
FromMAPMT amplifiers
Discri LMH 7220
DAC
Data[0..11]
DAC_Ctrl { A0, A1, R/W, CS, Reset, Ld }
{ Interface FPGA }
V_DAC_TestMod_Top
V_DAC_TestMod_Bot
Pulse_TestModule
Vref
Hit - Vcom
Hit +[0..15]
Clk_Diff_160Mhz
Clk_160
Global_Reset_SNATS_0
Global_Rst
SlowCtrl_SNATS_0
Slow Ctrl
IN_Data
OUT_Data
Clk
Reset
Synchro Inhibit
DLL
Hit Fine
Hit Coarse
Cpt_48b
Fine Time Mem
Coarse Time Mem
(16x5)
(16x48)
Encodeur
Mux
Mux
OUT_Data[0..15]
Add_Channel[0..3]
Clr_Channel
Data_Out_Select [0..1]
Select_Data/Hit (inhibit hit)
Cmd_Channels_SNATS_0
Data_Select_SNATS_0
SNATS

The SuperNemo test board



SEQUENCE TYPE

- Le PM fourni le signal
- Fast Shapper + Discri (SNIFE) génèrent l'info de trigger pour SNATS. Chaque voie a un trigger indépendant.
- SNATS effectue la mesure de temps sur la ou les voies touchées
- Le FPGA de "Block" lit en parallèle la charge fou rnie par SNIFE après conversion (12 bits / 20 Mhz) et le temps dans SNATS.

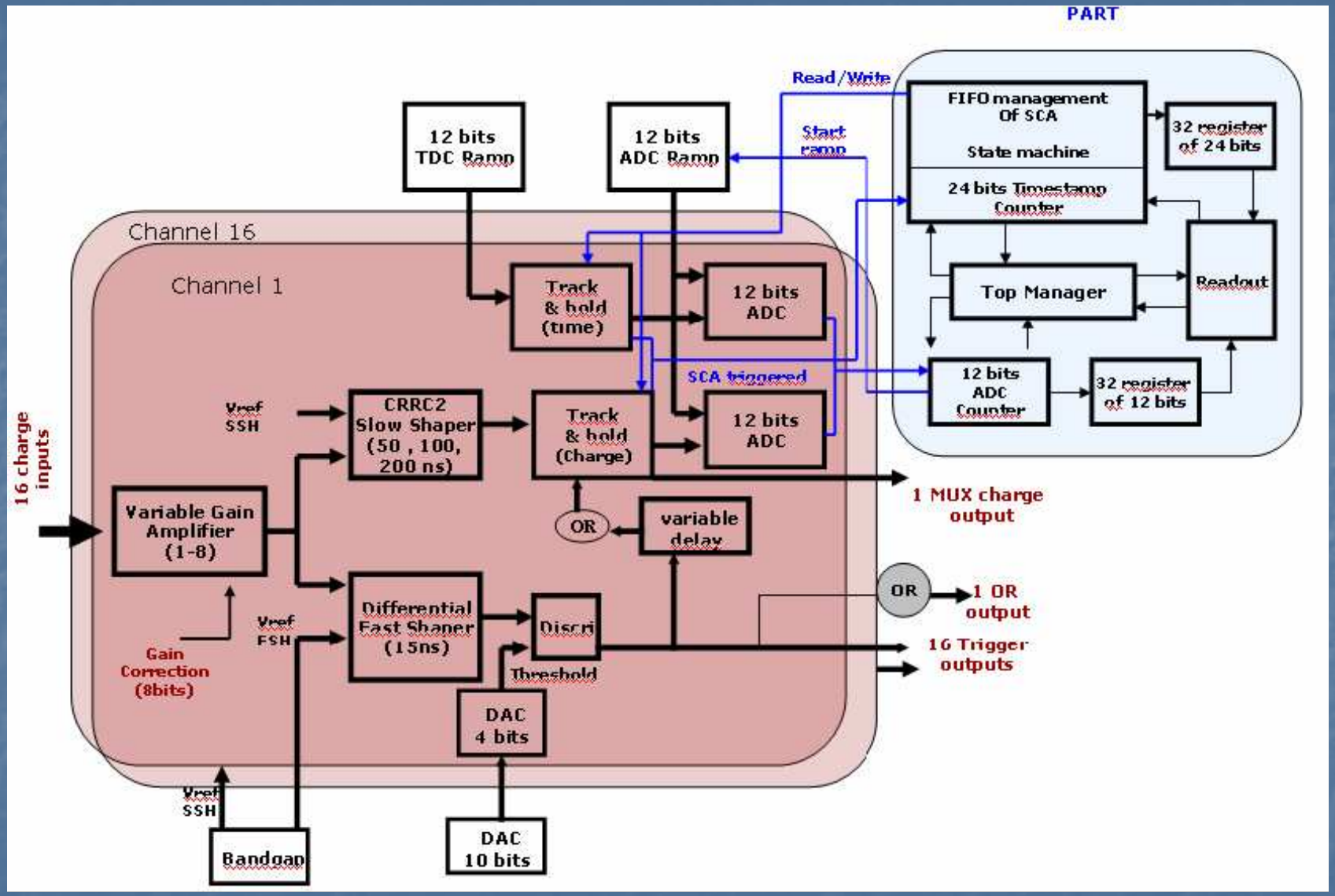
Lecture de SNATS :
- On scrute le registre de voie touchée
- Si une ou plusieurs voies touchées on effectue la lecture en adressant la ou successivement les voies touchées.
- Après lecture raz de la ou les voies touchées.

Lecture de SNIFE :
- L'info de voie touchée est obtenu par lecture de SNATS
- On effectue la lecture en adressant la ou successivement les voies touchées.
- Après lecture raz de la ou les voies touchées

SN_FEB ARCHITECTURE

January 06, 2009

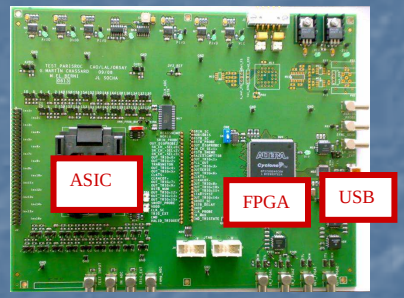
Parisroc front-end ASIC developed @ LAL.

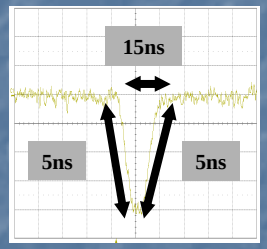


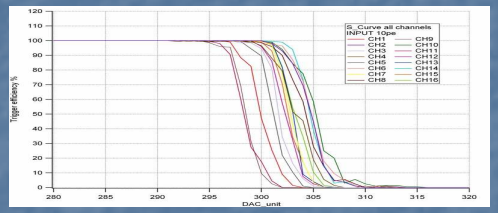
All the measurements are done with an input signal produced by a generator, as shown in fig. 6, simulating a PM tube signal. The voltage goes from 0 to 250mV to represent a charge up to 50pC for a PM tube gain taken at 10^6.

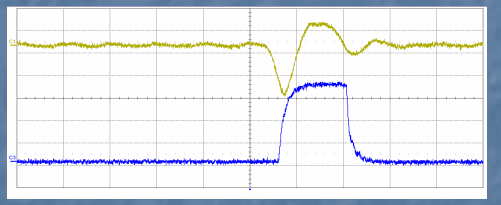
1.Trigger measurements

Noise at the output of the fast shaper is 2.5mV RMS (equivalent to 0.08 p.e.).
One photo-electron signal gives 30mV at the fast shaper output with a rise time of 7ns as shown in fig. 7.









The trigger efficiency versus threshold with an injected charge of 10 photo-electron for all channels is given in the S-curves of fig.8.
The spread of these curves is less than 7 LSB, equivalent to 15mV or 0.5 photo-electron as the LSB of the DAC is 2mV (0.07pe). The noise, given by the slope of the curve, is less than 0.1 photo-electron.
The time walk is about 4 ns

Summary

1. TDC: the current TDC seems to be OK for the barrel except its trigger rate capability
   -> do we go on designing a TDC for the barrel based on the 100-ps SNATS chip with the evolution we propose. We need a clear green light to start the study and involve people as soon as possible in the collaboration.

2 The Parisroc front-end ASIC is not adapted to our requirements. We need to develop a specific ASIC to shape the PM signals and generate a trigger without " walk " and with or without output shaper for the charge measurement. We have to find new collaborators on that item. Paris 6 has been contacted …

3 Do we plan to use the test board in the current version ? Can we learn something with it or do we want to develop a specific version ?