CMOS MAPS: Design Challenges and State of the Art

Lucio Pancheri

Department of Industrial Engineering, University of Trento
TIFPA – INFN, Trento

Cogne, 12- 16 February 2018

Research on silicon detectors in Trento

Clean room

FBK

UniTN
Dept. Physics

INFN-TIFPA

SP204

UniTN
Dept. Industrial
Engineering

Via dei Valo

Proton therapy

TIFPA

UniTN

FBK

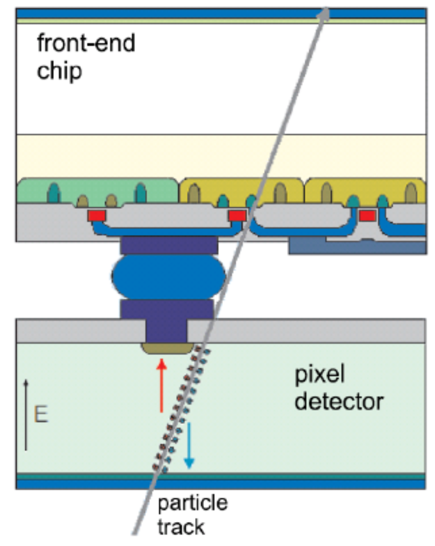
Povo-Pantè

Gionghi

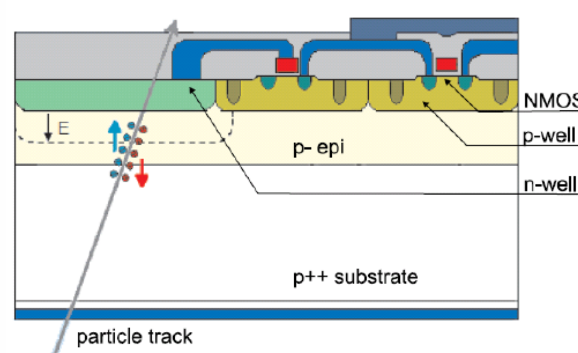
© 2016 Google

Pixel detectors for tracking in HEP

- **Hybrid Pixel Sensors**
  - Adopted in major experiments at LHC (ATLAS, CMS, ALICE)
  - Detectors and electronics are developed and optimized separatly
  - Excellent radiation damage tolerance



- **Monolithic Active Pixel Sensors (MAPS)**
  - Detectors and electronics fabricated on the same substrate
  - Emerging, still not widespread in HEP



L. Gonella, Particle Physics Seminar, 2017

MAPS development - motivation

- Adoption of MAPS in HEP applications:
  - Higher spatial resolutions
  - Lower material budget
  - Cost
- Synergies outside HEP tracking applications:
  - X-ray imaging
  - IR imaging
  - Medical imaging with particles
  - Space

Outline

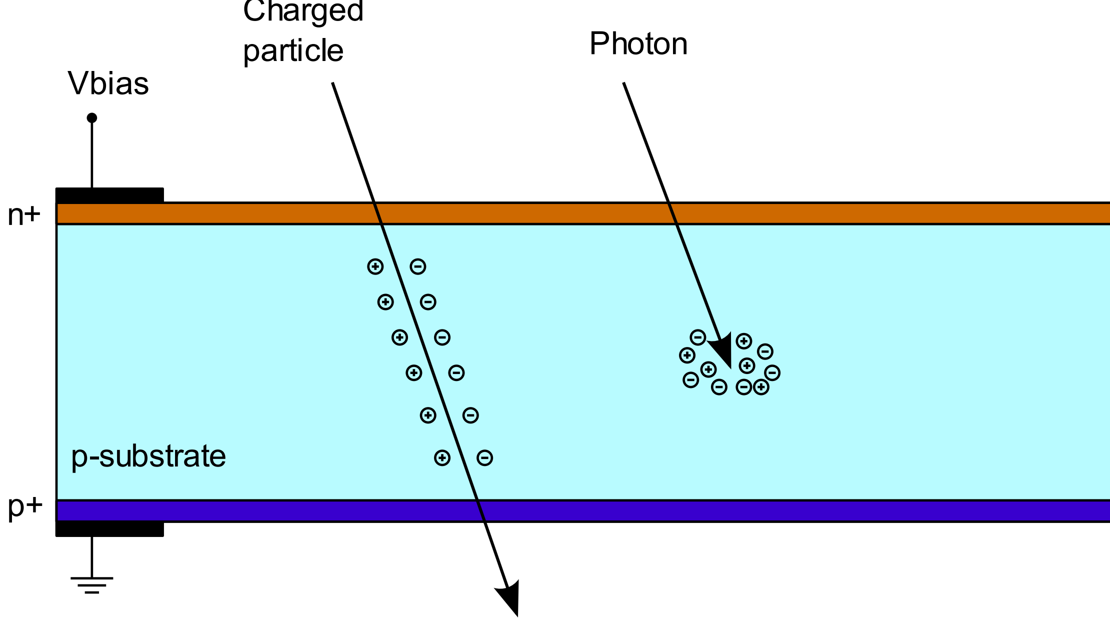
- Radiation detection in silicon
- CMOS technologies: characteristics, opportunities and challenges
- Monolithic active pixels for photon imaging
- MAPS: design approaches and research directions
- SEED project overview

Outline

- Radiation detection in silicon
- CMOS technologies: characteristics, opportunities and challenges
- Monolithic active pixels for photon imaging
- MAPS: design approaches and research directions
- SEED project overview

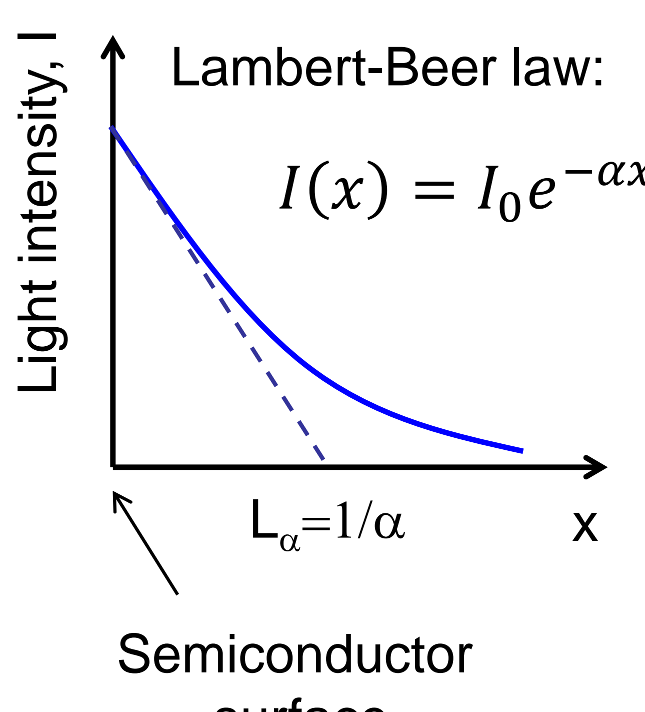
Radiation signal detection

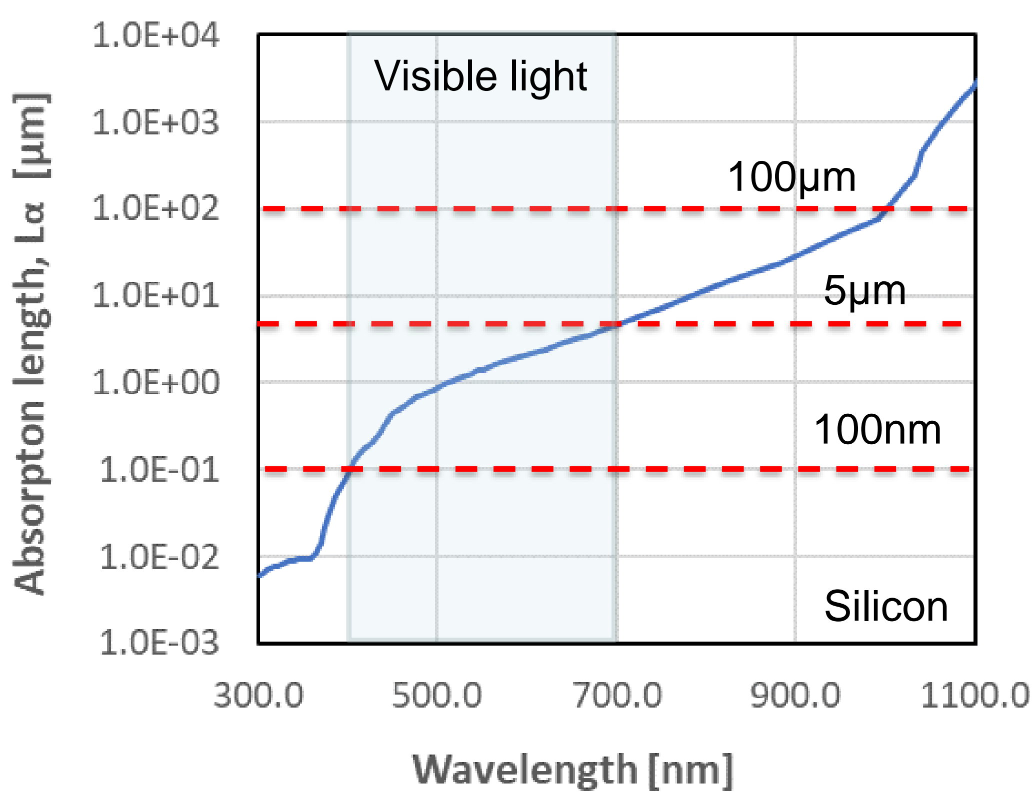
- Charge generation
- Charge collection
- Amplificaton – analogue processing (shaping)
- Recording (Signal Amplitude, Thresholding, Time of arrival, Signal Width)



Photons: absorption length

NUV – Visible – NIR light: 1 e-h pair per photon





X-rays

EUV, X-rays: "Point-like" interaction with the production of many e-h pairs in a small region, a few μm wide.

Average number of e-h pairs:

$$n_{e-h} = \frac{E_{ph}}{E_{ion}}$$

Si ionization energy

E_{ion}=3.6eV

100μm

100nm

Absorption Length (μm)

1000
100
10
1.0
0.1
0.01
0.001

Soft X-ray

Extreme Ultraviolet

Far (or vacuum) Ultraviolet

Near UV, Visible, Near IR

0.1 1.0 10 100 1000

Wavelength (nm)

10,000 1000 100 10 1.0

Photon Energy (eV)

280e-

www.ll.mit.edu

Charged particles: ionization energy loss in Si

100
10
1
dE/dx [MeV−cm2/g]
10^0 10^1 10^2 10^3 10^4 10^5 10^6
energy [MeV]

Charged pion in Silicon

Minimum Ionizing Particle (MIP)

G.Lutz, Semiconductor Radiation detectors, Springer, 1999

Energy loss distribution in silicon

500 MeV pion in silicon

640 μm (149 mg/cm^2)

320 μm (74.7 mg/cm^2)

160 μm (37.4 mg/cm^2)

80 μm (18.7 mg/cm^2)

$f(\Delta/x)$

1.0
0.8
0.6
0.4
0.2
0.0

Δ_p/x

Mean energy loss rate

100 200 300 400 500 600

Δ/x (eV/μm)

Landau distribution

S.Terzo, PhD thesis, MPI, 2015

Generated electrons vs. thickness

MPV [e/µm]

85
80
75
70
65
60

50 100 150 200 250 300 350 400

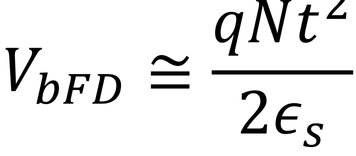
Thickness [µm]

500 MeV pion
120 GeV pion
6 GeV electron
β-electron (^{90}Sr)

S.Terzo, PhD thesis, MPI, 2015

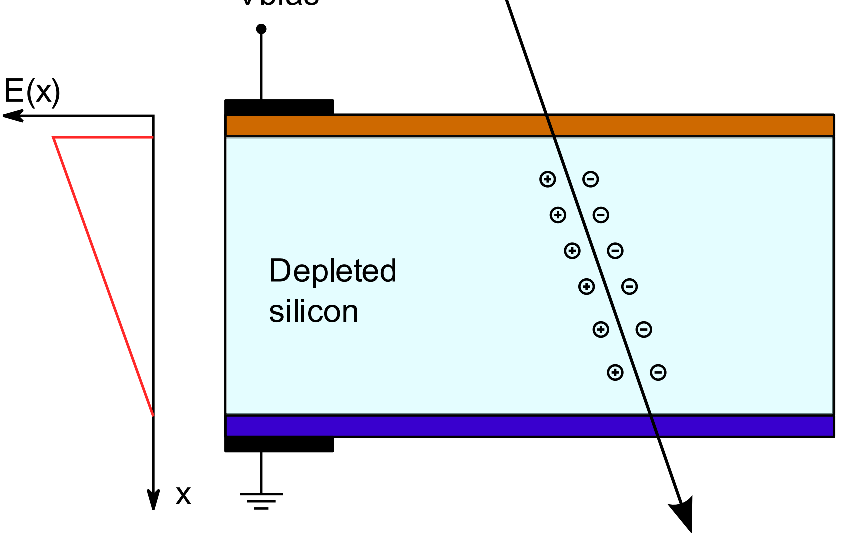
Detector bias

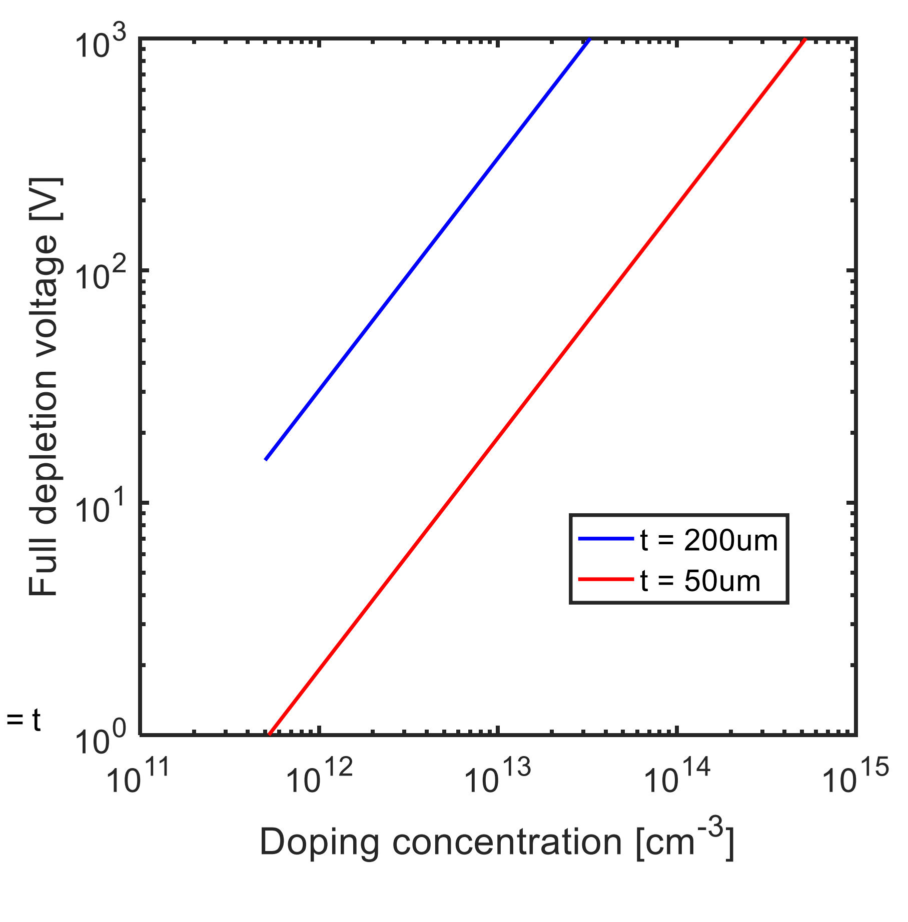
Minimum bias voltage for full depletion:



$$V_{bFD} \cong \frac{qNt^2}{2\epsilon_s}$$

N: detector doping
t: detector thickness

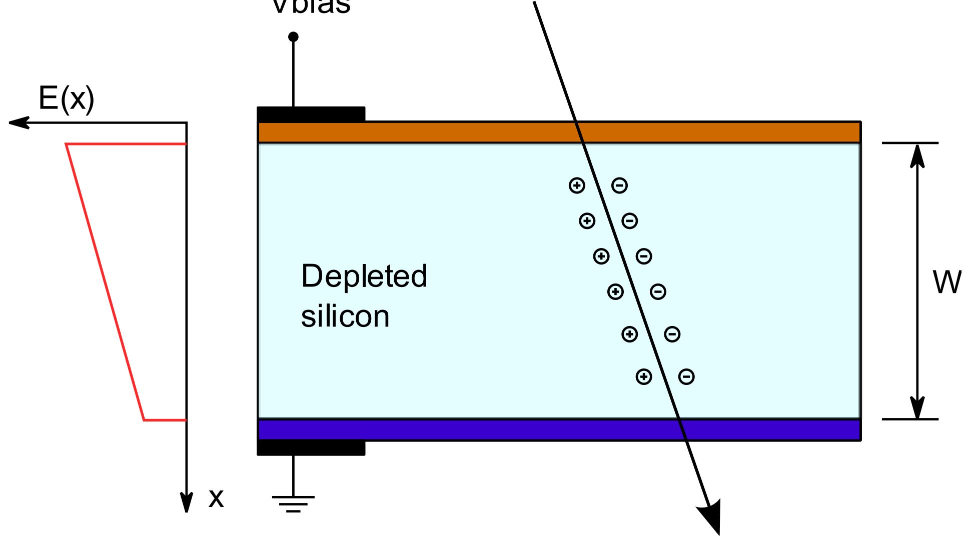


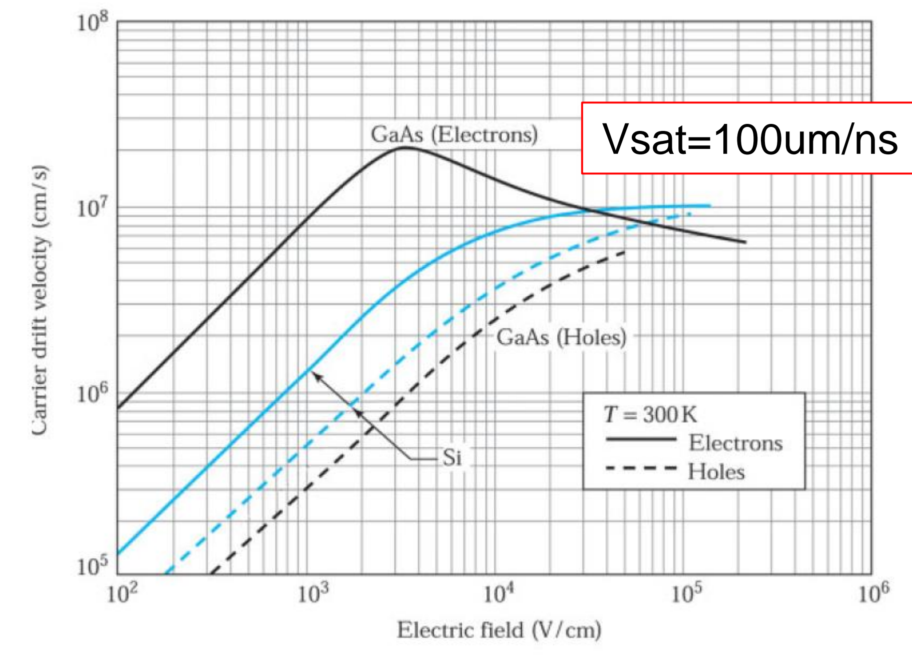


Charge collection

In a **fully depleted** detector, collection speed depends on carrier transit time in the depleted region (W)

$$t_1 = \frac{W}{v} = \frac{W^2}{\mu V_{bias}} \geq \frac{W}{v_{sat}}$$

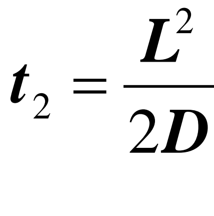




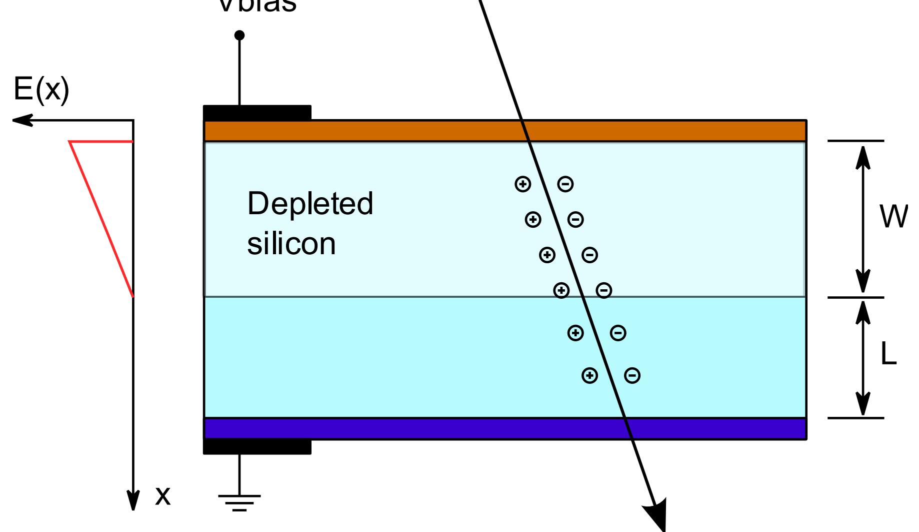
Sze, Semiconductor devices, Wiley & Sons, 2012

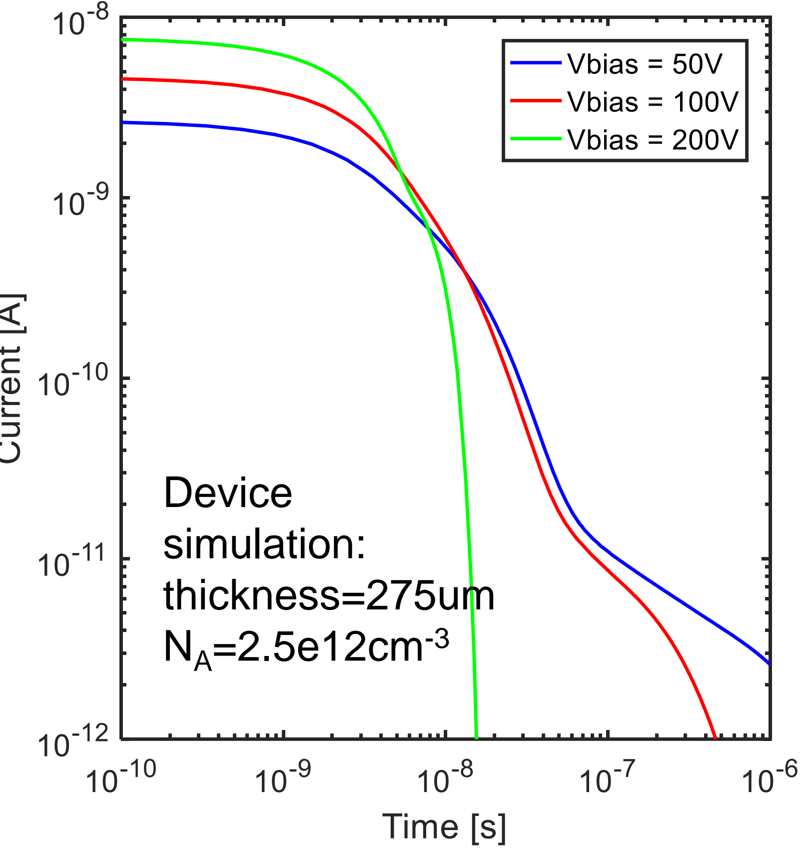
Charge collection

In a **partially depleted** detector, there is a contribution of diffusion time in the non-depleted region (L)



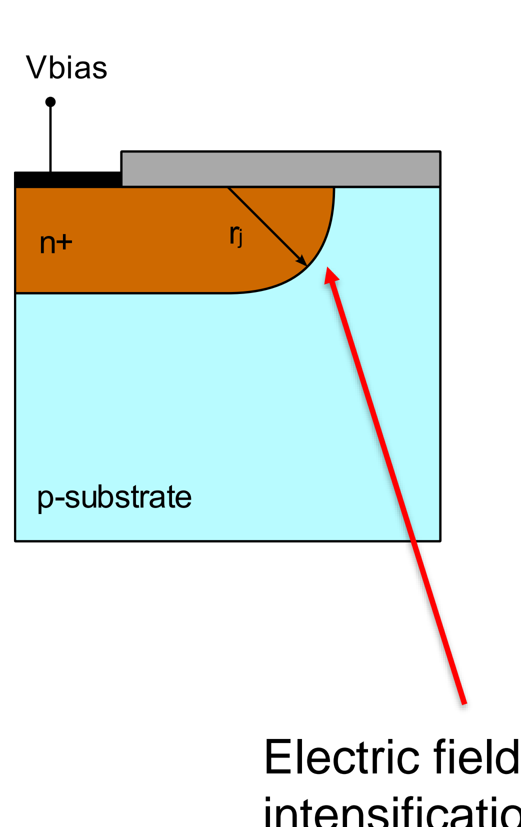
$$t_2 = \frac{L^2}{2D}$$





Detector bias

Early breakdown at the junction borders



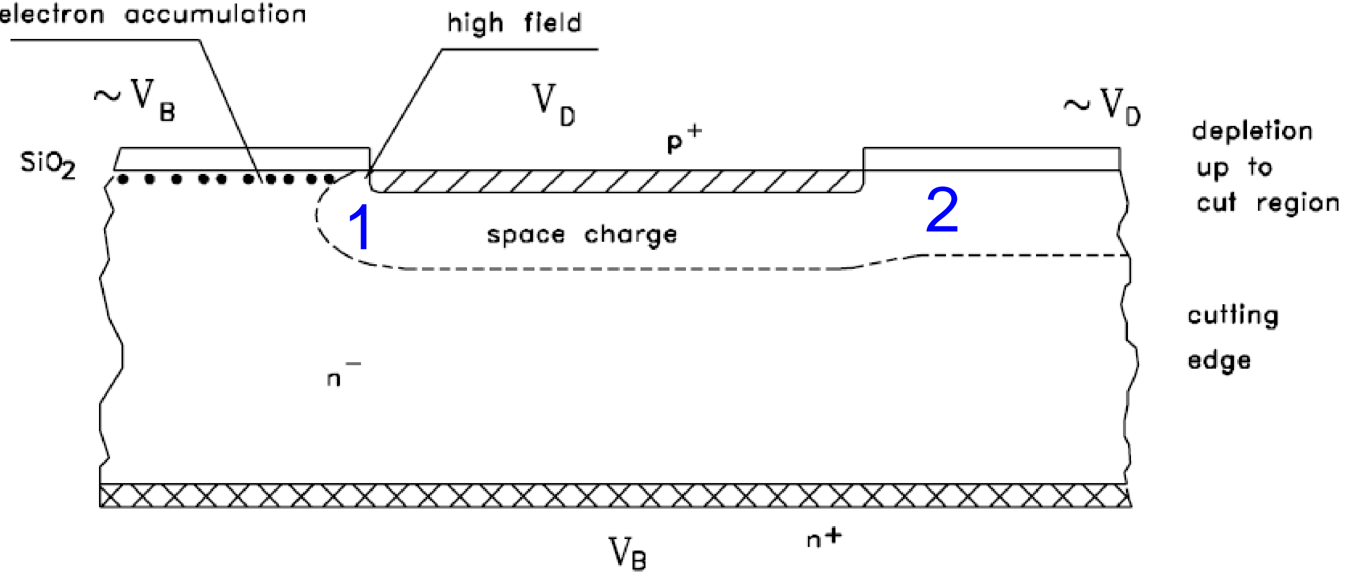
Electric field intensification

Sze and Gibbons, Solid-state Electron., 1966

Influence of interface charge

Two extreme cases depending on Si/SiO_2 interface charge (process, humidity, radiation damage, …):

1. Early Breakdown at the junction edge
2. Extension of the depleted region up to the cut line: large reverse bias due to the generation in the damaged cut region



G.Lutz, Semiconductor Radiation detectors, Springer, 1999

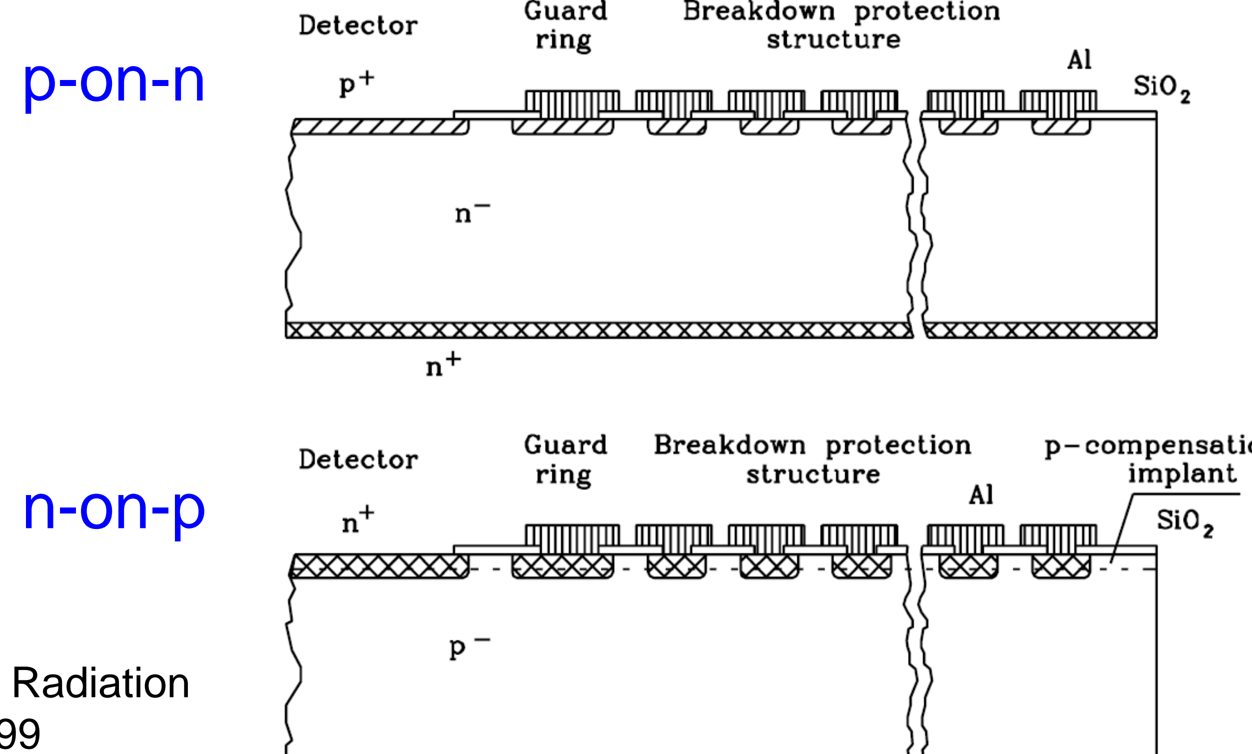
Detector bias

Handling Large Bias Voltages:

- Deep implantations or diffusion (large r_j)
- Multiple guard rings protection structures

p-on-n

n-on-p



G.Lutz, Semiconductor Radiation detectors, Springer, 1999

Readout electronics

Preamplifier:
Charge to voltage conversion
gain: $1/C_f$

A. Rivetti, CMOS Front-End Electronics for Radiations Sensors, CRC Press, 2015

Detector:
provides current signal

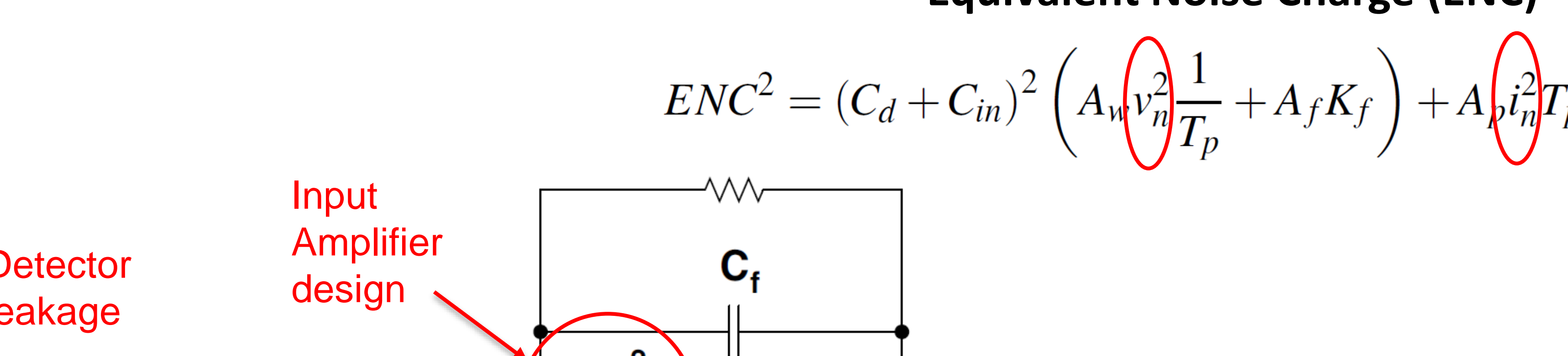
Shaper (band-pass filter):
optimized SNR
(minimizes ENC)

Requirements for low-noise

- Low **detector** and amplifier input **capacitance**
- Low detector **leakage current**
- Optimized amplifier design
- Optimized shaping filter

Total noise summarized with the **Equivalent Noise Charge (ENC)**

$$ENC^2 = (C_d + C_{in})^2 \left(A_w v_n^2 \frac{1}{T_p} + A_f K_f \right) + A_p i_n^2 T_p$$



A. Rivetti, CMOS Front-End Electronics for Radiations Sensors, CRC Press, 2015

Radiation damage in detectors

Two general types of radiation damage to the detector materials:

1) Surface damage due to Ionizing Energy Loss (IEL): accumulation of positive charge in the oxide (SiO_2) and at the Si/SiO_2 interface

2) Bulk (Crystal) damage due to Non Ionizing Energy Loss (NIEL): displacement damage, built-up of crystal defects

Surface radiation damage

- Most e-h pairs recombine
- Electrons escape, holes are much slower and finally get trapped

SiO_2:
μ_n~20cm^2/(Vs),
μ_p~2x10^{-5} cm^2/(Vs)

- Strong effects of the bias during irradiation

T.R. Oldham, Ionizing radiation effects in MOS oxides, World Scientific, 1999

Consequences for detectors

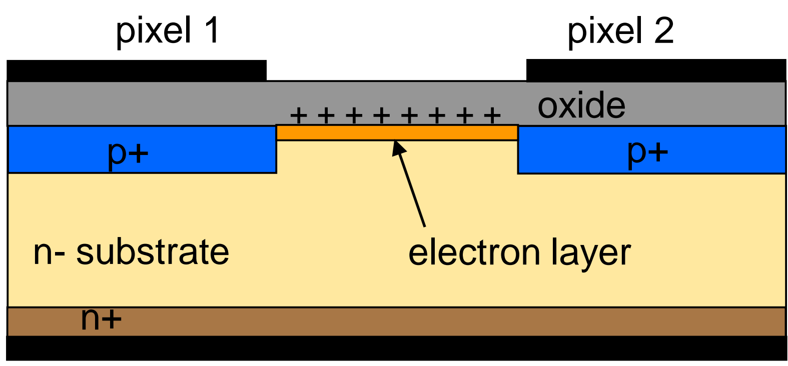
1. Positive fixed oxide charge density induces a negative charge at the Si-SiO_2 interface, which affects:
   a) isolation between n^+ regions;
   b) parasitic capacitance between adjacent regions (→ noise);
   c) electric fields at surface: breakdown;

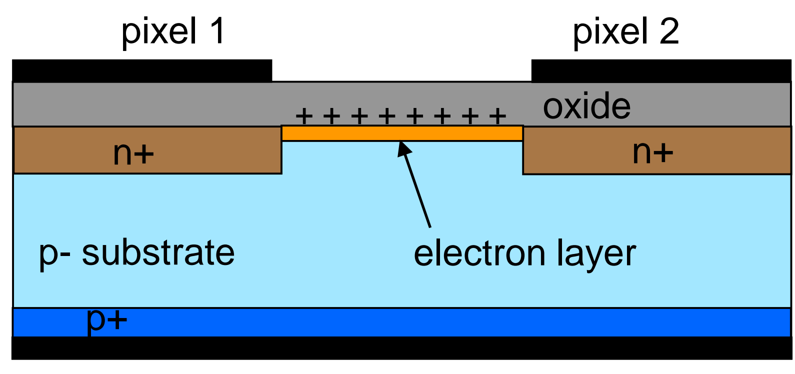
2. Surface generation/recombination leads to increased surface leakage current;

Radiation effects may vary with detector structure …

P-on-N vs N-on-P

With reference to pixel detectors



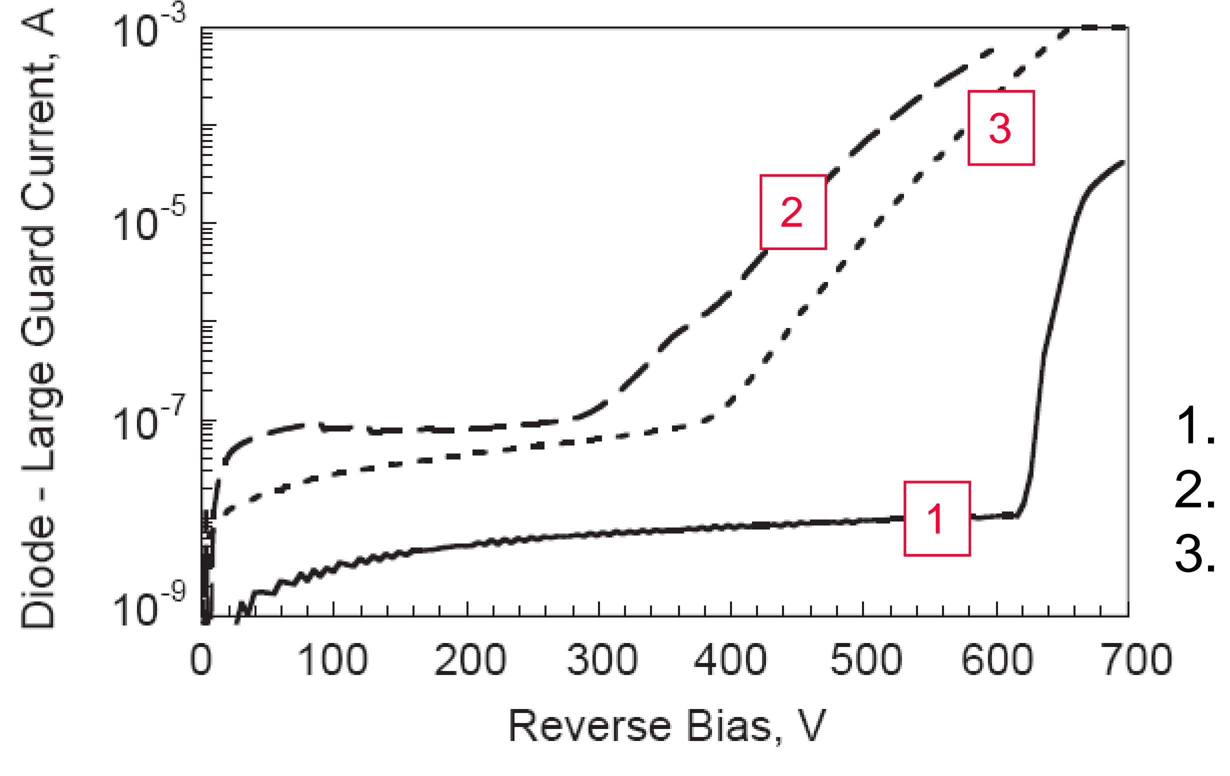


- Pixels are “**self-isolated**”
- Increase of oxide charge density further improves isolation, but:
  - reduces **breakdown** voltage
  - increases inter-pixel **capacitance**

- Pixels are connected by electrons
- Need for **isolation structures**

P-on-N: edge breakdown

Irradiation: CNR Bologna, ^{60}Co gamma source, 200krad(Si)



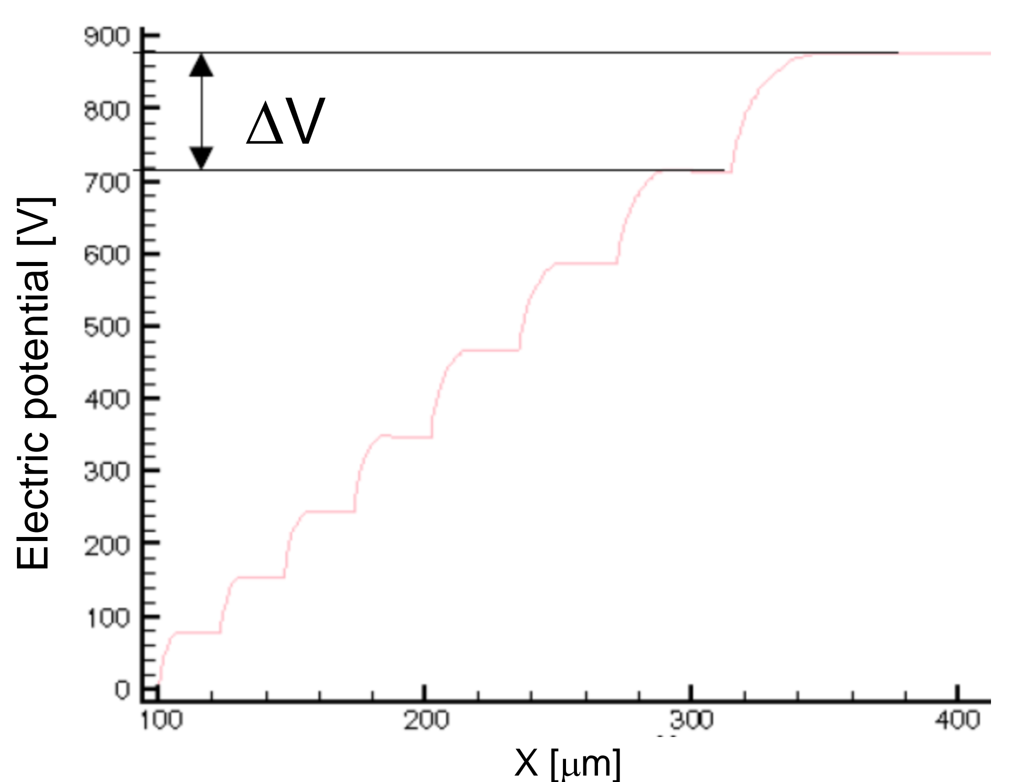
1. pre-irradiation
2. soon after irradiation
3. four days after irradiation

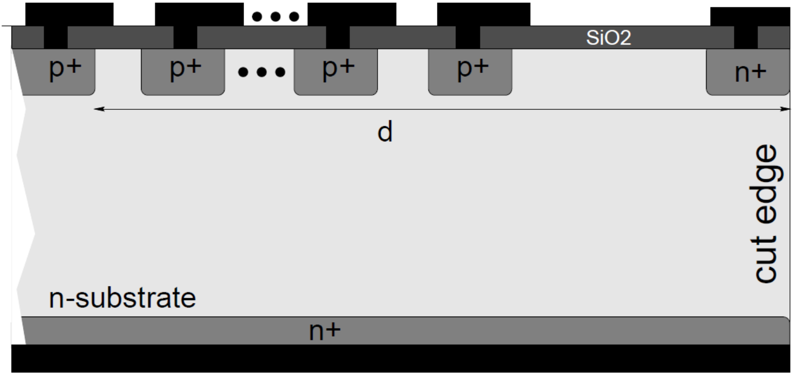
M. Da Rold, et al., IEEE TNS 44(3) (1997) 721

Breakdown voltage decreases after irradiation, and is slightly recovered with room temperature annealing

Multiple rings with field plates

- Guard ring potential scales according to punch-through spreading
- The potential (field) can be evenly distributed enhancing the breakdown voltage, at the expense of dead area at the edges
- Main design parameters: ring spacing, FP size, oxide thickness





M. Da Rold, et al., IEEE TNS 46(5) (1999) 1215, and references therein

Radiation Damage – Bulk Effects

Spatial distribution of vacancies created by a 50 keV Si-ion in silicon.
(typical recoil energy for 1 MeV neutrons)

van Lint 1980

M.Huhtinen 2001

Z=14, A=28
E=50 keV
505 Vacancies

particle → Si_S → E_K>25 eV — V, I — **V**acancy + **I**nterstitial → *point defects (V-O, VV, ..)*

E_K > 5 keV — *point defects and clusters of defects*

Michael Moll – MC-PAD Network Training, Ljubljana, 27.9.2010

NIEL - Displacement damage functions

1 MeV neutron equivalent damage

1MeV

NIEL - Hypothesis: Damage parameters scale with the NIEL

(! does not hold for all particles & damage parameters)

Michael Moll – MC-PAD Network Training, Ljubljana, 27.9.2010

Effect on detector properties

Bulk (Crystal) damage due to Non Ionizing Energy Loss (NIEL)

1. Increase of leakage current (increase of shot noise)
2. Change of effective doping concentration (higher depletion voltage, under- depletion)
3. Increase of charge carrier trapping (loss of charge)

Impact on detector performance and **Charge Collection Efficiency**

Michael Moll – MC-PAD Network Training, Ljubljana, 27.9.2010

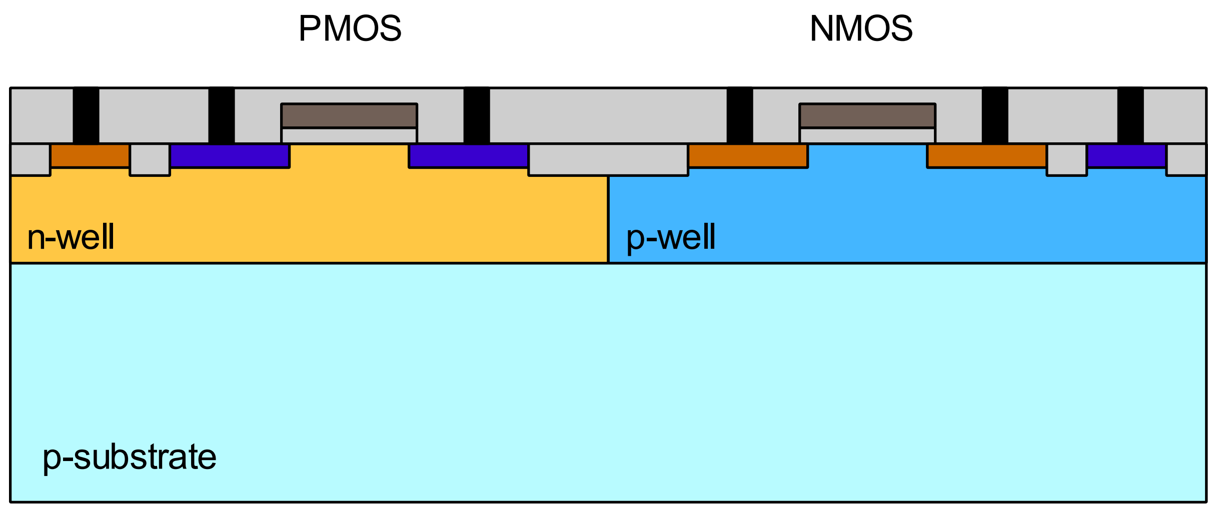
Outline

- Radiation detection in silicon
- CMOS technologies: characteristics, opportunities and challenges
- Monolithic active pixels for photon imaging
- MAPS: design approaches and research directions
- SEED project overview

CMOS process

- Twin-tub process: industrial standard for digital electronics
- Standard CMOS process includes p/n junctions that can be used for radiation detection
- Commercial development of CMOS optical image sensors started in the 1990s

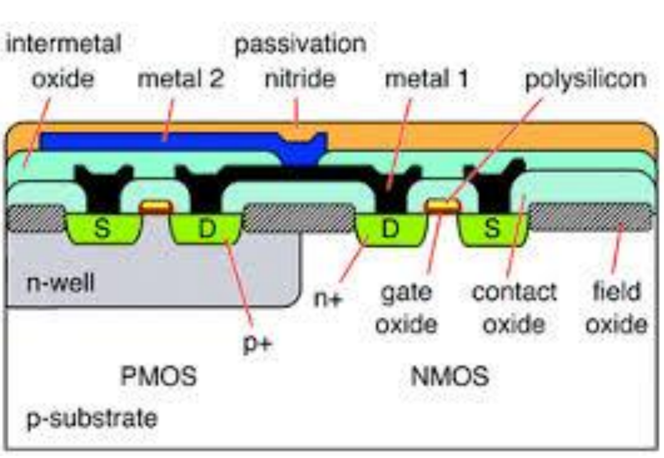
Standard CMOS process - simplified cross section



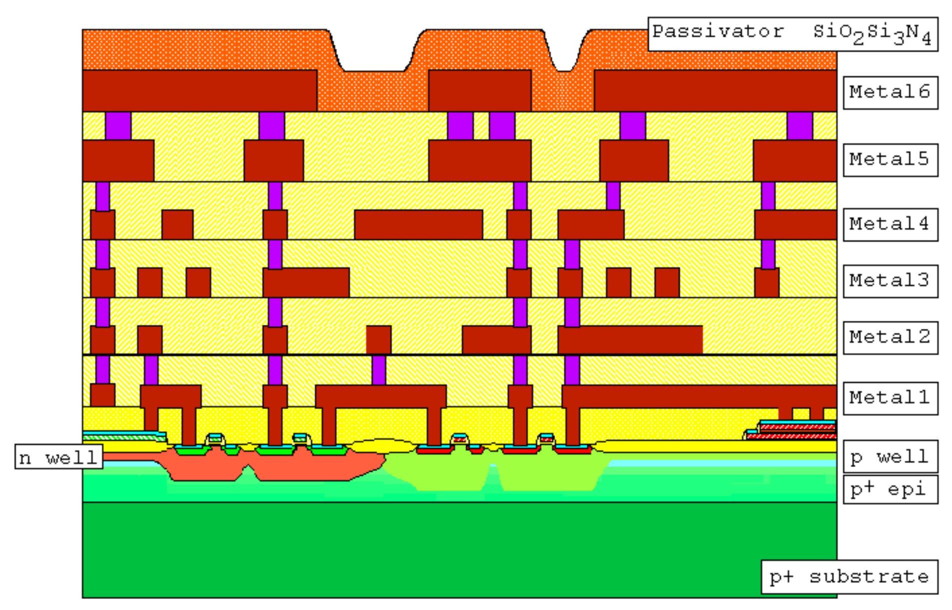
CMOS process layer stack

In standard CMOS, stack thickness increases with technology advancement

2-metal process:
Passivation stack: < 1µm



6-metal process
passivation stack thickness: 3-5µm



CMOS technologies

MOSFET gate length scaling

K. Schuegraf, IEEE J. Electron Devices Society, 2013

CMOS technology roadmap

Date Production Part Available*

Foundry	2012	2013	2014	2015	2016	2017	2018	2019	2020
tsmc	28HPM		20SoC 28HPC	16FF-T 16FF+	16FFC	10FF	7FF	7HPC	5nm
SAMSUNG			20LPE	14LPE	14LPP	10LPE	10LPP	7nm	
GLOBAL FOUNDRIES					14LPP	22FDX		7nm 12FDX	
intel	22nm	22SoC	14nm	14SoC	14nm+	10nm 10SoC			7nm

*risk production and qualification start is typically 1 year ahead

www.techinsights.com

Digital mainstream

How transistors are evolving

No end in sight for logic scaling

ASML
Public
Slide 17
November 2014

N 20	N 20 / N 14	N10	N 20 / N 7	N 7 / N 5	N 5 / N 3.5
Bulk CMOS: Complementary Metal Oxide Semiconductor	**SOI:** Partially depleted Silicon on insulator	**SOI:** Fully depleted Silicon on insulator	**Bulk FinFet :** fin field effect transistor	**SOI FinFet :** silicon on insulator fin field effect transistor, III-V	Gate-all-around transistor

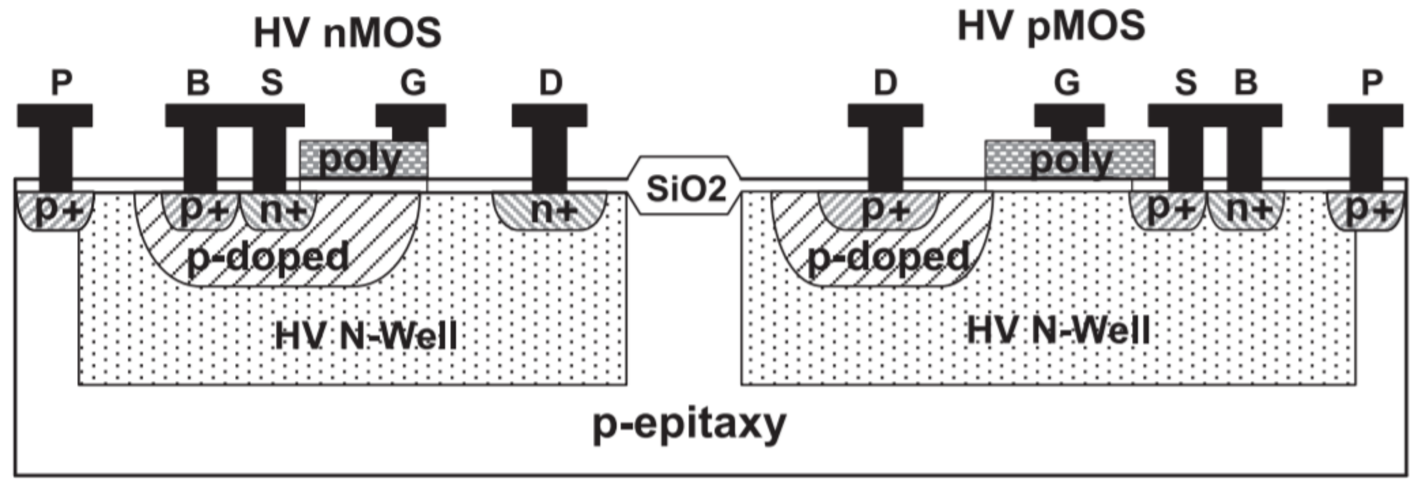
www.sec.gov

Add-ons to standard CMOS

- Supply voltage reduces with CMOS node size: advanced digital nodes not ideal for analog design:
  - Low input/output voltage range
  - Low headroom for cascode stages
- Technology add-ons for **analog circuits**:
  - 3.3V – 5V transistors
  - Different thresholds: high – low – 0 threshold
  - Metal capacitors

High-Voltage CMOS

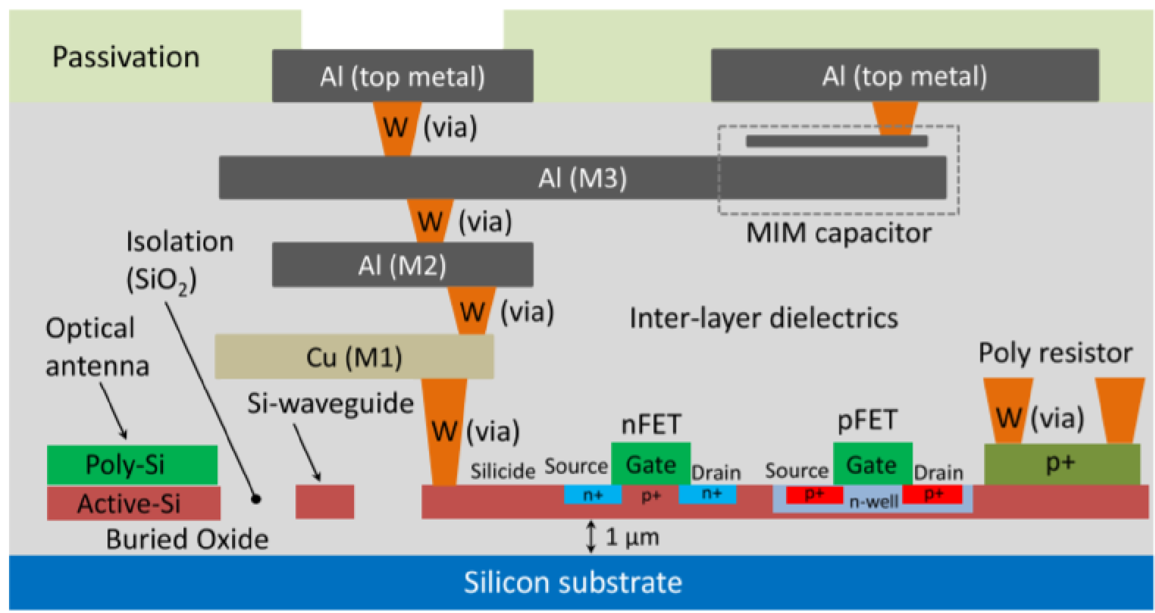
- Power electronics: high voltage MOSFETS
- Low-doped substrate or epitaxial layers
- Deep nwells and pwells in addition to regular nwell and pwells



S. Dai, IEEE TCAS I, 2015

SOI processes

- Insulator substrate: SiO_2 buried oxide or sapphire
- Low parasitics (RF applications, high speed)
- Higher substrate costs



S. Chung, IEEE J. Solid-State Circuits, 2018

Research on hybrid bonding

	3D-SIP			3D-SIC	3D-SOC			3D-IC
3D Technology	"PoP"	"Chip last"	"Chip first"	Die stacking	Parallel W2W		Sequential FEOL	
3D-Wiring level	Package I/O	Chip I/O Interposer I/O	Chip I/O	Global	Semi-global	Intermediate	Local	FEOL
				Chip BEOL Wiring Hierarchy				
Partitioning	Functional unit	subsystem	Embedded die	Die	Blocks of standard cells		Standard cells	Transistors
Technology	Package-to Package reflow	Multi-die SIP 3D/2.5D stack	FO-WLP Embedded die	3D D2D, D2W 2.5D Si-interposer	Wafer-to-Wafer bonding Hybrid bonding	Via-last	Active layer transfer or deposition	
2-tier stack Schematic								
Characteristic	Solder ball Stack	• C4, Cu-pillar Si-Organic • Through-Mold-vias	• Bumpless • Si-RDL • Through-Package-vias	• µbump • Si-to-Si • Through-Silicon-Via	BEOL between 2 FEOL layers Overlay 2nd tier defined by W2W alignment/bonding		Overlay 2nd tier defined by litho scanner alignment	FEOL stack
Contact Pitch	400⇒350⇒300µm	120⇒80⇒60µm	60 ⇒40 ⇒20µm	40 ⇒20 ⇒10⇒5µm	5µm ⇒ 1 µm	2 µm ⇒ 0.5 µm	200nm ⇒ 100nm	< 100 nm
Relative density:	1/100⇒1/77⇒1/55	1/9⇒1/4⇒1/2.3	1/2.3 ⇒ 1 ⇒ 4	1 ⇒ 4 ⇒16⇒ 64	64 ⇒ 1600	400 ⇒ 6400	4 10^4 ⇒ 1.6 10^5	$> 1.6\ 10^5$

Eric Beyne, IMEC, January 2018

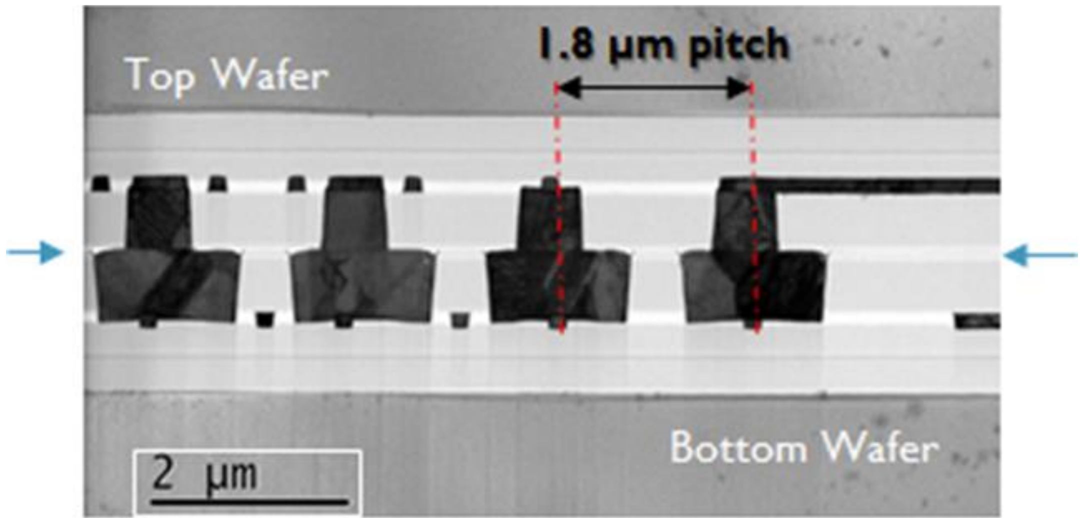
Hybrid bonding – State of the Art

By David Manners 24th January 2017

Electronics Weekly.com

Imec, EVG demo superior overlay accuracy for wafer-to-wafer bonding

Imec and EVG have demonstrated 1.8µm pitch overlay accuracy for wafer-to-wafer bonding.

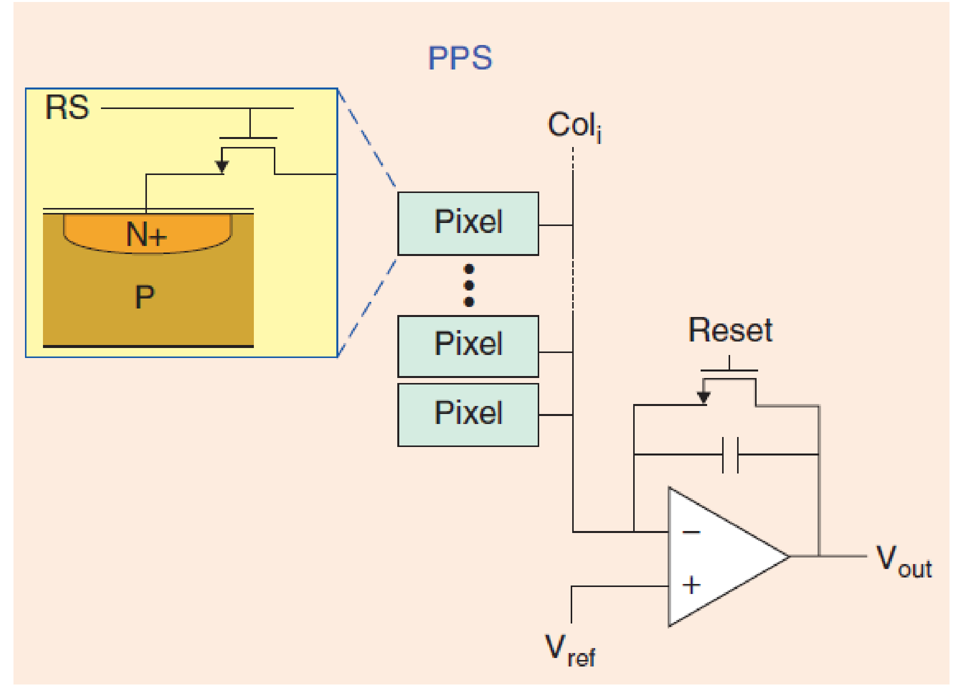


https://www.evgroup.com/en/about/news/2017_01_imec/

Outline

- Radiation detection in silicon
- CMOS technologies: characteristics, opportunities and challenges
- Monolithic active pixels for photon imaging
- MAPS: design approaches and research directions
- SEED project overview

Passive Pixel Sensor (PPS)



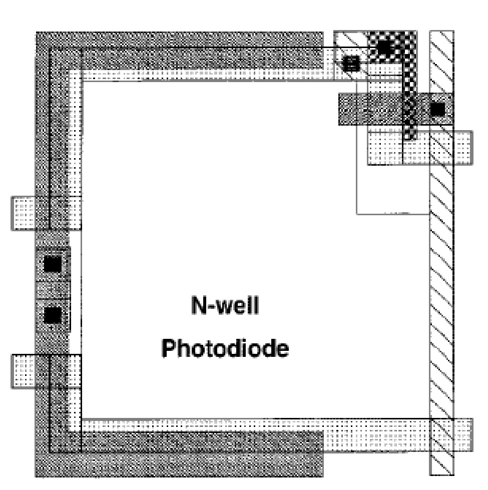
- The PPS consists of a photodiode and just one transistor TX.
- TX is used as a charge gate, switching the contents of the pixel to the charge integration amplifier (CIA).

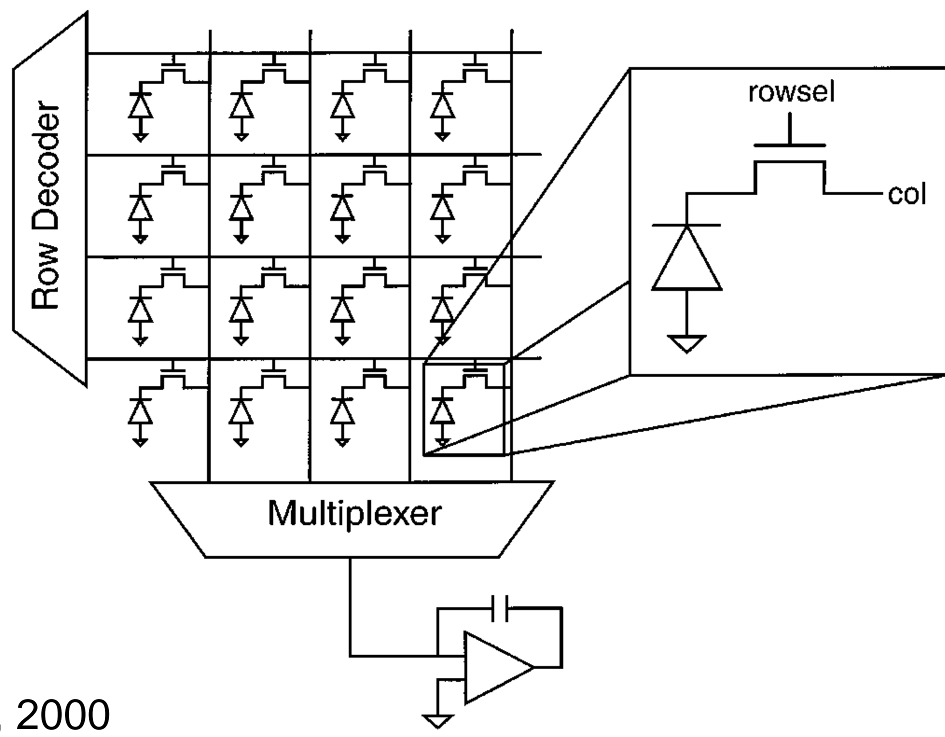
First introduced by G. Weckler in 1967:
G. P.Weckler, IEEE J. Solid-State Circuits, vol. SC-2, pp. 65–73,1967.

A. El Gamal, "CMOS Image Sensors", IEEE Circuits and Devices Magazine, pp. 6 – 20, 2005.

Passive Pixel Sensor (2)

- Advantage: high fill factor – each pixel has only one transistor.
- Architecture: 1 amplifier per chip or 1 amplifier per column



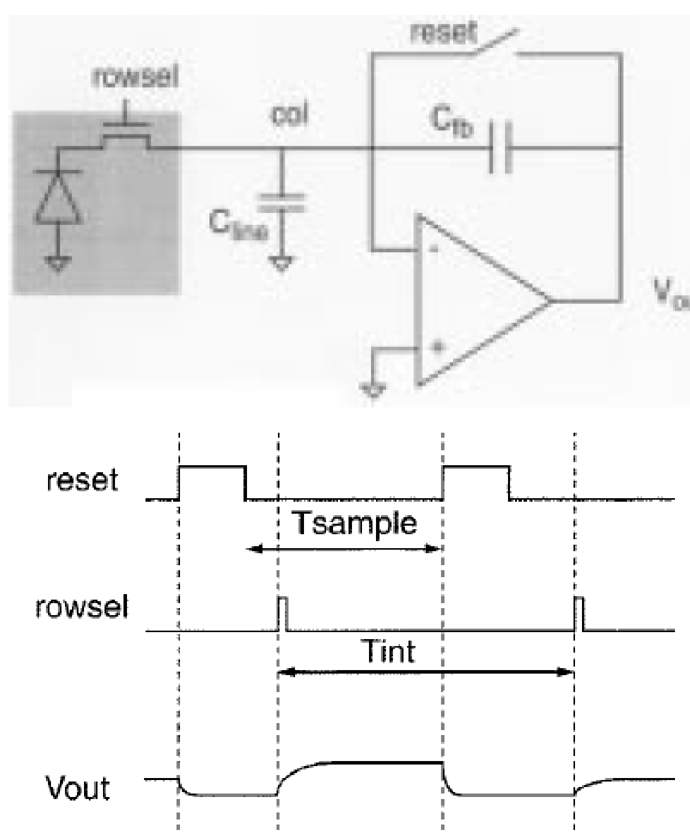


I. L. Fujimori, IEEE J. Solid-State Circuits, 2000

Passive Pixel Sensor (3)

Major problem: large capacitive loads (metal lines):

- High **readout noise**
  250 electrons rms typically
- Low readout speed in large pixel arrays.



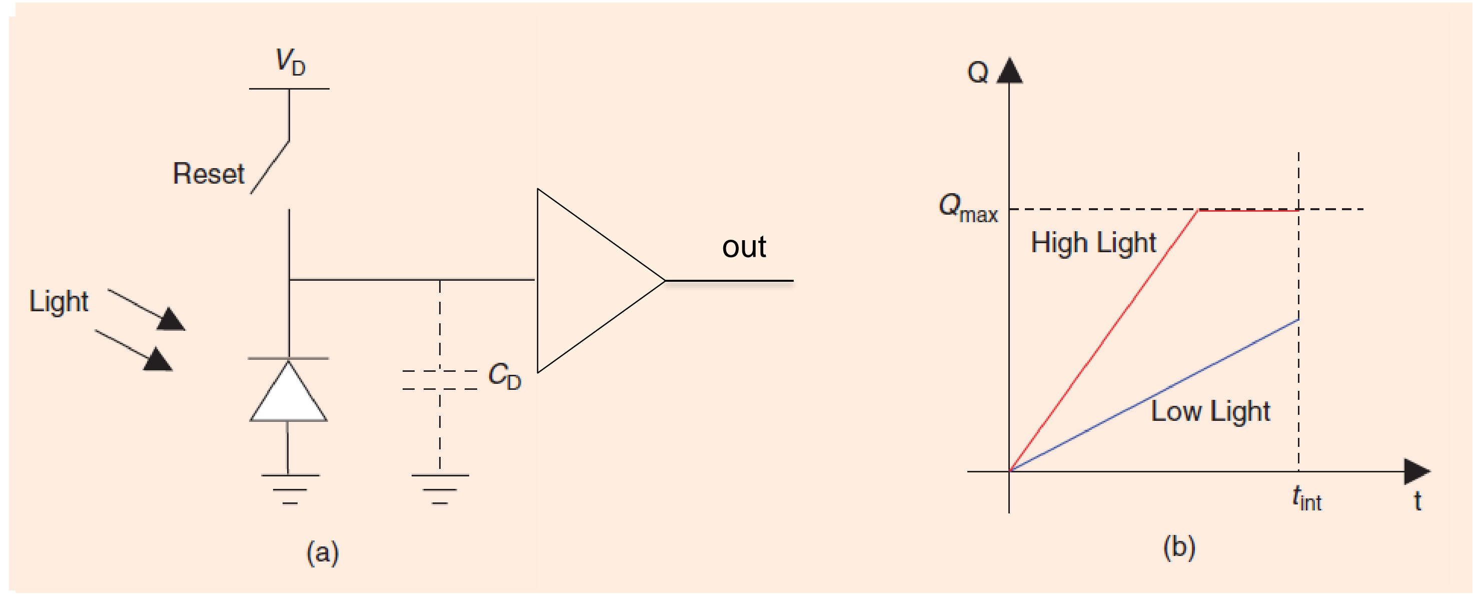
Active Pixels

- Buffer amplifier in the pixel
- Origins: end of the 1960s
- Optical imaging applications
- CCDs were much more reliable at the time. Active pixel emerged in the 1990

- P.J.W. Noble, "Self-Scanned Silicon Image Detector Arrays". IEEE Tran. Electron Dev. Vol. 15, pp. 202–209, 1968.
- S. G. Chamberlain, "Photosensitivity and Scanning of Silicon Image Detector Arrays". IEEE Journal of Solid-State Circuits vol. 4 pp. 333–342, 1969.

Active Pixel Sensor

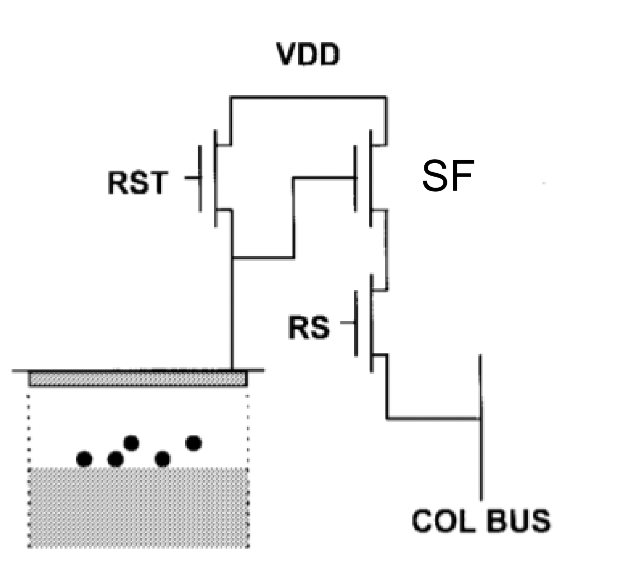
- Charge is integrated on photodiode capacitance
- Output of the photodiode is buffered using in-pixel follower

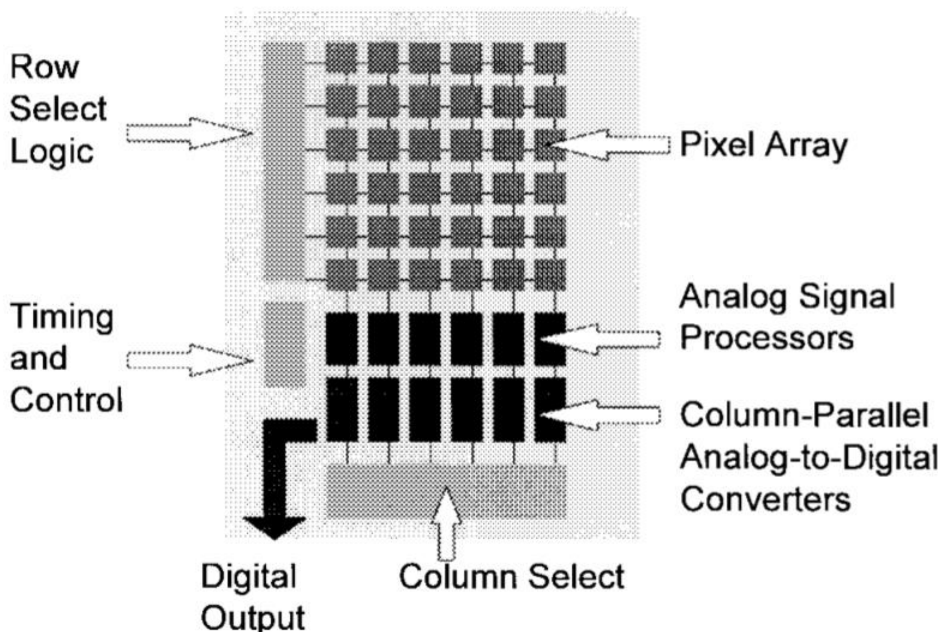


A. El Gamal, IEEE Circuits and Devices Magazine, 2005.

Active Pixel Sensor (3T - APS)

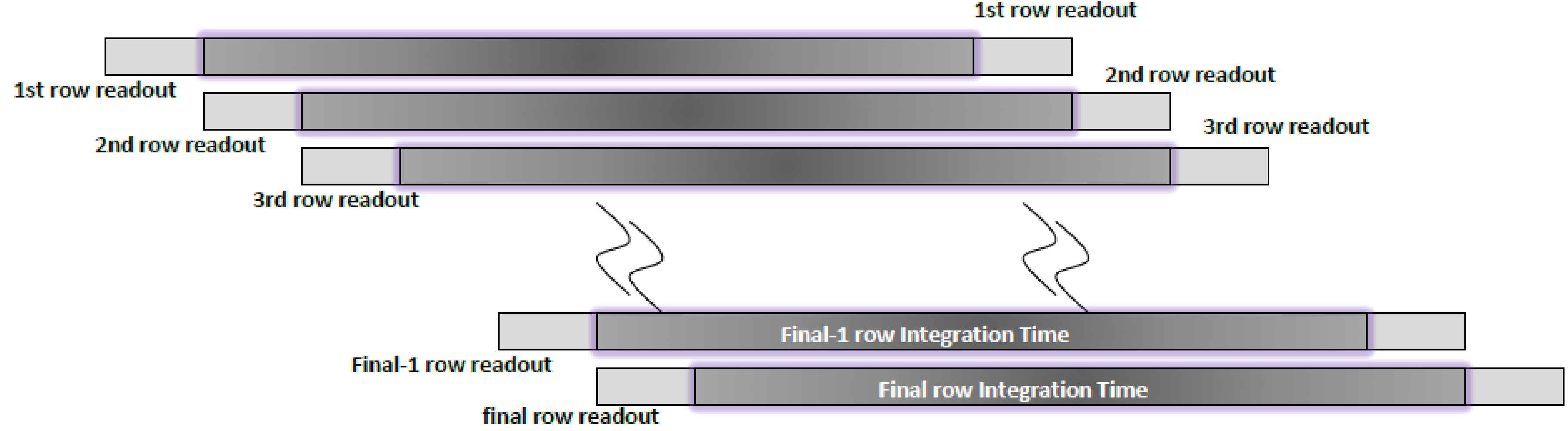
Conversion gain depends on the total capacitance at the SF gate: PD + parasitic capacitances





E. R. Fossum, "CMOS image sensors :electronic camera-on-a-chip", IEEE Trans. On Electron Devices 44 (10) (1997)

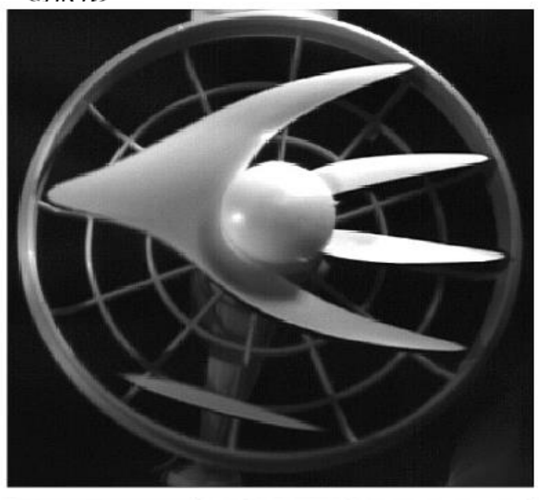
Array redout: rolling shutter

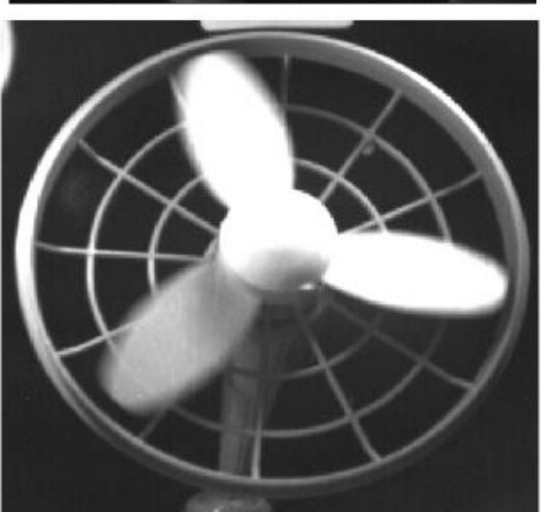


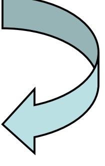
- Pixel voltage is read out one row at a time
- Row integration times are staggered by row/column readout time
- The progressive scanning of the image cause artifacts (distortion) when the scene is changing fast.

Rolling shutter effects

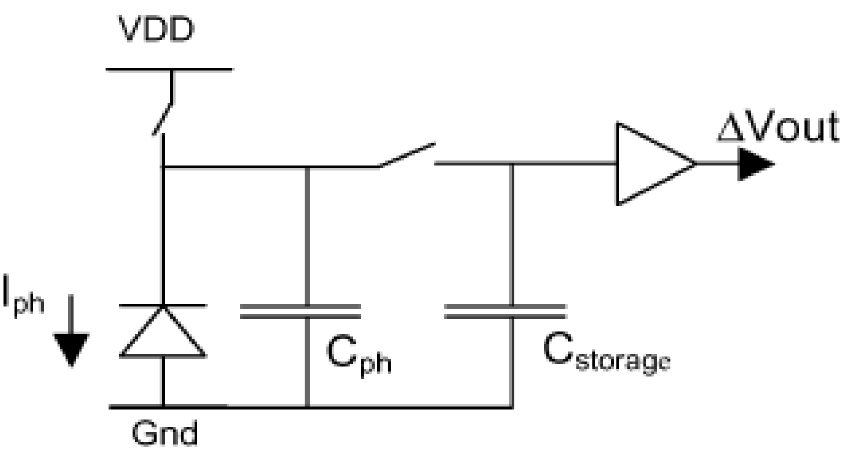
Global shutter pixels







- In-pixel Sample-and Hold
- Problem: GS adds complexity and reduces the Fill Factor

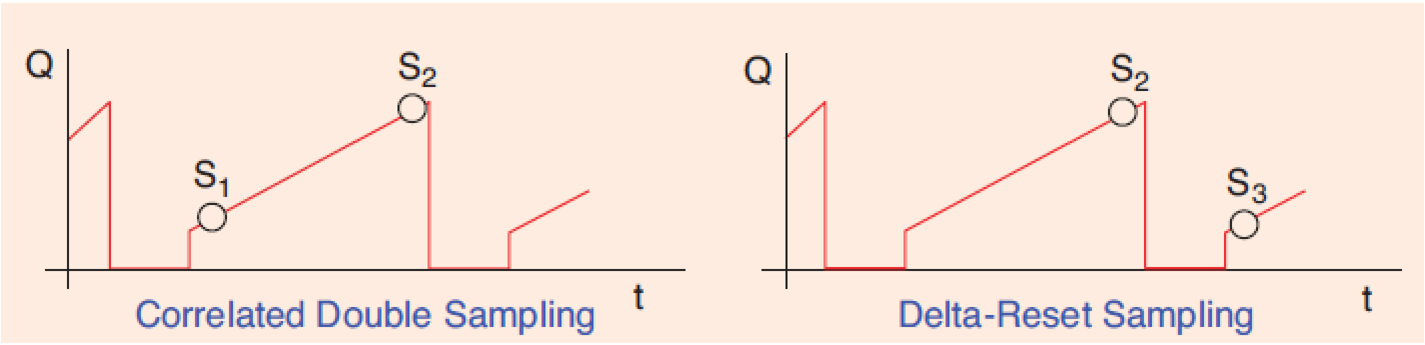


Ref: IEEE Transactions on Electron Devices, Vol. 50, No. 1, Jan. 2003

3T – APS: signal sampling

Two different sampling schemes:

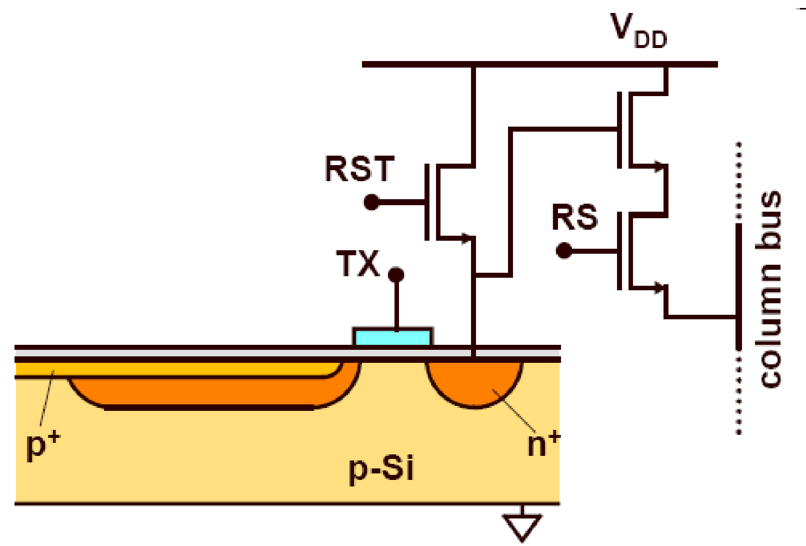
- **Correlated double sampling** (CDS):
  - eliminates reset noise
  - Samples are separated in time
- **Delta-reset sampling**:
  - Does not eliminate reset noise
  - samples are close in time



A. El Gamal, IEEE Circuits and Devices Magazine, 2005.

Pinned – photodiode APS (4T – APS)

- **Pinned photodiode**: buried p+/n/p photodiode that can be fully depleted of electrons
- First introduced in CCDs, later ported to CMOS image sensors



A. Theuwissen, Proc. IEEE ESSDERC 2007

Pinned photodiode operation

After light integration

After charge transfer

PPD associated to a TG + FD

PPD TG FD

PPD TG FD

N_{PPD} p+ n+ SCR SCR p-epi p-epi

N_{PPD} p+ n+ SCR SCR p-epi p-epi

Standard PD associated to a TG + FD

PD TG FD

PD TG FD

n+ N_{well} SCR SCR

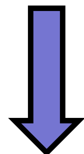
N_{well} n+ SCR SCR

A. Pelamatti PhD Thesis, University of Toulose, 2015

4T-APS vs 3T-APS

Advantages:

- Conversion gain (q/C_{FD}) is independent of detector, 4T-APS can achieve higher conversion gain than photodiode APS
- Lower noise: reset noise cancellation and lower dark current



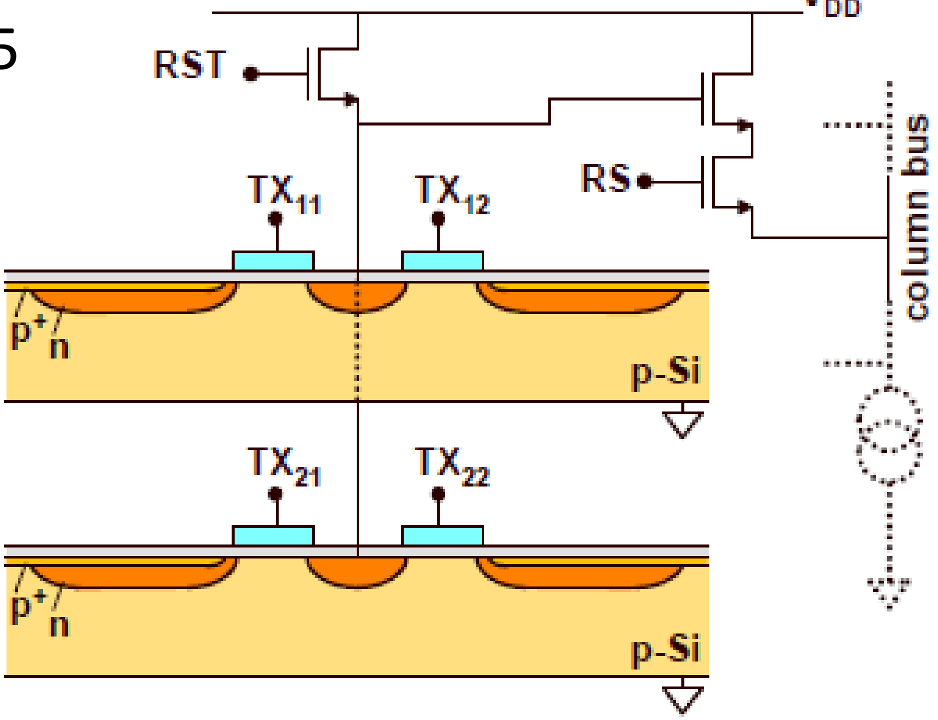
Higher performance (SNR) for low-light imaging

Disadvantages:

- More devices than 3T-APS (lower Fill Factor)
- Destructive readout

Transistor sharing

- A group of pixels (typically 4) can share some transistors (reset, SF, row select).
- Total number of transistors in 4 pixels: 4 + 3
- Transistors x pixel: 7/4 = 1.75
- Other sharing schemes can be implemented



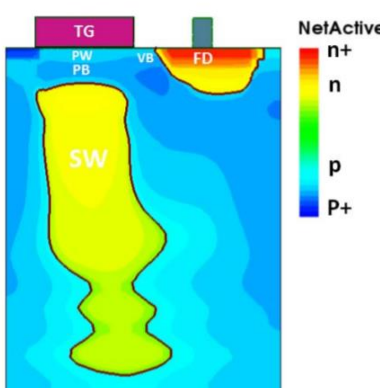
A. Theuwissen, Proc. IEEE ESSDERC 2007

Noise reduction

Sub-electron noise reduction by

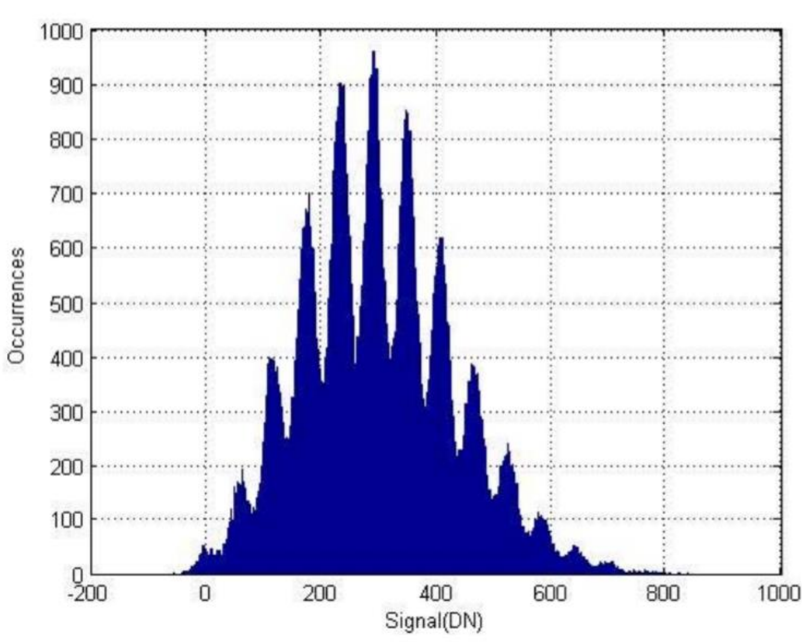
- Boosting conversion gain
- Implementing advanced filtering techniques
- Optimizing process

} **Photon counting**



Pixel pitch: 1.4um
Conversion gain: 400uV/e-
Noise rms: 0.34e-

Output signal histogram



J. Ma and E. Fossum, IEEE Electron Device Letters, 2015

Pixel size scaling

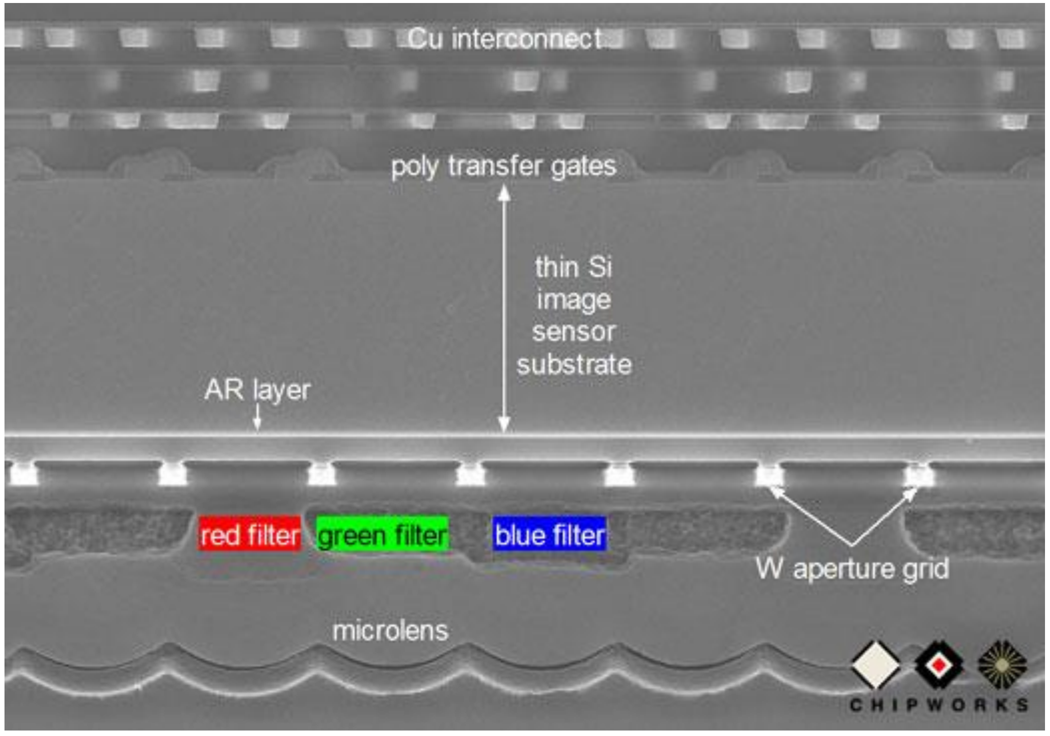
- Commercial products with 0.9um pixels are entering the market
- Current research: deep sub – um pixels (0.4 – 0.7um pitch)

(um^2)
Minimum Pixel Area
100
10
1
Microlens
Inner Microlens
Shifted Microlens
Lightpipe
Pinned PD
(PPD)
50% shrinkage
in 3.5 years
BSI
Stack
DTI
CCD
CMOS
80 85 90 95 00 05 10 15
Mass Production Year

N. Teranishi – FFE 2016

CIS processes: backside illumination

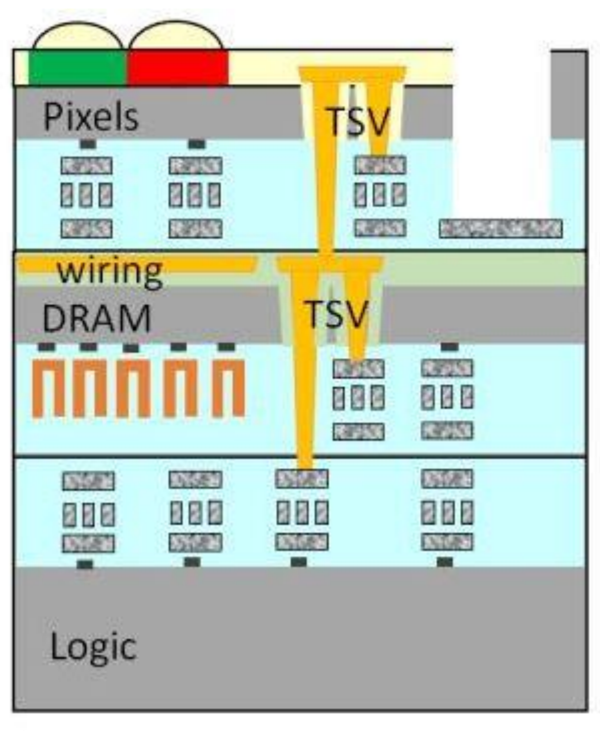
- Thinning down to 2.5um – 3um
- Backside processing
- Color filters
- Microlenses



http://image-sensors-world.blogspot.it

CIS processes: 3D stacking

- State of the art: Sony 3-layer stacked image sensor



Sony, IEDM 2017

- Upper TSV connects pixels and DRAM chips
- Lower TSV connects DRAM and logic chips
- TSV wiring is located on DRAM backside

TSV diameter: 2.5μm
pitch: 6.3μm

Deep Depletion PPD sensors

18 µm thick, 1kΩ·cm epitaxial silicon

180nm CMOS process

Goal: low-noise IR imaging

Deep Depletion Extension:
Allows backside bias

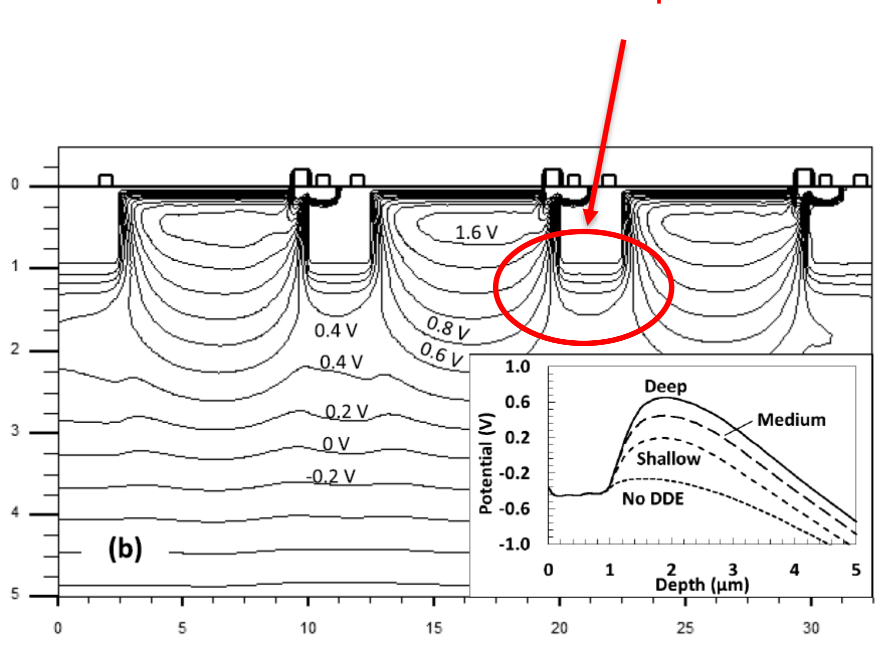
OD
RSEL
T1
T2
OUT
Guard ring
V_{BSB}
Guard space
3.3V
0 V
TG
RG
RD
Pinning implant (p+)
p-well
n-well
STI
PPD (n)
n+
n+
STI
Pixel p-well
Pixel p-well
Deep n-well
DDE (n)
Sense node
DDE (n)
L_{DDE}
Not depleted
Depleted
High resistivity epitaxial Si (p-)
p++ substrate

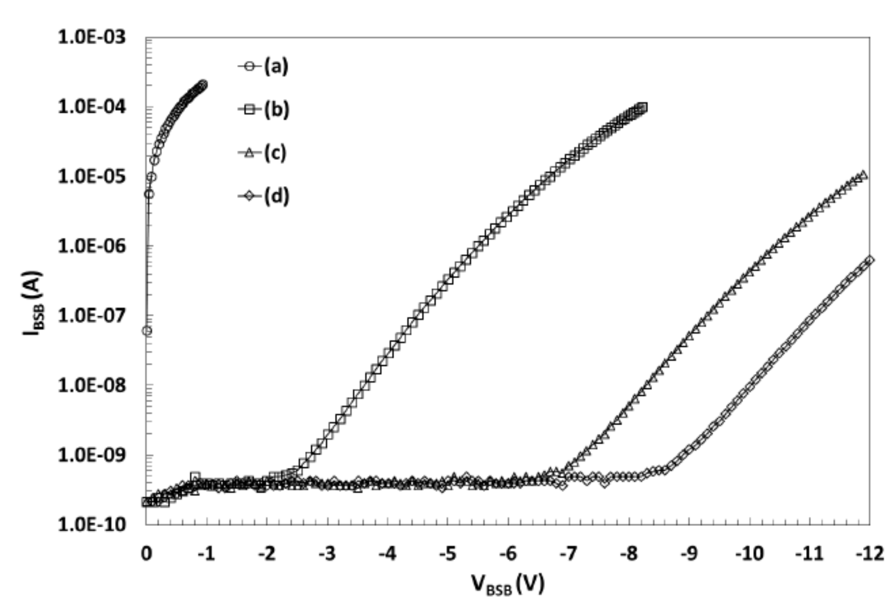
K.D. Stefanov, IEEE Electron Dev. Lett., vol. 38, no. 1, pp. 64-66, Jan. 2017.

Deep Depletion PPD: backside bias

Backside current vs. DDE implant dose

Barrier potential





Outline

- Radiation detection in silicon
- CMOS technologies: characteristics, opportunities and challenges
- Monolithic active pixels for photon imaging
- MAPS: design approaches and research directions
- SEED project overview

MAPS applications in HEP

Few example applications in HEP so far:

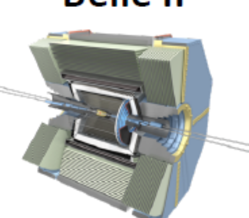
- STAR: detector area = 0.15 m^2, data taking started in 2014
- ALICE: detector area = 12 m^2, to be installed in 2020
- Promising for precision experiments (ILC)
- R&D for outer pixel layers at HL-LHC

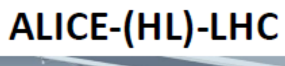
Pixel detectors for HEP

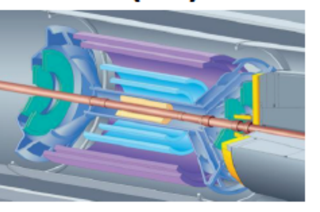
Rate and Radiation Levels

STAR

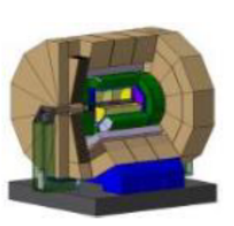
Belle II



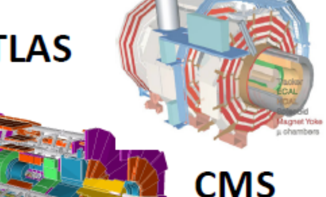




ILC



ATLAS



CMS

Numbers for innermost layers (r ≈ 5cm,) -> scale by 1/10 for typical strip layers (r > 25 cm)

	STAR	Belle II	ALICE-LHC heavy ion	ILC	LHC pp	HL-LHC-pp	
						Outer	Inner
BX-time (ns)	110	2	20 000	350	25	25	25
Particle Rate (kHz/mm^2)	4	400	10	250	1 000	1 000	10 000
Φ (n_{eq}/cm^2)	few 10^{12}	3 x 10^{12}	> 10^{13}	10^{12}	$2x10^{15}$	10^{15}	$2x10^{16}$
TID (Mrad)*	0.2	20	0.7	0.4	80	50	> 1000

*per (assumed) liftetime
LHC, HL-LHC: 7 years
ILC: 10 years
others: 5 years

in need for
- much less material
- higher resolution
- thinner strips & monolithic pixels

state of the art
- large area strips
- hybrid pixels

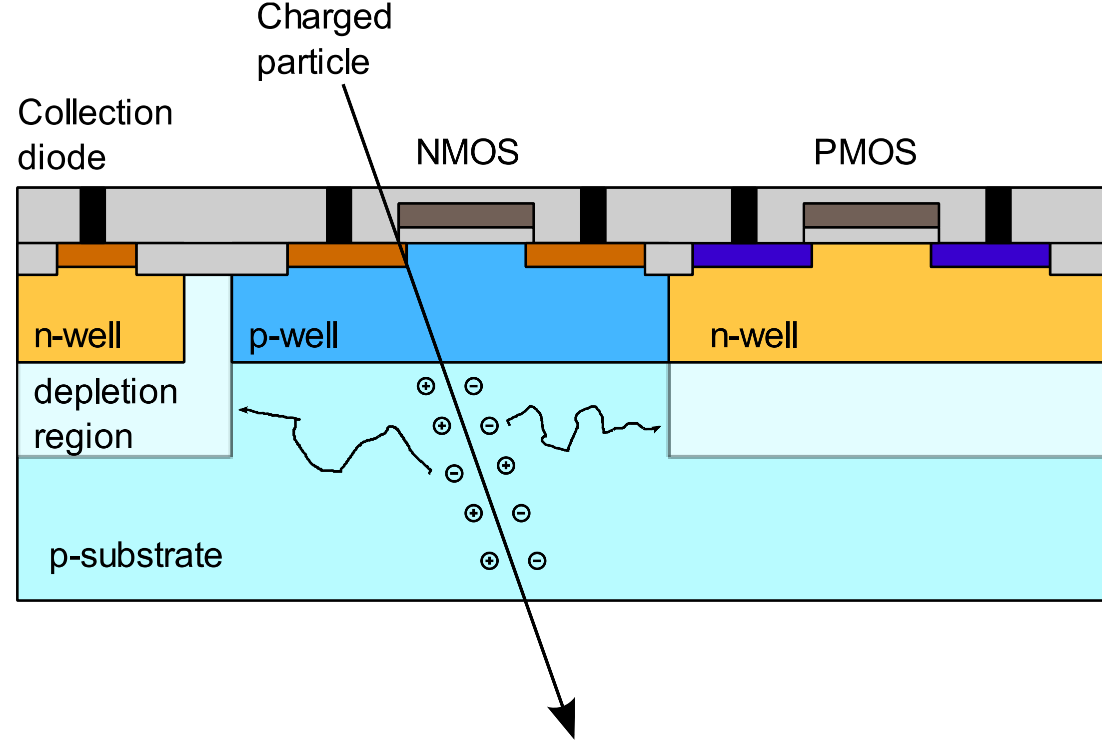
- even larger area
- radhard sensors
- higher rates R/O
- R&D of new types

N. Wermes, 14th VCI Wien, 2/2016

Monolithic sensors

Standard CMOS has problems:

- Collection speed: slow diffusion in undepleted substrate
- Competitive collection by nwell: low efficiency

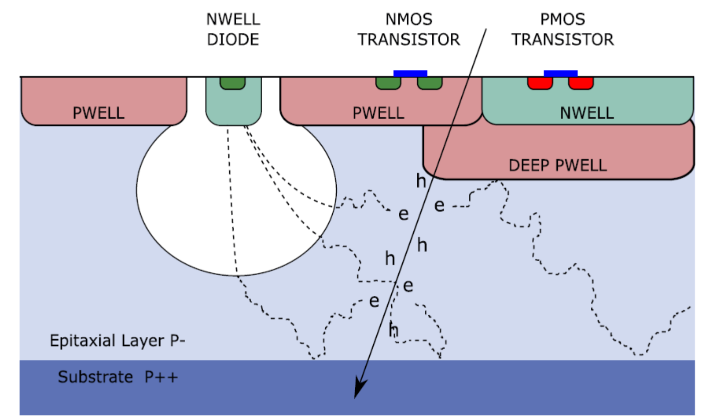


Solutions

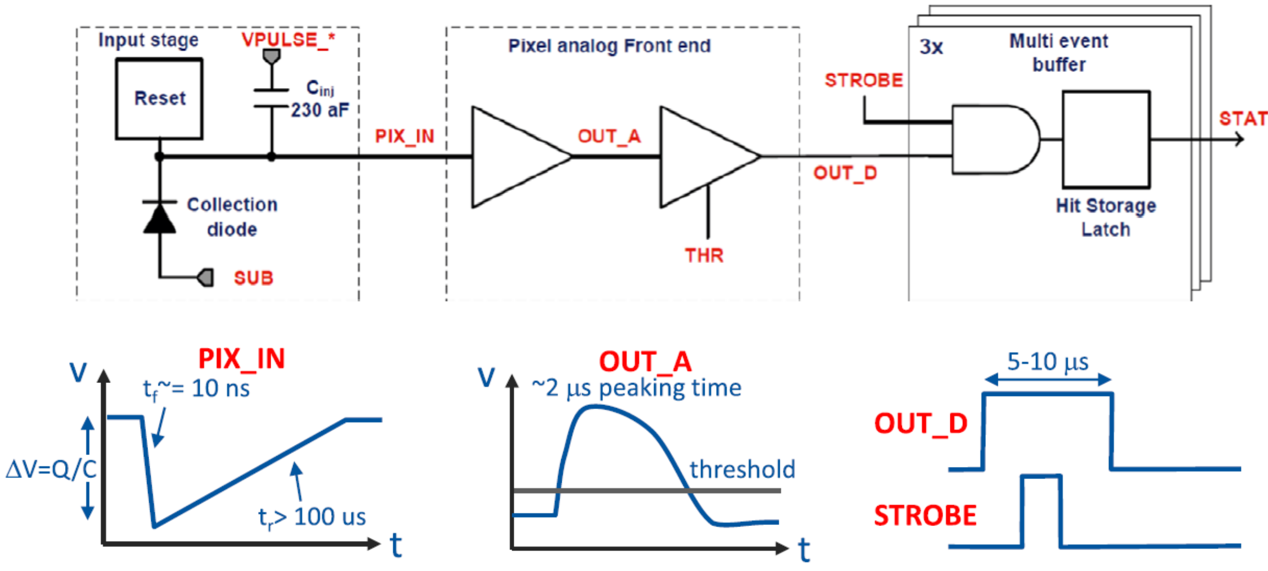
- Lowering substrate doping: high resistivity silicon
- High bias voltage
- Avoid competitive charge collection. Three approaches:
  1. Isolating nwells other than collection electrodes with deep pwell
  2. Put CMOS electronics inside the collection electrode
  3. Isolate the electronics from the detectors with a buried oxide layer → SOI

ALPIDE approach

- Nwell shielded by deep pwell
- High resistivity (> 1kΩ cm) p-type epi-layer with 25 μm thickness
- 28 x 28 μm^2 pixel size
- Small sensor capacitance → low noise
- Partial depletion: drift and diffusion
- Radiation tolerance (TID) up to 700 krad



J.P. Crooks, et al., IEEE TNS 2007



G. Aglieri Rinella, NIMA 845 (2017) 583–587

ALPIDE performance

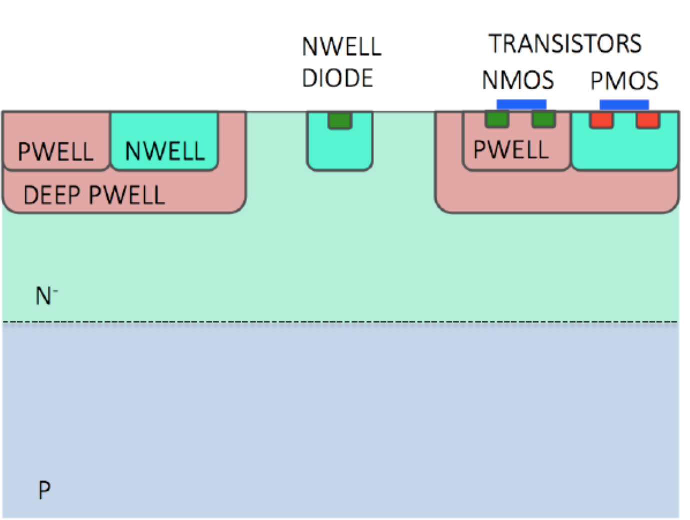
- **Efficiency > 99.5%**
- **Fake hit rate < 10^{-5}** over wide threshold
- NIEL up to **10^{13} (1MeV n_{eq})/cm^2**

Detection Efficiency
Fake-Hit Rate/Pixel/Event
Threshold Current I_{THR} (pA)
Efficiency Fake-Hit Rate
Non-irradiated
1.0×10^{13} 1MeV n_{eq}/cm^2
sensitivity limit
0.015% pixels masked

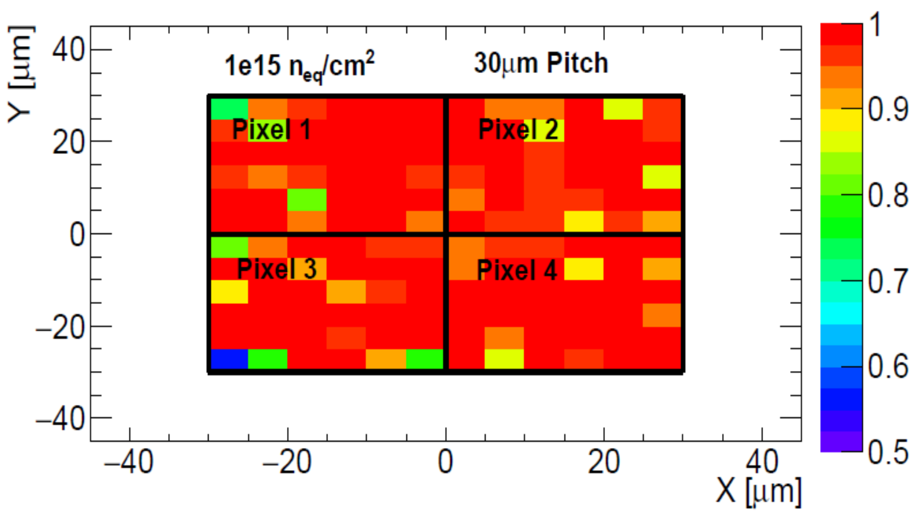
G. Aglieri Rinella, NIMA 845 (2017) 583–587

ALPIDE with n-layer

- Fully depleted n- layer: collection by drift
- Fast charge collection: few ns
- Good efficiency and speed at **10^{15} (1MeV n_{eq})/cm²**



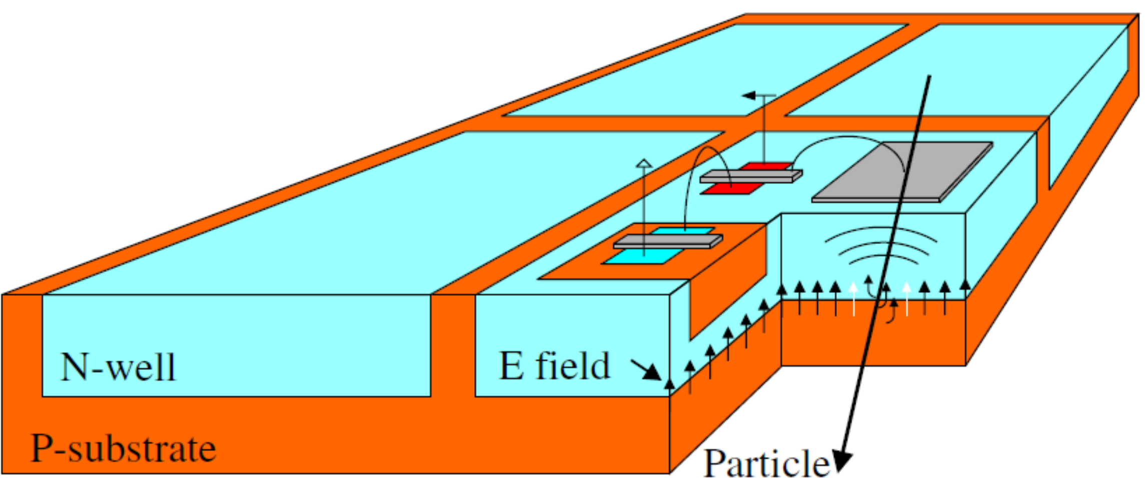
Efficiency vs. hit position



H. Pernegger et al., 2017 JINST 12 P06008

High Voltage CMOS

- The collection diode is a deep nwell.
- The CMOS electronics (pwells + nwells) is inside the deep nwell
- High voltage bias can be applied



I. Peric et al., NIM A582 (2007) pp. 876-885

High-Resistivity HV-CMOS

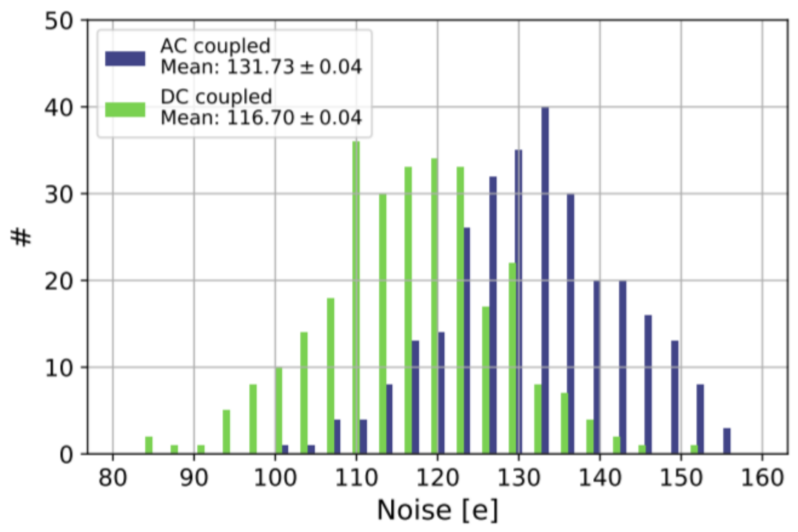
High resistivity substrates (>2 kOhm/cm)

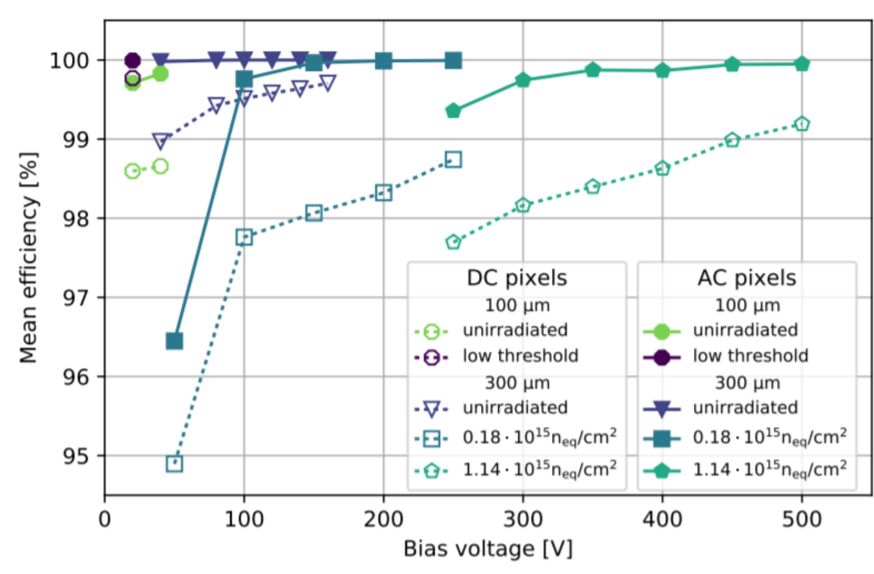
Promising approach:

- Fast charge collection
- High efficiency at fluence > 10^{15} n_{eq}/cm^2

Main drawback:

- Parasitic capacitance: large noise





D.-L. Pohl, 2017 JINST 12 P06020

Fully depleted SOI sensors

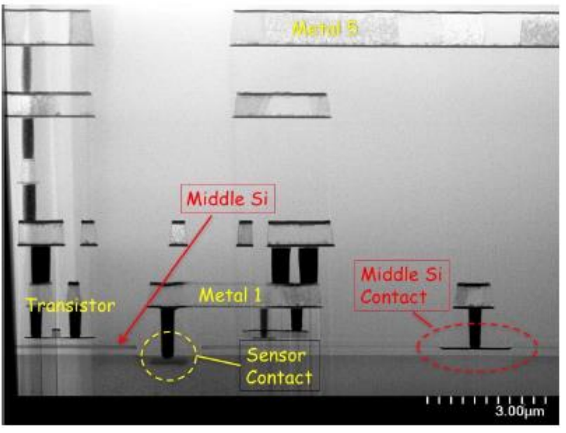
Buried oxide: separates detectors from electronics

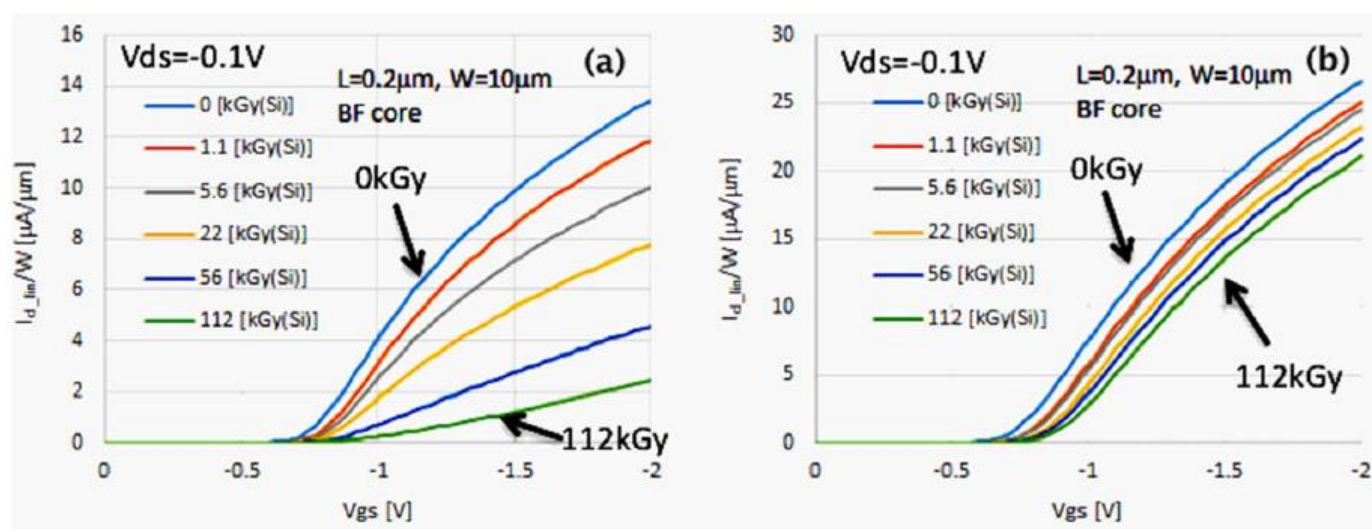
LSI Circuit
NMOS
PMOS
BOX (Buried Oxide)
Middle Si
p+
p- Si Sensor
(High Resistivity
Substrate)
n+
Buried n-Well
p+
Back Plane
Radiation
(X-ray, Electron, Alpha, Charged Particles, ...)

Y. Arai, IEEE IEDM 2017

FD-SOI progress

- Problem: buried oxide affects electronics → back-gate effect
- Solution: 2 buried oxide layer
- Ionizing radiation tolerance up to 100kGy

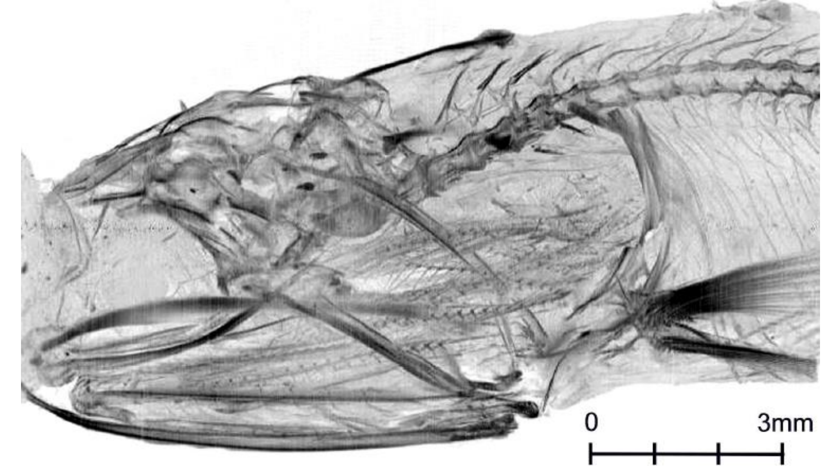


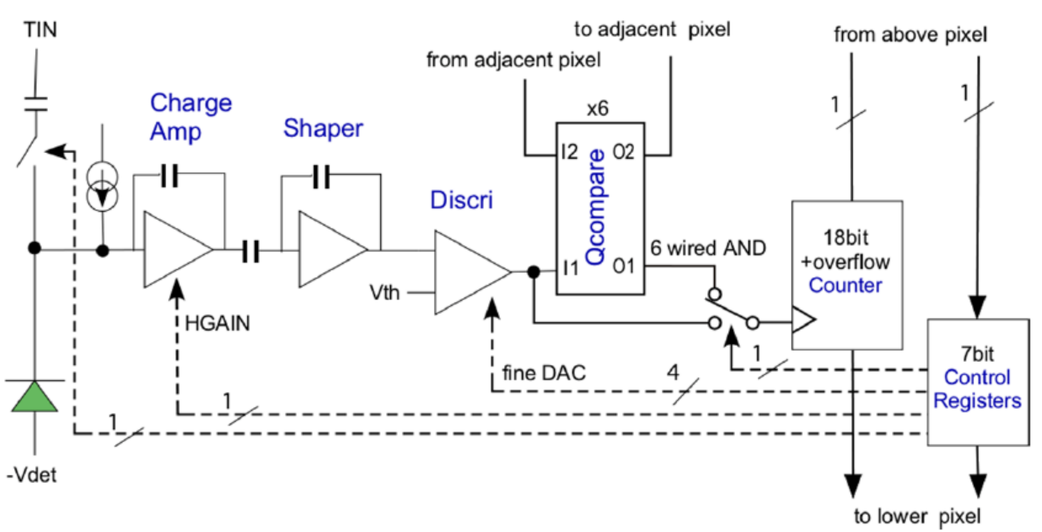


Y. Arai, IEEE IEDM 2017

FD-SOI: X-ray imaging

- Pixel size: 17 µm
- Pixel count: 512 x 832
- Substrate thickness 500µm
- In-pixel photon counting electronics





Y. Arai, IEEE IEDM 2017

Monolithic pixel array with backside junction

CMOS readout and control electronics

N–well containing PMOS circuitry

300 um

Drift paths

Collection electrodes

N–diffusion

Depleted P –type substrate

Isolation structure

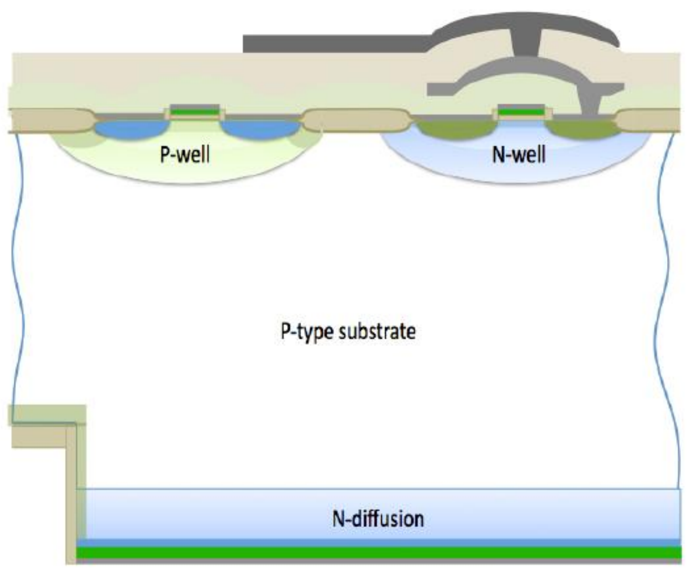
Not to scale

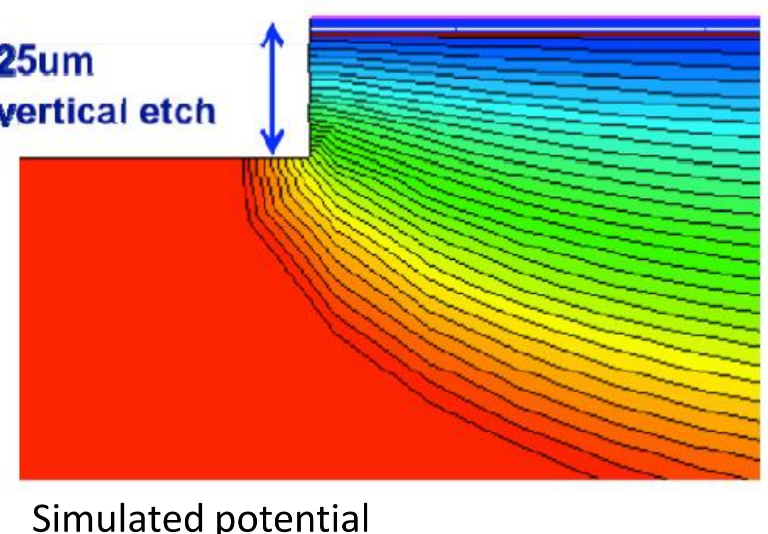
W. Snoeys, IEEE Tran. Electron Dev., 1994

J. D. Segal, IEEE NSS, Knoxville, TN, 2010, pp. 1896-1900.

Monolithic pixel array with backside junction

- PMOS-only pixel electronics
- BS junction terminates on a trench for breakdown prevention
- Difficult to integrate in a commercial CMOS





Simulated potential

J. D. Segal, IEEE NSS, Knoxville, TN, 2010, pp. 1896-1900.

Outline

- Radiation detection in silicon
- CMOS technologies: characteristics, opportunities and challenges
- Monolithic active pixels for photon imaging
- MAPS: design approaches and research directions
- SEED project overview

INFN project SEED project

Sensor with Embedded Electronics Development

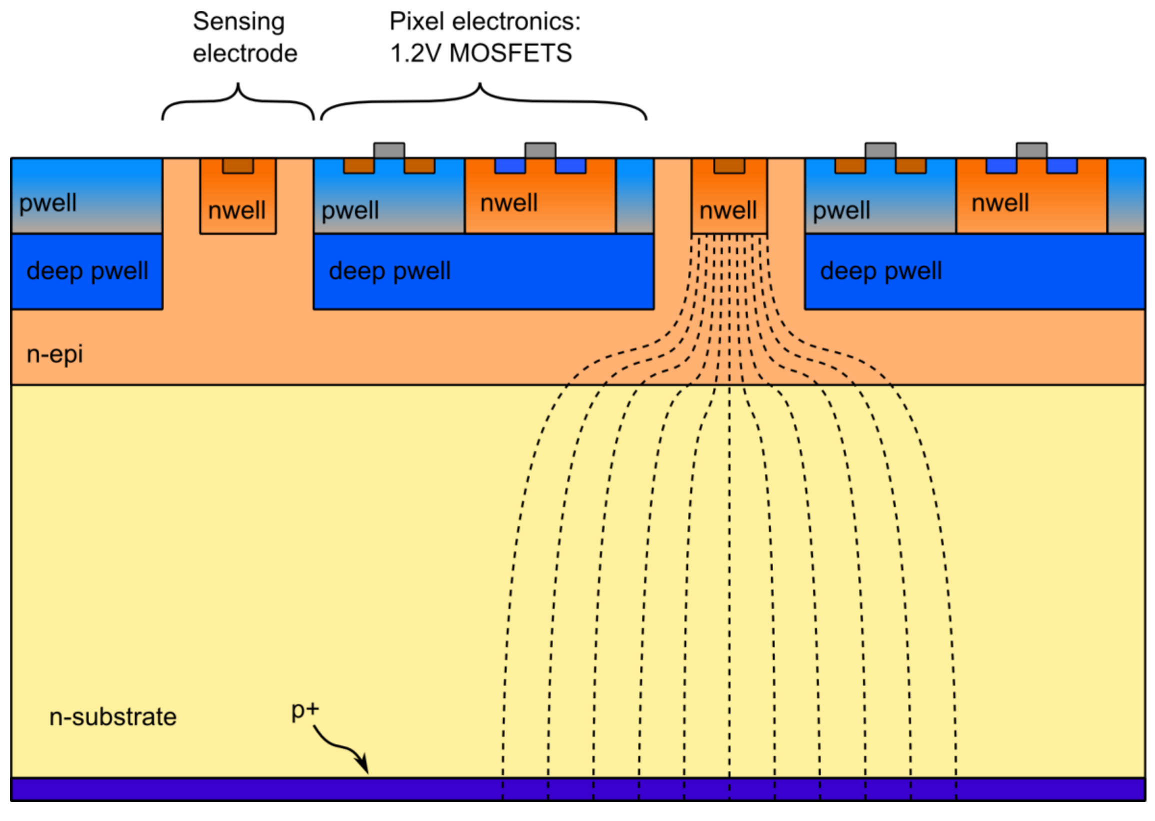
- Goal: fully depleted monolithic pixel sensor
- High timing resolution (ns)
- Integrated CMOS pixel electronics
- Process development with an industrial partner (LFoundry)

INFN sections: Torino, Padova, Trento, Frascati, Perugia

INFN-LFoundry patent pending

SEED approach

Starting point: 110nm CMOS process with 1.2V transistors
Substrate thickness: 300um
Substrate doping: n-type, phosphorus, 2.5e12 cm^{-3}

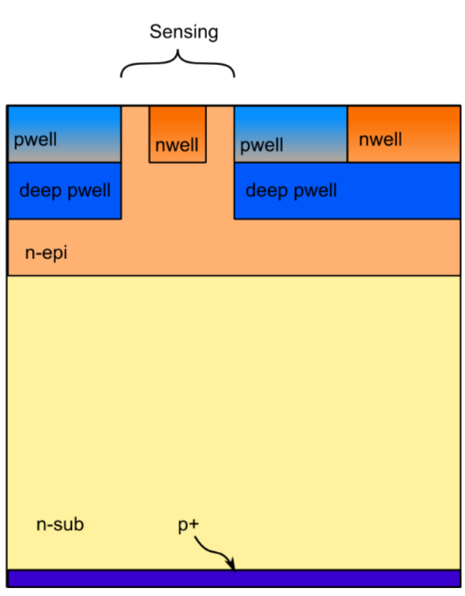


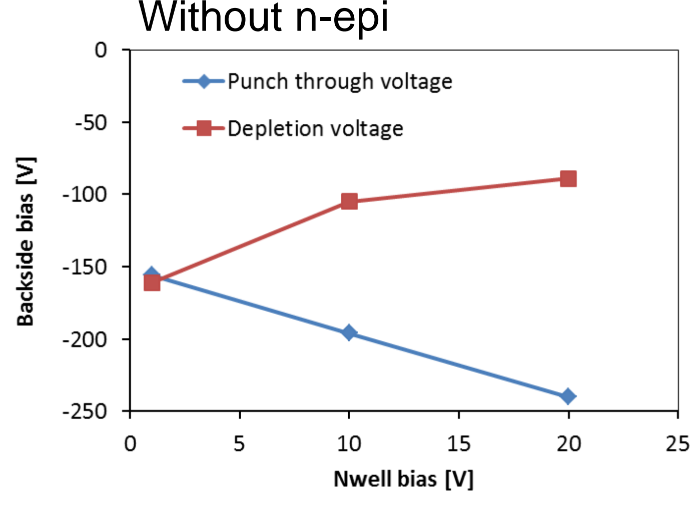
Sensor bias

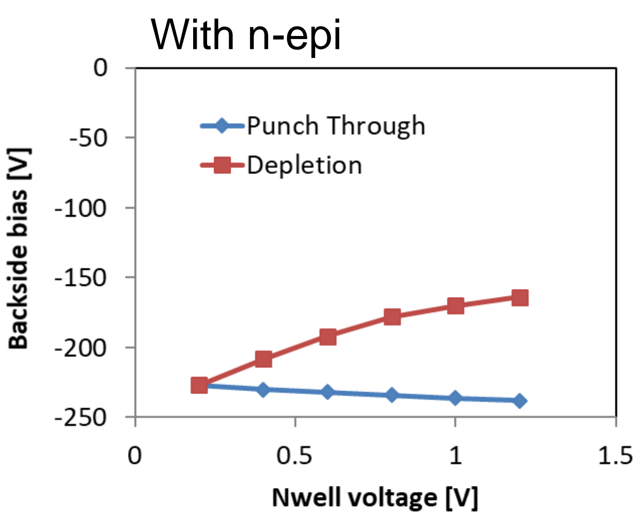
Backside bias:
- Large enough to reach **full depletion**
- Small enough to avoid **punch through**

Constraint: maximum n-well voltage is 1.2V (available low voltage transistors)

N-type epitaxial layer with doping larger than substrate: increased control of the potential barrier below deep pwell







Charge collection: 300um

n170_msh

Vbias= -200V

MIP incident in
3 different positions

DopingConcentration (cm

1.255e+18
6.535e+15
3.401e+13
-1.234e+12
-2.711e+14
-5.206e+16
-1.000e+19

1
2
3

W = 50um T = 300um

Ntop TotalCurrent(tran_n194_des)
Ntop TotalCurrent(tran_n195_des)
Ntop TotalCurrent(tran_n203_des)

Current [A]

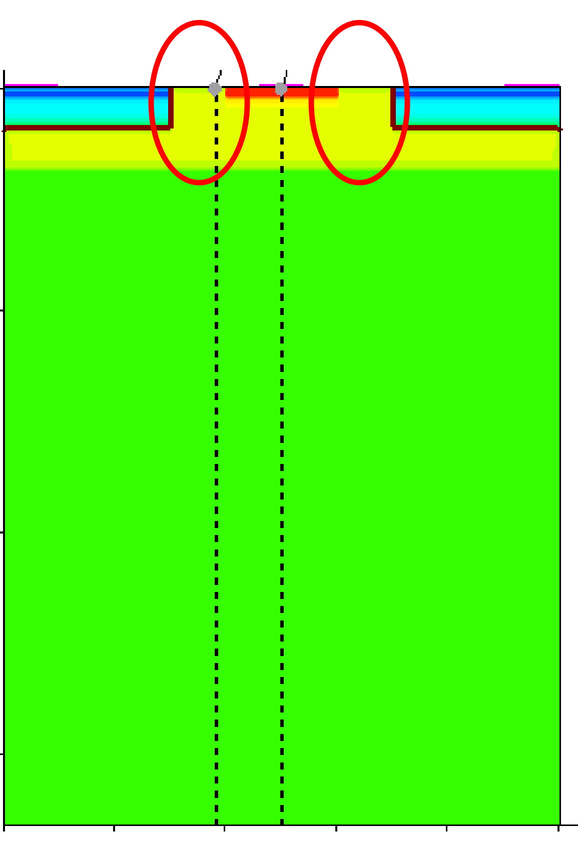
Time [s]

Pixel width 50um
Thickness 300um

< 30ns for complete collection

Collection node capacitance

Dominant contribution:
perimeter capacitance



Approximate perimeter cap:

0.25fF/um

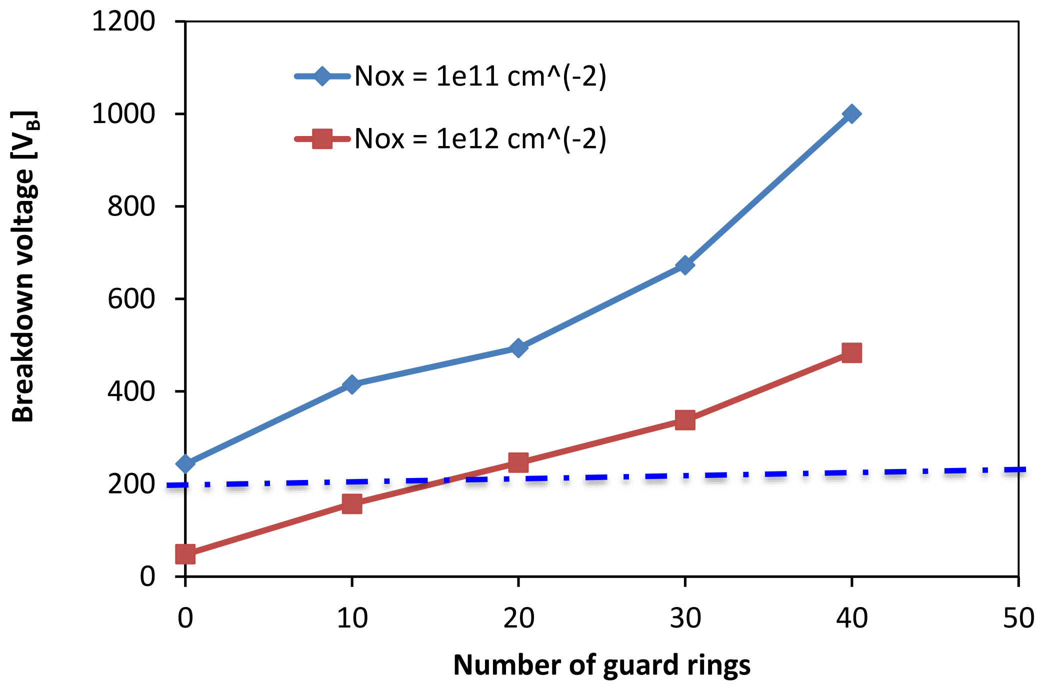
Capacitance for a 10um x 10um collection node = 10fF

Sensor periphery

- Nwell guard ring in the top plane
- Pwell ring termination structures in the back plane

Sensing
nwell
pwell
nwell
deep pwell
n-epi
Chip edge
p+
n-sub
passivation1
passivation2
metal
Pixel array
GR Pitch
GRW
FPW
Guard rings

Breakdown voltage simulations



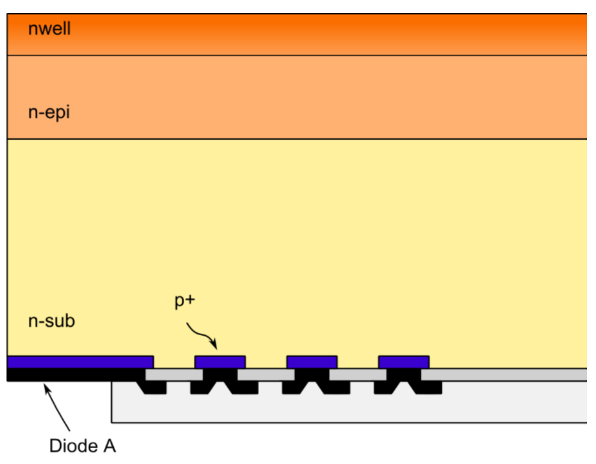
GR pitch = 6um

20 GR termination structure size = 120um

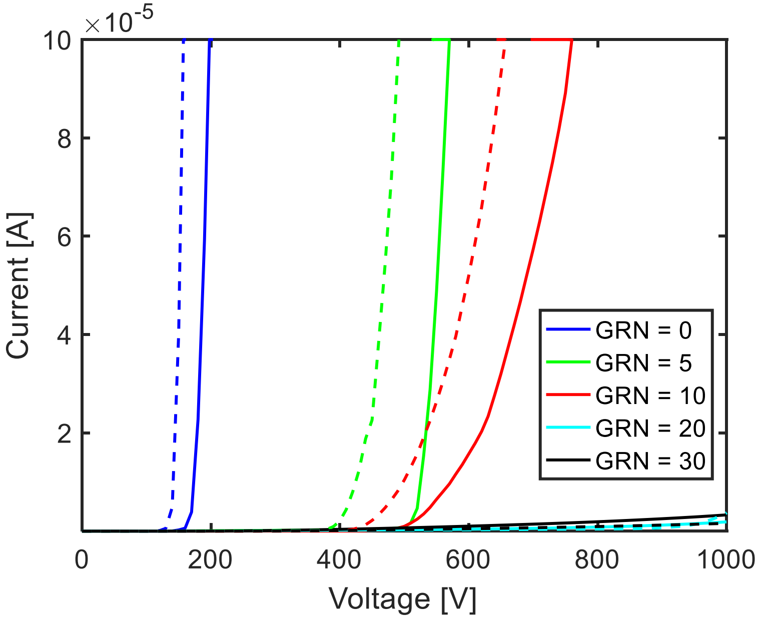
- P+ shallow junction: many guard rings are needed
- Simulations with low (10^{11} cm^{-3}) and high (10^{12} cm^{-3}) positive oxide charge density
- At least 20 GR are needed to bias the sensor at 200V in the worst case

Test structures: breakdown voltage

- Test diodes with different guard ring number (GRN)
- Breakdown voltage increases with GRN
- Test on unirradiated diodes and after 1Mrad irradiation (X-rays)
- Diodes with 20 and 30 guard rings have a breakdown voltage larger than 1000V



Continuous lines: unirradiated diodes
Dashed lines: irradiated diodes (1Mrad)



Test structure: pseudo-pixel array

- Small (8x8) pixel array in parallel without electronics with external readout. Pixel size 50um x 50um

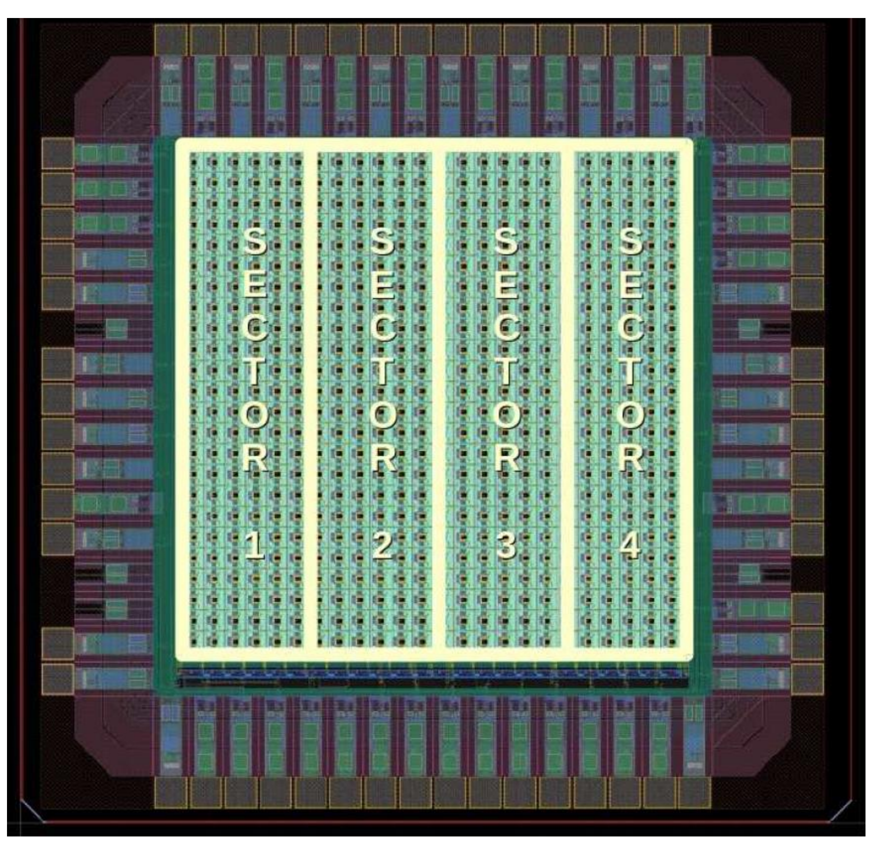
Vnwell
Vpwell=0V
V_{GR}
nwell
pwell
deep pwell
nwell
pwell
deep pwell
nwell
pwell
deep pwell
nwell
nwell
n-epi
n-sub
p+
Vbias

Test pixels dark current

- Dark current can be measured only if the sensor is depleted
- Strong depletion dependence on small applied nwell voltage

Array cross section

Pixel array



- Die area: 2×2 mm^2
- low voltage operation: 1.2 V
- matrix of 24×24 pixel units organized in 4 independent sectors
- 6 columns x 24 rows in each sector

Pixel schematic and layout

Reset
Cf
Preamp
Sensor
Cp
Charge Injection
Sample Baseline
Sample Signal
Buffer 1
Buffer 2
Buffer 1
Buffer 2
$C_{BASELINE}$
C_{SIGNAL}
Baseline
Signal

The front-end electronics

Pixel layout
ANALOG
Buffer1
Buffer2
Buffers
Preamp + Charge Inj + Baseline Regulator
Noise Inj
Buffer1
Buffer2
FFs
DIGITAL
50 µm
50 µm

- Both NMOS and PMOS transistors are used
- The electronics fits an area of 30 µm ×30 µm
- Digital in-pixel logic

Chip parameters

Parameter	Value
Analog gain	$\approx$130 mV/fC (2.1 mV/100 e^-)
	Transmission $\approx$ 370 μW
Sensor Cap	40 fF
Storage Cap	$\approx$ 70 fF (MIM CAPS)
Linearity Range	400 mV - 950 mV
Readout Speed	Up to 5 MHz
Other features	Internal Test Pulse
	Mask Mode
	Baseline Regulator
Shutter type	Snapshot Shutter
Readout Type	Correlated Double Sampling [3]

Array backside measurements - CV

$\times 10^{24}$

2
1.5
1
0.5
0

0 50 100 150 200

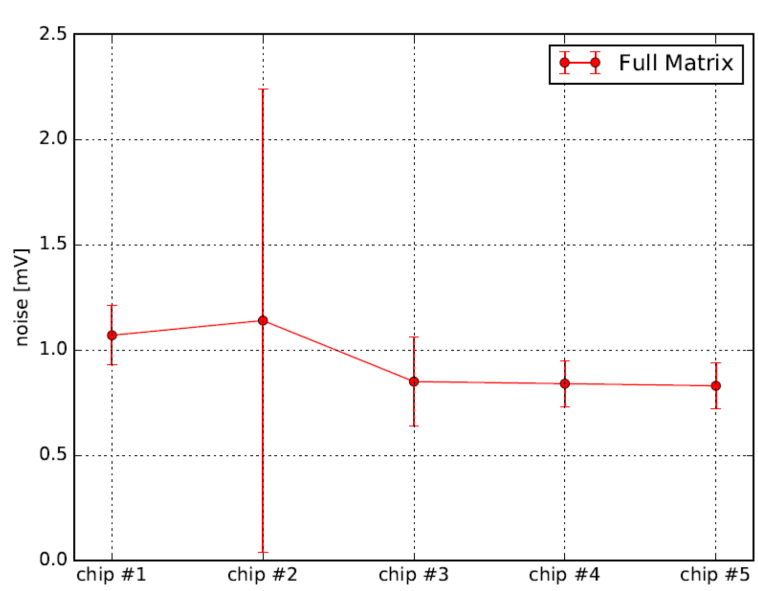
Voltage [V]

$1/C^2$ [F^{-2}]

Array1
Array2
Array3
Model (planar)

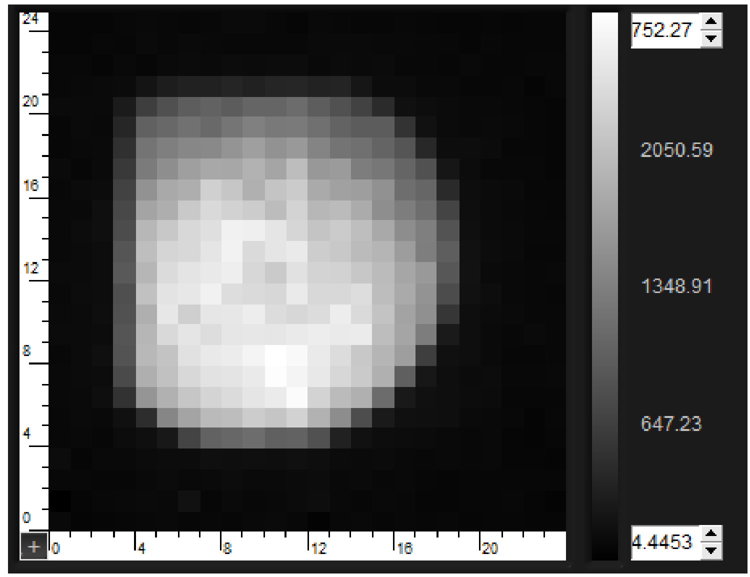
Doping 2.4 x 10^{12} cm^{-3} – same as wafer specification

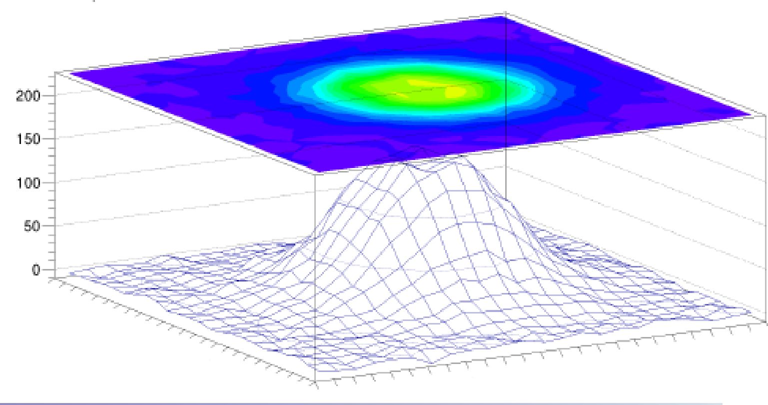
Pixel array characterization



Average noise ~ 1mV:
ENC < 50e- rms at RT

IR laser pulse intensity map





Measurements with ^{55}Fe

Cluster signal, Channel 0

csig	
Entries	3031
Mean	425.9
RMS	54.67
χ^2 / ndf	154.6 / 50
Constant	299.2 ± 7.4
Mean	432.9 ± 0.7
Sigma	38.36 ± 0.62

ADC

Cluster signal, Channel 1

csig	
Entries	4343
Mean	419.4
RMS	54.18
χ^2 / ndf	217.8 / 49
Constant	429.5 ± 8.9
Mean	425.8 ± 0.6
Sigma	38.32 ± 0.53

ADC

- Expected energy for the ^{55}Fe peak: 5.9 keV (1650 e−)
- Standard deviation: 520 eV at RT
- Measured energy value: 420 counts used to estimate analog gain (117mV/fC)

SEED: on-going and future plans

- Measurements on more chips and test structures (information on tech. variability)
- Radiation damage (IEL and NIEL)
- Charge collection speed (laser)

- New run with different substrate thickness:
  - 100 – 150um: particle tracking
  - 500um: X-ray imaging