SuperB IFR: outline of the IFR DAQ electronics: estimates on bandwidth requirements

Outline of readout electronics for the SuperB IFR detector : TIMING mode readout

SuperB-IFR numerology:

- Barrel: N_Barrel = 3600
- EndCaps: N_EndCap = 2400 + 2400

(quoting G. Cibinetto)

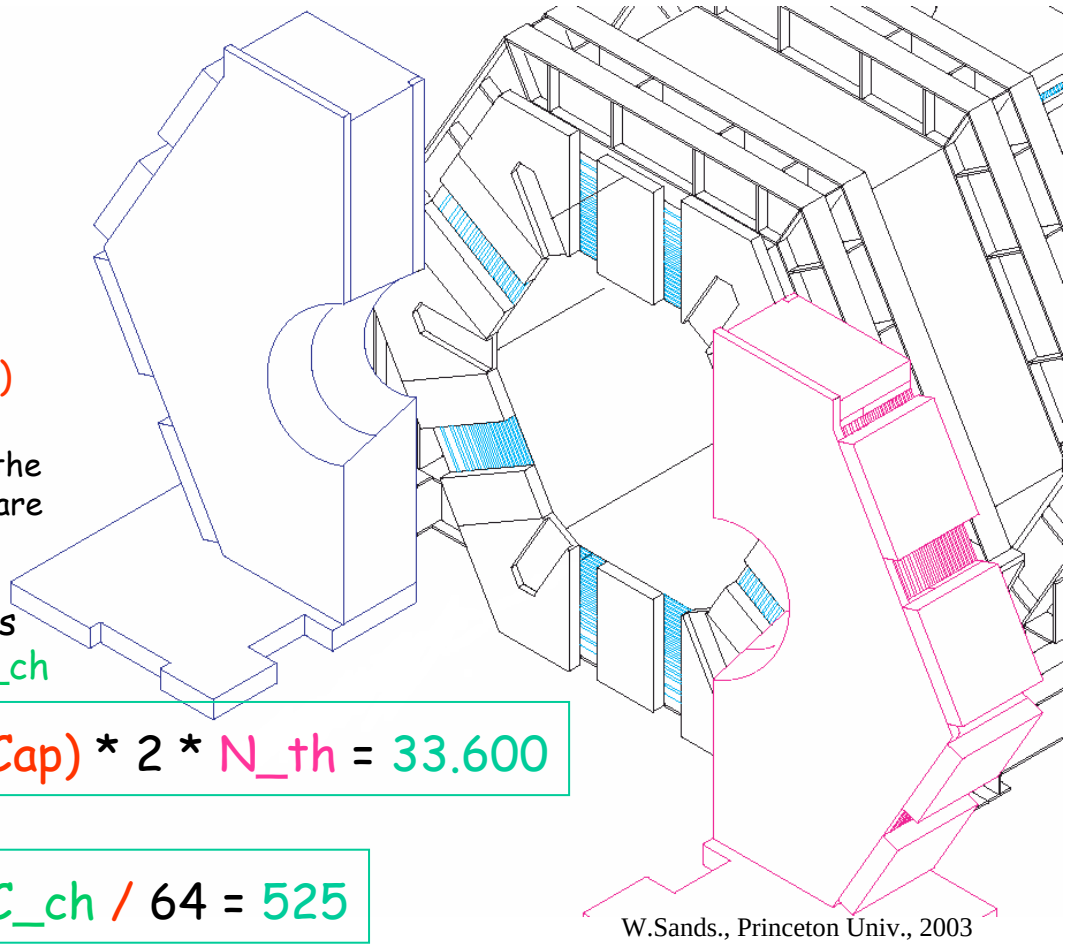
Assuming:

- readout in TIMING mode with N_th (=2) thresholds:

both the high threshold (2.5 p.e. for instance) and the low threshold (1.5 p.e. for instance) crossing times are acquired by the F.E., the second threshold crossing validating the first for better noise rejection.

-> each scintillator is readout at both ends

-> total number of TDC channels: N_TDC_ch



W.Sands., Princeton Univ., 2003

$$N\_TDC\_ch = (N\_Barrel + N\_EndCap) * 2 * N\_th = 33.600$$

$$N\_TDC\_board = N\_TDC\_ch / 64 = 525$$

Hopefully the tests on the prototype will show that it will be possible to keep:

N_th = 1

but in the meantime it is better to consider the worst option

!!! Multihit TDC ASICs currently available assume a reference clock of 40MHz meanwhile the latest document edited by D.Breton and U. Marconi assumes a 56.25MHz clock: it is an issue !!!

Outline of readout electronics for the SuperB IFR detector : TIMING mode readout

SuperB-IFR numerology:

"Physics" rate : **500kHz**/channel, in the hottest region, arising from:

- particle rate : O(100Hz) / cm^2 (including background)
- dimensions of a detector element : < 400cm x 4cm (thickness 20mm)

(quoting R.Calabrese, W.Baldini, G.Cibinetto)

"Dark count" rate : **for a 1mm^2 SiPM by FBK**:

(quoting R.Malaguti, L.Milano test results in Ferrara)

@ 0.5pe threshold

- @ 25°C, 34.4V: ≈ 360kHz
- @ 5°C, 33.8V: ≈ 128kHz

@ 2.5pe threshold

- @ 25°C, 35V: ≈ 20kHz
- @ 5°C, 34V: ≈ 6.3kHz

!!! The "dark count" rate scales with the sensor's area and we don't know yet which would be the final area of the sensor of choice (a 4mm^2 is also being considered)

!!! We need to have, on each processing channel, one comparator with a low threshold (0.5pe? 1.5pe? Only prototype test will tell) → it's TDC input will see the highest rate.

Let's consider a "Hit" rate of:

Hit_rate = physics_rate + dark count_rate ≤ 1MHz per TDC input !!!

Proposal of readout electronics for the SuperB IFR detector : TIMING mode readout

SuperB-IFR numerology:

A "Hit" rate of 1MHz per channel is compatible with the input and output rate of the TDC_GPX or the CERN HPTDC

BUT:

if we don't do L1 trigger matching on board

if we do L1 trigger matching on board

NEXT PAGE

Assuming that:

- "Hits" are packed into **FRAMES collecting all hits recorded in a time-slice of, say, 6.4us**
- Each FRAME contains:
  - Header = Board ID + Frame ID (allows to reconstruct ABSOLUTE timing for hit records) : 12 Byte
  - Channel ID + hit timing information RELATIVE to beginning of frame : 4 Byte per Hit
  - Trailer = WordCount + CRC : 4 Byte
- On each TDC half of the channels has a 1MHz input rate and half has a 500KHz input rate

  → we can expect, for a 64 channel TDC card, an **average** frame size of:

  <Frame size> = 12 + (6.4 hit * 32 + 3.2 hit * 32) * 4 + 4 ≈ 12 + 320 * 4 + 4 ≈ **1.3kB**

A.C.R. 2009-02-13

Each 64 channel TDC card would produce a sustained stream of (on average) :

<Bandwidth per 64ch TDC> = 1.3kB / 6.4us ≈ **200MB/s**

→ it would need a 5Gbps link to the downstream buffers !!!

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Proposal of readout electronics for the SuperB IFR detector : TIMING mode readout

SuperB-IFR numerology:

From previous slide

if we do L1 trigger matching on board

Assumptions on L1 trigger rate and window:

- L1 trigger at fixed latency with respect to the event (our preferred option): latency in the order of 10us
- L1 trigger rate : 150KHz (*)
- L1 trigger window : 1us (*)

(*) (quoting "Electronics, trigger and DAQ for SuperB.", D. Breton, U.Marconi, Feb. 11 2009)

NOTE: **if a fixed latency trigger is adopted** it might be convenient to use the HPTDC ASICs which have internal trigger matching resources instead of the TDC-GPX which would require intense parallel processing to provide primary storage and perform trigger matching off-chip.

To roughly estimate the "trigger matched" output bandwidth from a 64 channel TDC card one could assume a reduction factor of: (1/150KHz) / 1us = 6.(6)

Each 64 channel TDC card would produce a "TRIGGER MATCHED" sustained stream of (on average) :

<Bandwidth per 64ch TDC> = 200MB/s / 6.(6) ≈ 30MB/s

(it would be less if we could implement:

- D.Breton's scheme to handle the "overlap" of trigger requested data
- the BhaBha veto)

→ **a 1Gbps link to the downstream buffer would be adequate**

A.C.R. 2009-02-13

Proposal of readout electronics for the SuperB IFR detector : BINARY mode readout

SuperB-IFR numerology:

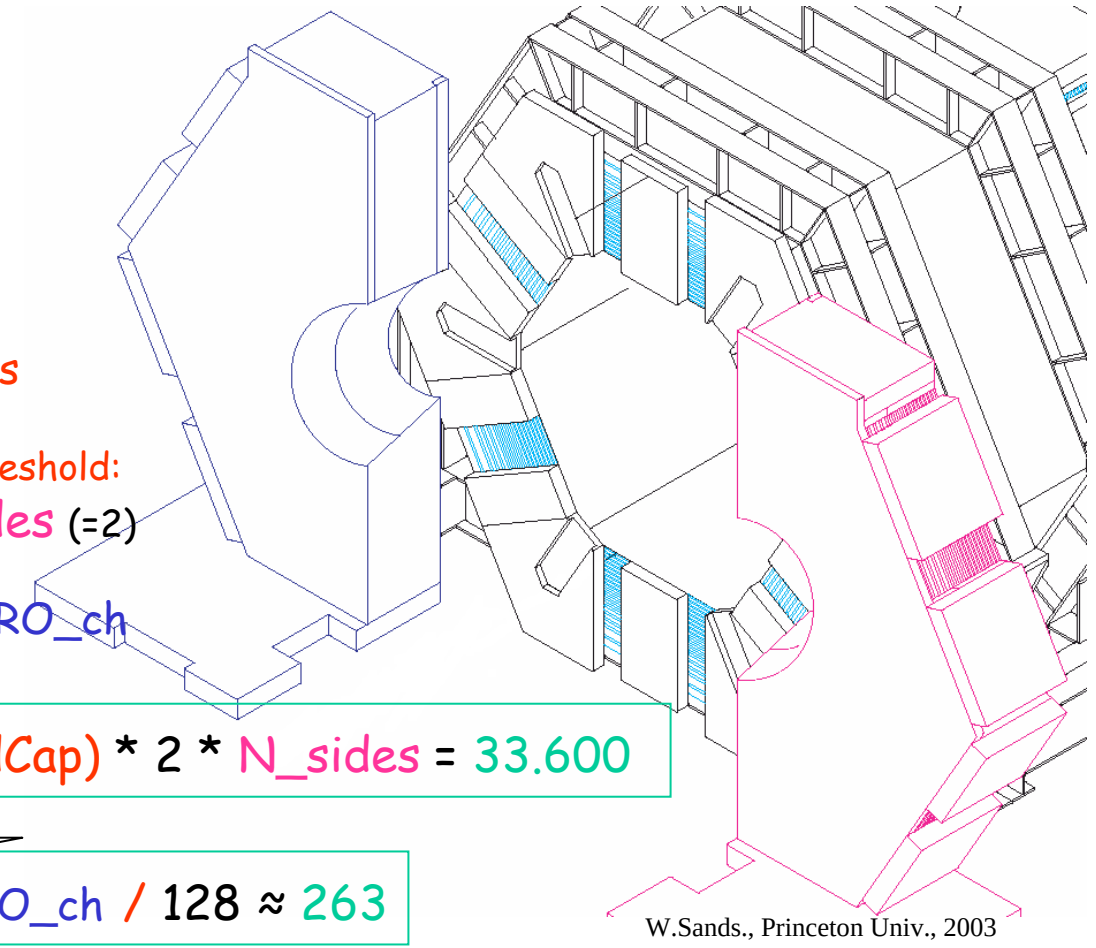
- Barrel: N_Barrel = 3600
- EndCaps: N_EndCap = 2400 + 2400

(quoting G. Cibinetto)

Assuming:

- the number of (thin) scintillators doubles (for X-Y readout; it's a coarse estimate)
- readout in BINARY mode with single threshold:
- each scintillator is readout from N_sides (=2) ends

-> total number of BiRO channels: N_BiRO_ch



W.Sands., Princeton Univ., 2003

$$N\_BiRO\_ch = (N\_Barrel + N\_EndCap) * 2 * N\_sides = 33.600$$

$$N\_BiRO\_Board = N\_BiRO\_ch / 128 \approx 263$$

It is possible that construction / dead space constraints will result in :

N_sides = 1

at least for part of the scintillators but let's now consider the full number

Proposal of readout electronics for the SuperB IFR detector : BINARY mode readout

SuperB-IFR numerology:

"Physics" rate : **500kHz**/channel, in the hottest region, arising from:

- particle rate : O(100Hz) / cm^2 (including background)
- dimensions of a detector element : < 400cm x 4cm (thickness 20mm)

(quoting R.Calabrese, W.Baldini, G.Cibinetto)

"Dark count" rate : **for a 1mm^2 SiPM by FBK**:

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@ 0.5pe threshold

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- @ 5°C, 33.8V: ≈ 128kHz

@ 2.5pe threshold

- @ 25°C, 35V: ≈ 20kHz
- @ 5°C, 34V: ≈ 6.3kHz

!!! The "dark count" rate scales with the sensor's area and we don't know yet which would be the final area of the sensor of choice (a 4mm^2 is also being considered)

!!! We need to have, on each processing channel, just one comparator with a 2.5pe threshold

→ The dark count rate @ 2.5pe threshold is just a fraction of the physics rate

Let's consider a "Hit" rate of:

Hit_rate = physics_rate + dark count_rate ≈ 600kHz per BiRO input

Proposal of readout electronics for the SuperB IFR detector : BINARY mode readout

SuperB-IFR numerology:

A Hit_rate of 600kHz per channel will be processed by an FPGA which will sample the input pulses and provide temporary storage for the samples

LET's ASSUME:

- 20ns minimum pulse width from the Front End discriminators → dead time of 1.2% for a 600kHz rate
- FPGA sampling clock of 56.25MHz

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if we don't do L1 trigger matching on board ← SO: → if we do L1 trigger matching on board

NEXT PAGE

Assuming that:

- "Hits" are packed into **FRAMES collecting, say, 256 samples of all 128 inputs corresponding to a time-slice of** ≈ 4.55us
- Each FRAME contains:
  - Header = Board ID + Frame ID (allows to reconstruct ABSOLUTE timing for hit records) : 12 Byte
  - Channel ID + Sample ID for which the "Hit" was found : 2 Byte per Hit

  (**this implies that the FPGA performs ZERO SUPPRESSION: only address of active channels for each sample are recorded: to be tested**)
  - Trailer = WordCount + CRC : 4 Byte
- We can expect, for a 128 channel BiRO Front End Card, an **average** frame size of:

  <Frame size> = 12 + <2.73> hit * 128 * 2 + 4 ≈ 12 + 350 * 2 + 4 ≈ **0.72kB**

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128 channel BiRO Front End Card would produce a sustained stream of (on average) :

<Bandwidth per 128ch FE_BiRO> = 0.72kB / 4.55us ≈ **160MB/s**

→ it would need a 2.5Gbps link to the downstream buffers !!!

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Proposal of readout electronics for the SuperB IFR detector : BINARY mode readout

SuperB-IFR numerology:

From previous slide

if we do L1 trigger matching on board

Assumptions on L1 trigger rate and window:

- L1 trigger at fixed latency with respect to the event (our preferred option): latency in the order of 10us
- L1 trigger rate : 150kHz (*)
- L1 trigger window : 1us (*)

(*) (quoting "Electronics, trigger and DAQ for SuperB.", D. Breton, U.Marconi, Feb. 11 2009)

To roughly estimate the "trigger matched" output bandwidth from a 128 channel FE_BiRO one could assume a reduction factor of: (1/150KHz) / 1us = 6.(6)

Each 128 channel FE_BiRO card would produce a "TRIGGER MATCHED" sustained stream of (on average) :

<Bandwidth per 128ch FE_Biro> = 160MB/s / 6.(6) ≈ 24MB/s

(it would be less if we could implement:

- D.Breton's scheme to handle the "overlap" of trigger requested data
- the BhaBha veto)

→ **a 1Gbps link to the downstream buffer would be adequate**

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Proposal of readout electronics for the SuperB IFR detector : summarizing

TIMING mode readout

number of TDC_board ≈ 525

Channel per board = 64

Bandwidth per board

raw 200MB/s

trigger matched 30MB/s

BINARY mode readout

number of BiRO_Board ≈ 263

Channel per board = 128

Bandwidth per board

raw 160MB/s

trigger matched 24MB/s

ensured that the on-board FPGA can performs the on-line Zero Suppression mentioned above, the binary mode readout FEE should be less expensive than the timing mode readout of a factor ≈ 4

but

- input deadtime ≈ 1.2%
- detector construction more complex and with more dead areas due to fiber routing