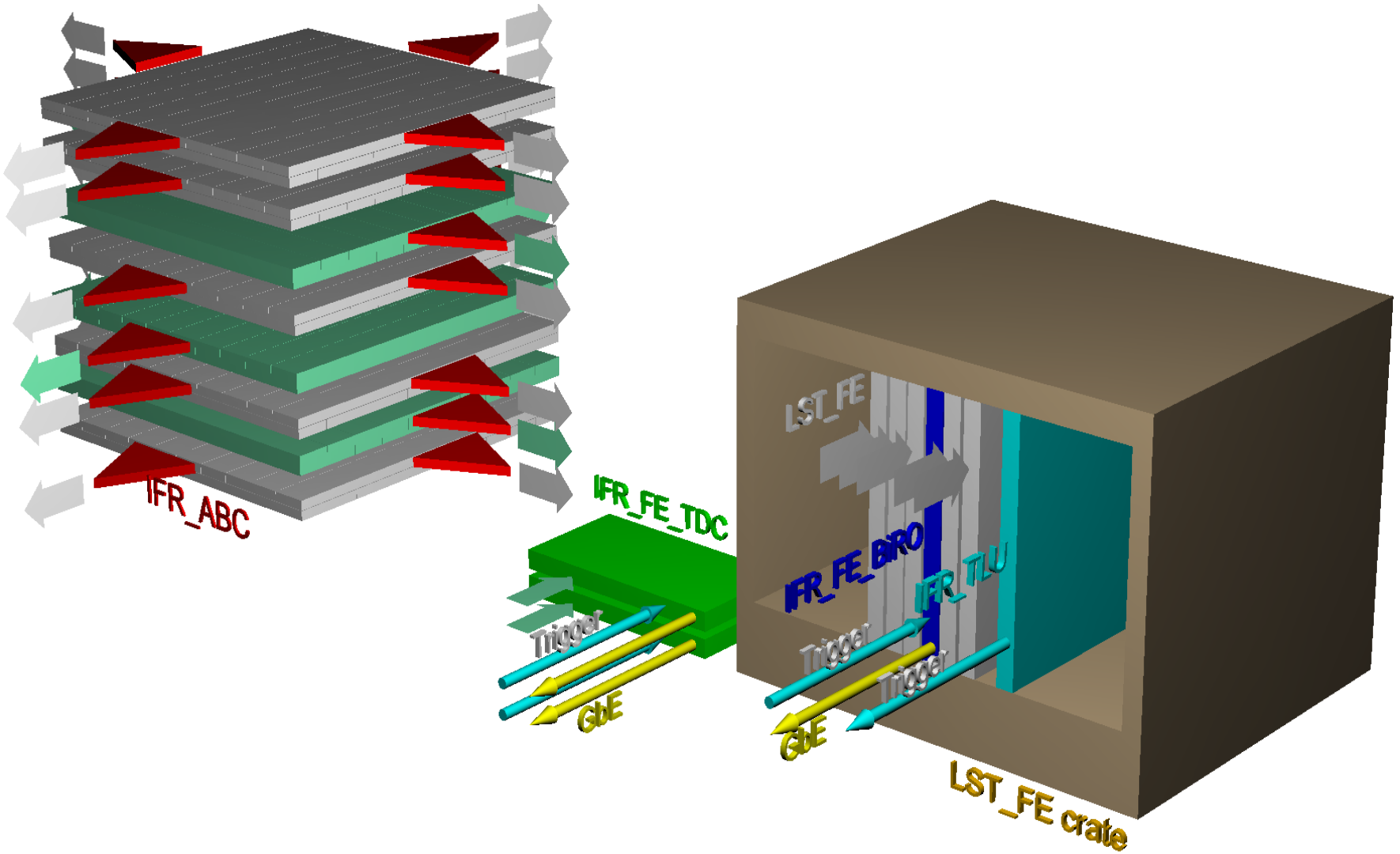


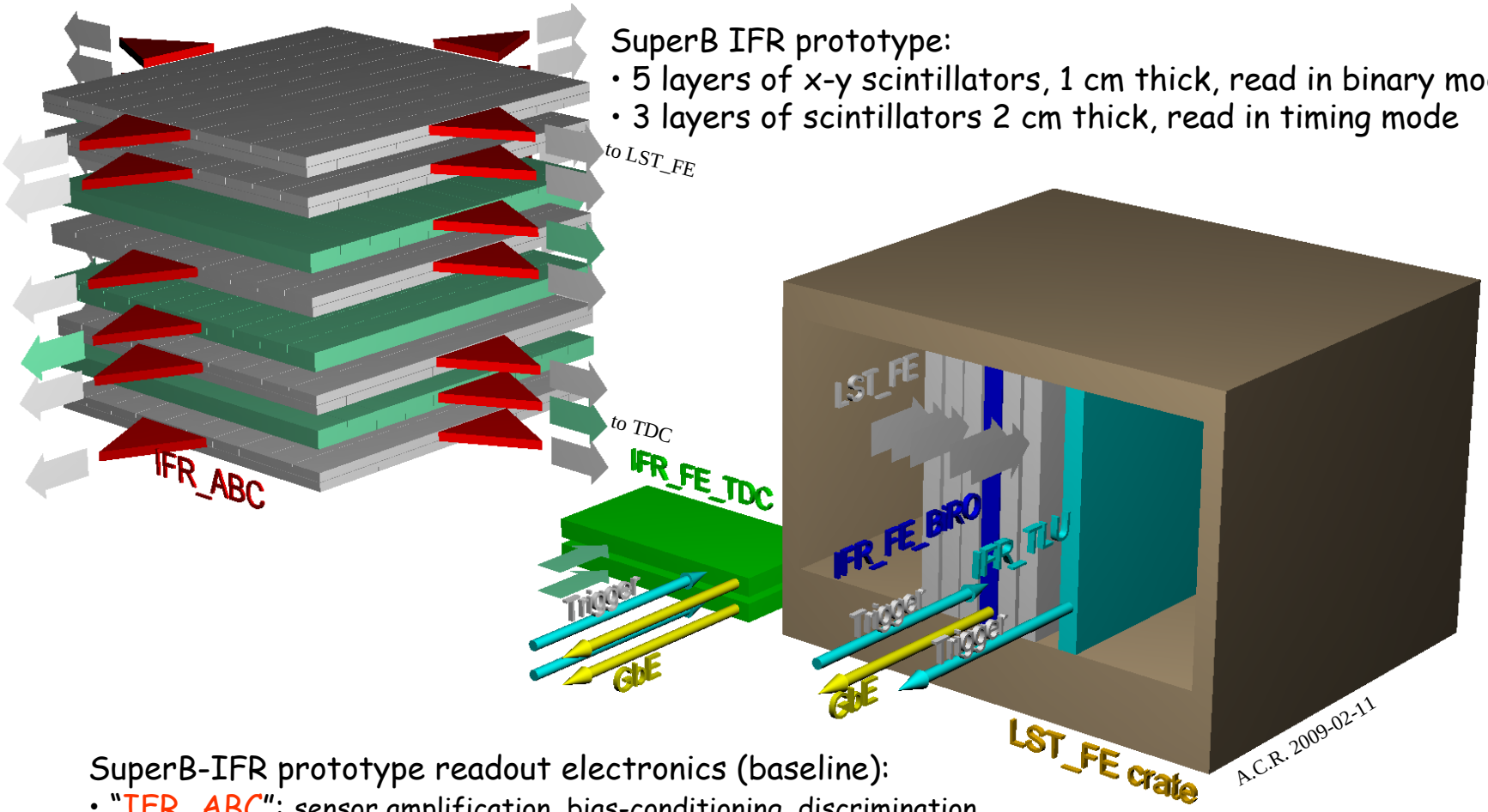
SuperB IFR: outline of the IFR prototype electronics

Summary

- Outline of readout electronics for the SuperB IFR prototype
- Status

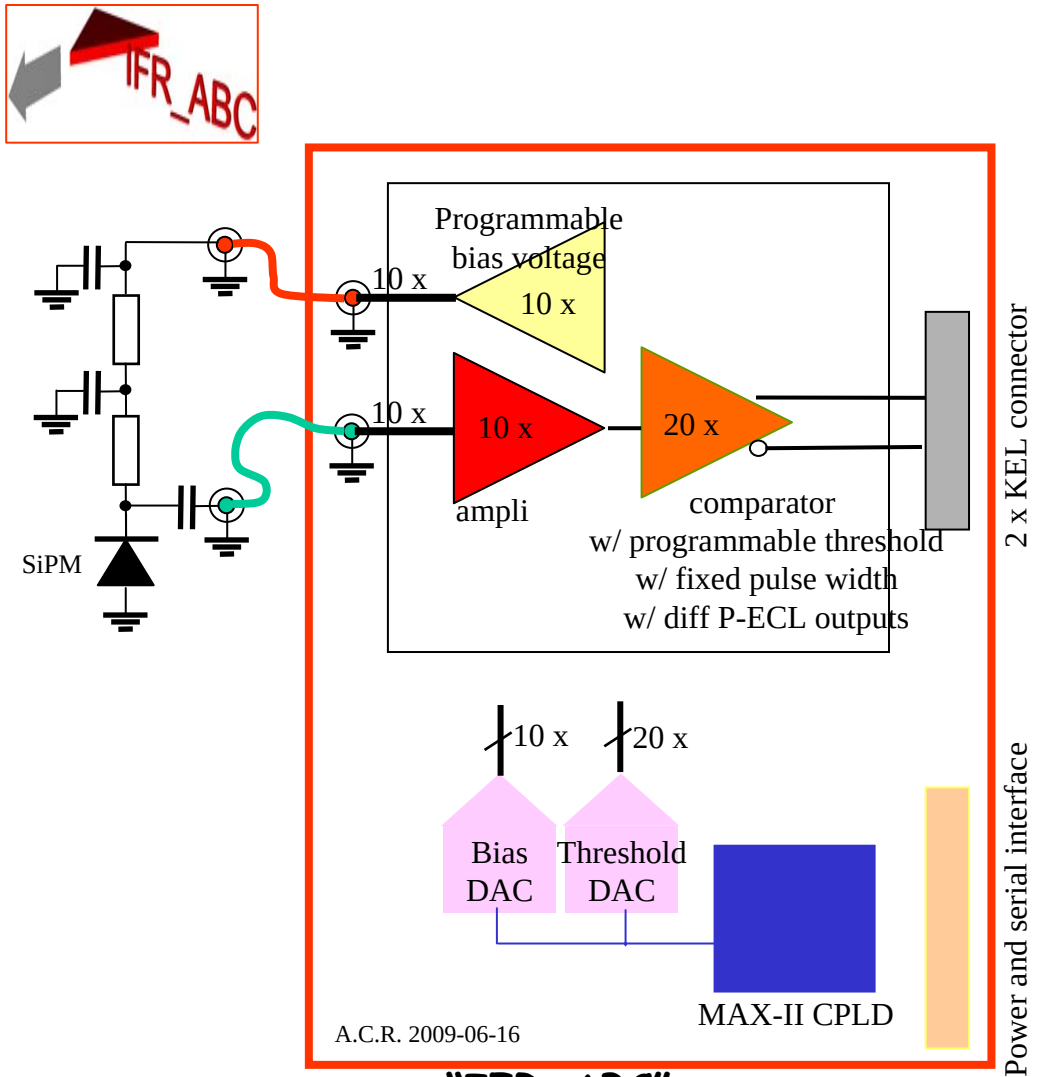
Outline of readout electronics for the SuperB IFR prototype

SuperB IFR prototype:
- 5 layers of x-y scintillators, 1 cm thick, read in binary mode
- 3 layers of scintillators 2 cm thick, read in timing mode



SuperB-IFR prototype readout electronics (baseline):
- "IFR_ABC": sensor amplification, bias-conditioning, discrimination
- "LST-FE": front end card used in BaBar IFR equipped with PECL receiver daughter cards. It samples status of inputs @ 80MHz and stores it, pending the trigger request
- "IFR_FE_BiRO": collects data from LST-FE cards upon trigger request and sends it to DAQ PC (via GbE)
- "IFR_FE_TDC": a multi-hit TDC design based on commercially available TDC chips with trigger interface and GbE output link to the DAQ PC
- "IFR_TLU": a module (Trigger Logic Unit) to generate a fixed latency trigger based on primitives from the IFR prototype itself or from external sources

Outline of readout electronics for the SuperB IFR prototype



Outline of the **"IFR_ABC"** card
(Amplifier, Bias, Comparator)

"IFR_ABC" card features:

- ampli: two stage w/discrete components: either 2xTHS4303 (2.6$ea) or BGA2748(0.42$ea) + BGA2716(0.33$ea)
- discri: ADCMP562BRQ (dual, 2.7$ea)

For the SuperB IFR prototype it is foreseen to use two comparators at different thresholds (2.5 pe and 1.5 pe for instance) for each sensor

- DAC: MAX5592 (10bit, octal, 5.24$ea)
- CPLD: ALTERA EPM1270GT144C5N (22$ ea)
- signal connector compatible with BaBar IFR signal cables (re-usable): KEL 8831E-034-170LD (3€ea for the PCB-mount+ 6.5€ea for the cable mount)

Total **"IFR_ABC"** needed for prototype readout :

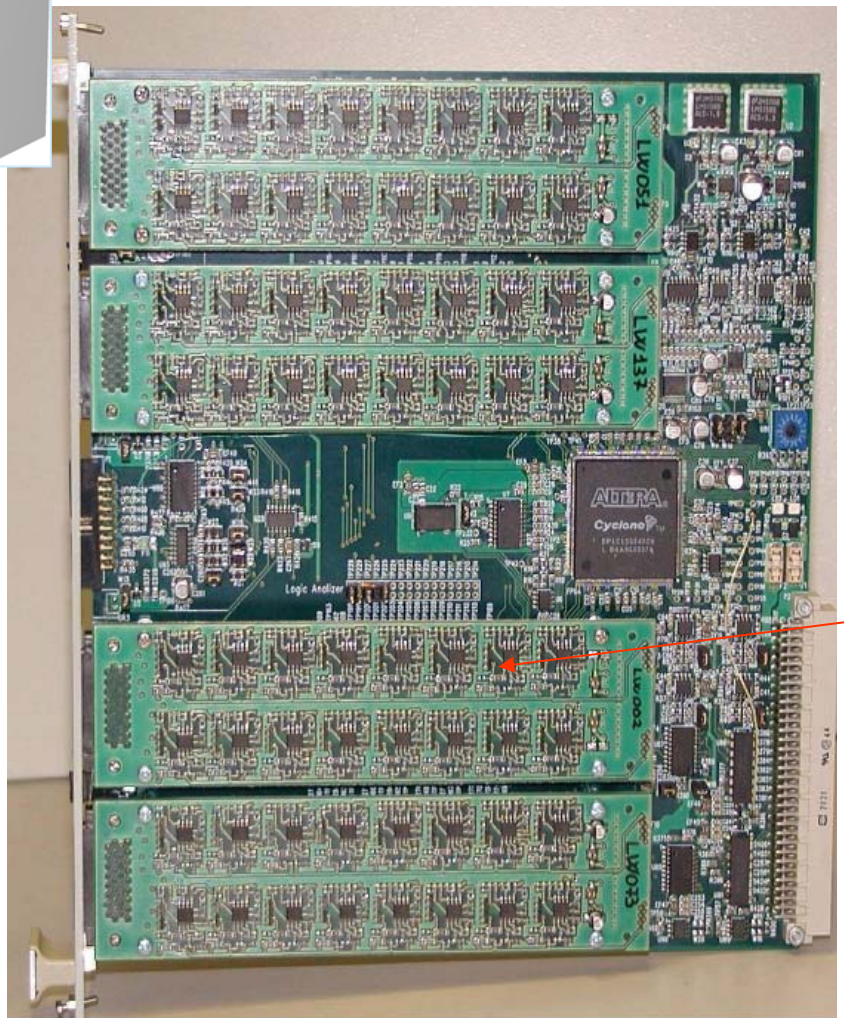
2 for X view of each of 5 BiRO planes (readout at both end of scintillator) +

2 for Y view of each of 5 BiRO planes (readout at both end of scintillator) +

2 for each of 3 planes read with TDCs

TOTAL "IFR_ABC" cards: 26

Outline of readout electronics for the SuperB IFR prototype



"LST_FE" card features:

• designed for the LST based IFR at BaBar. It sampled and stored the 64 inputs (divided among 4 daughter cards with 16 inputs each) for the BaBar trigger latency.

The LST_FE already provides 4 Fast-OR output signals, one per daughter card, which can be used for stand-alone triggering of the SuperB-IFR prototype (one daughter card = one side of one plane of thin scintillators)

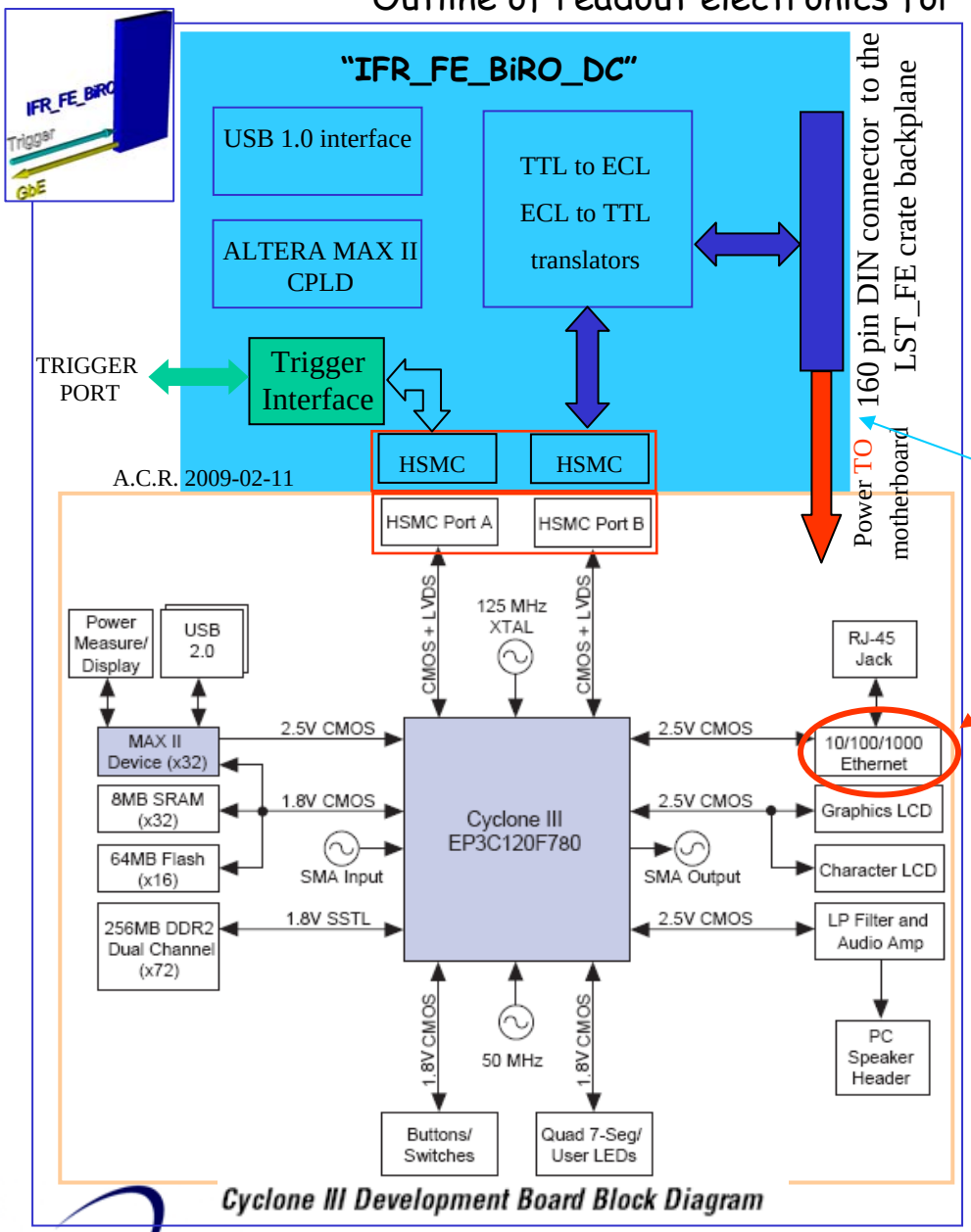
• to be used for the SuperB IFR prototype readout it needs replacement of present daughter cards with new daughter cards **"LST_FE_pECL_Rx"** which would:

a) translate the PECL differential inputs into TTL using, for instance, MC100LVELT23D dual PECL/LVTTL translators (2.3 €ea)

b) provide signal connectors compatible with BaBar IFR signal cables: KEL 8831E-034-170LD (3€ea for the PCB-mount+ 6.5€ea for the cable mount)

Total "LST_FE" needed for prototype readout in binary mode: 5 (one per BiRO plane)

Outline of readout electronics for the SuperB IFR prototype



Outline of the "IFR_FE_BiRO" card

"IFR_FE_BiRO" card features:

• motherboard: it is based on an ALTERA development board for the Cyclone III FPGA (**DK-DEV-3C120N, cost 1000 €**). The Cyclone III FPGA on board has enough memory resources to buffer the data collected from the LST_FE boards. Data requested by a trigger is sent over the GbE link featured by the development board.

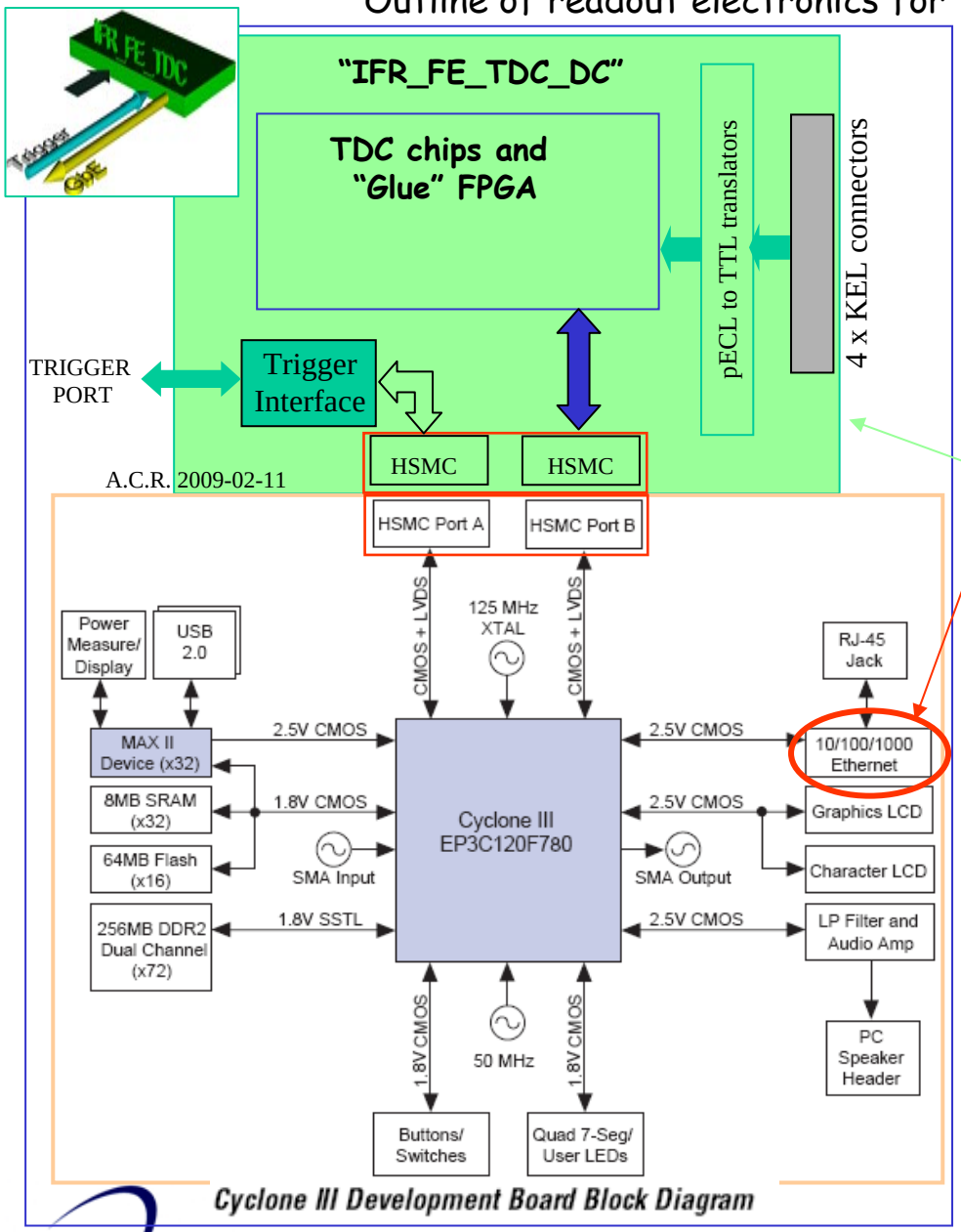
• daughter card (**"IFR_FE_BiRO_DC"**): it provides mostly level translators and connections to:

- the LST_FE crate backplane
- the Trigger Logic Unit
- the motherboard through the HSMC connectors (SAMTEC ASP-122952-01)

Total **"IFR_FE_BiRO_DC"** needed for the prototype readout: 2 (one for the "IFR_FE_BiRO", one for the "IFR_TLU")

The LST_FE and the IFR_FE_BiRO cards are hosted in one of the LST_FE crates recovered from BaBar (**designed by INFN Genova for the LST-based IFR readout**).
The LST_FE crate has just arrived in Ferrara

Outline of readout electronics for the SuperB IFR prototype



Outline of the "IFR_FE_TDC" card

"IFR_FE_TDC" card features:

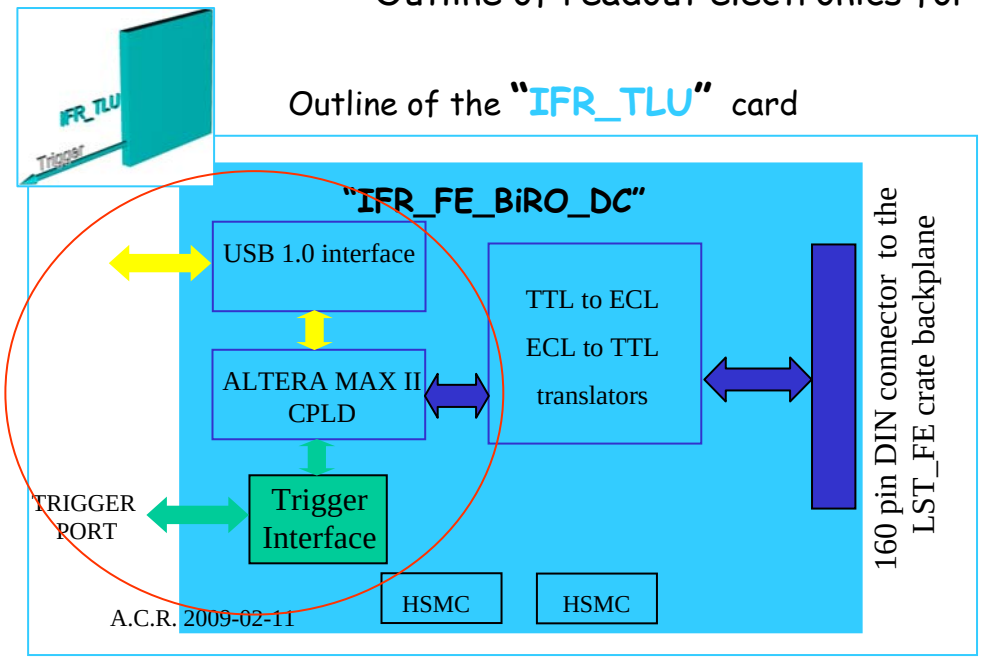
• motherboard: it is based on an ALTERA development board for the Cyclone III FPGA (**DK-DEV-3C120N, cost 1000 €**). The Cyclone III FPGA on board continuously collects data from the **"IFR_FE_TDC_DC"** daughter card and stores it in a circular buffer pending a trigger request. Data requested by a trigger is sent over the on-board GbE link.

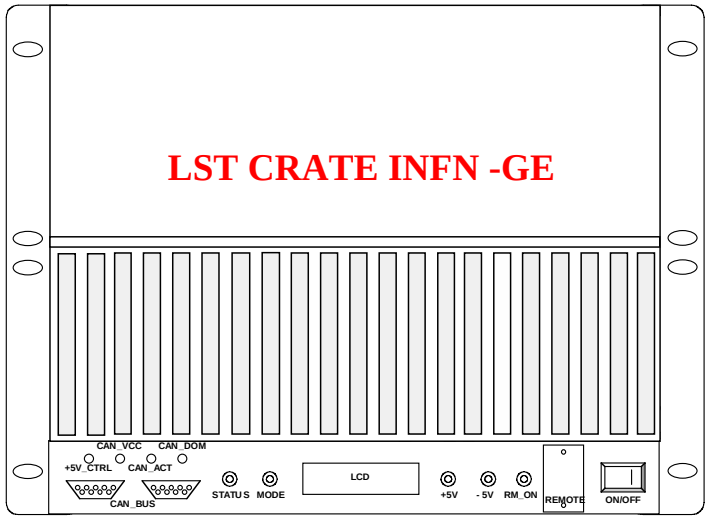
• daughter card (**"IFR_FE_TDC_DC"**): it features commercially available TDCs (8 x ACAM TDC-GPX as a baseline) to handle at least 64 channels per board. An on-board FPGA configures the TDC chips, provides the primary buffers into which dat is stored pending the trigger request and performs transfer of "trigger matched data" through a FIFO-buffered output port towards the motherboard.

Total "IFR_FE_TDC" needed for prototype readout : 4 (assuming timing measurement with double threshold)

The "IFR_FE_TDC" is not strictly necessary for the prototype readout; it is R&D toward the Front End Electronics to be included in the TDR; in the end the final "IFR_FE_TDC" will be built on a single board. A back-up solution foresees the use of a CAEN V1290A VME TDC

Outline of readout electronics for the SuperB IFR prototype





Layout of the BaBar LST crate

"IFR_TLU" card features:

• **it is simply the "IFR_FE_BiRO_DC"** (plugged in a specific location of the LST_FE backplane) in which the section based on the ALTERA MAX-II CPLD is activated.

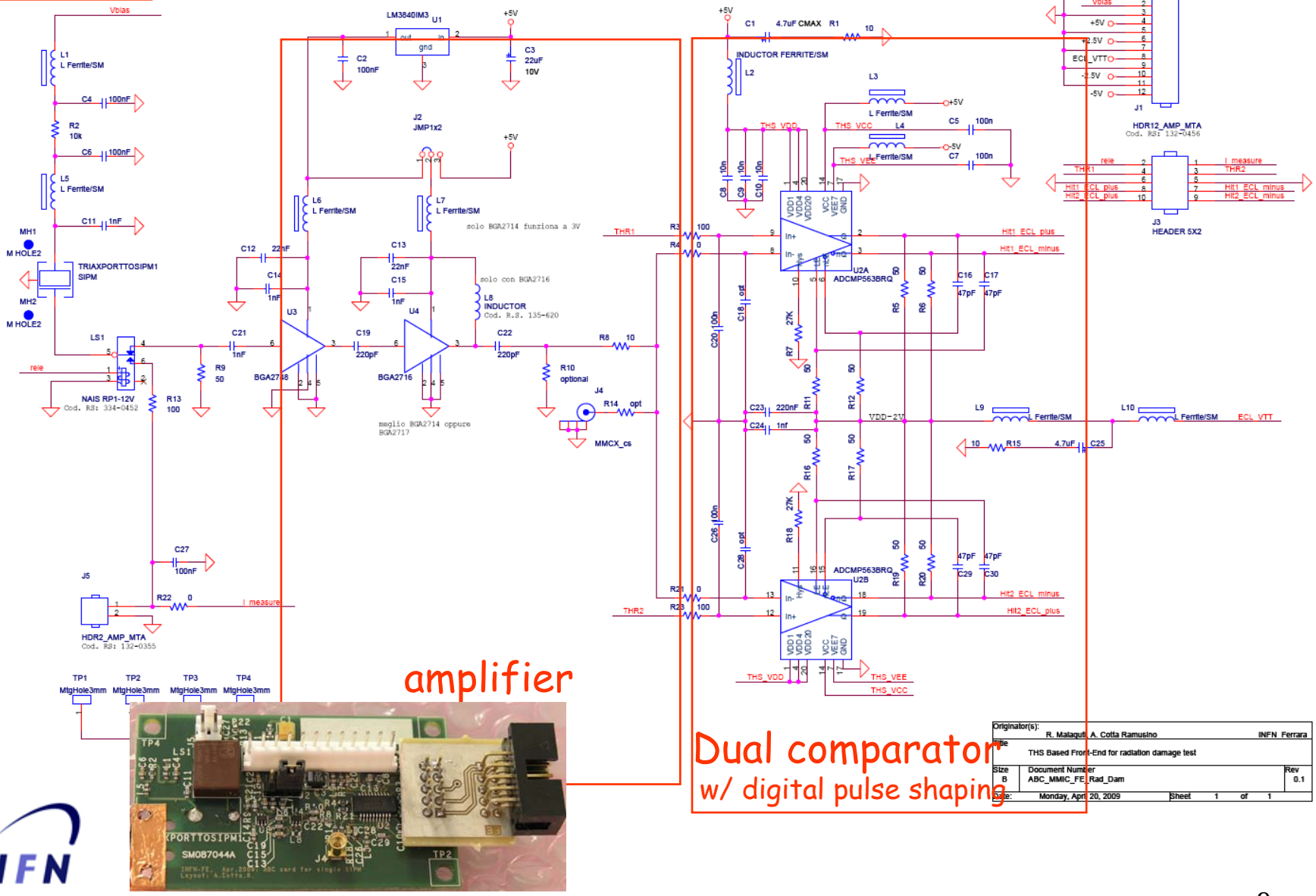
The CPLD performs programmable (via USB 1.0) combinatorial functions on the "Fast-OR" signals coming from the "LST_FE" cards to generate the trigger requests to the DAQ.

the "IFR_TLU" provides level translators and connections to:

- the LST_FE crate backplane
- the Trigger Logic Unit I/o port (which includes an Open Collector "Busy" Line driven by the FE cards)
- additional inputs for external trigger sources

Outline of readout electronics for the SuperB IFR prototype

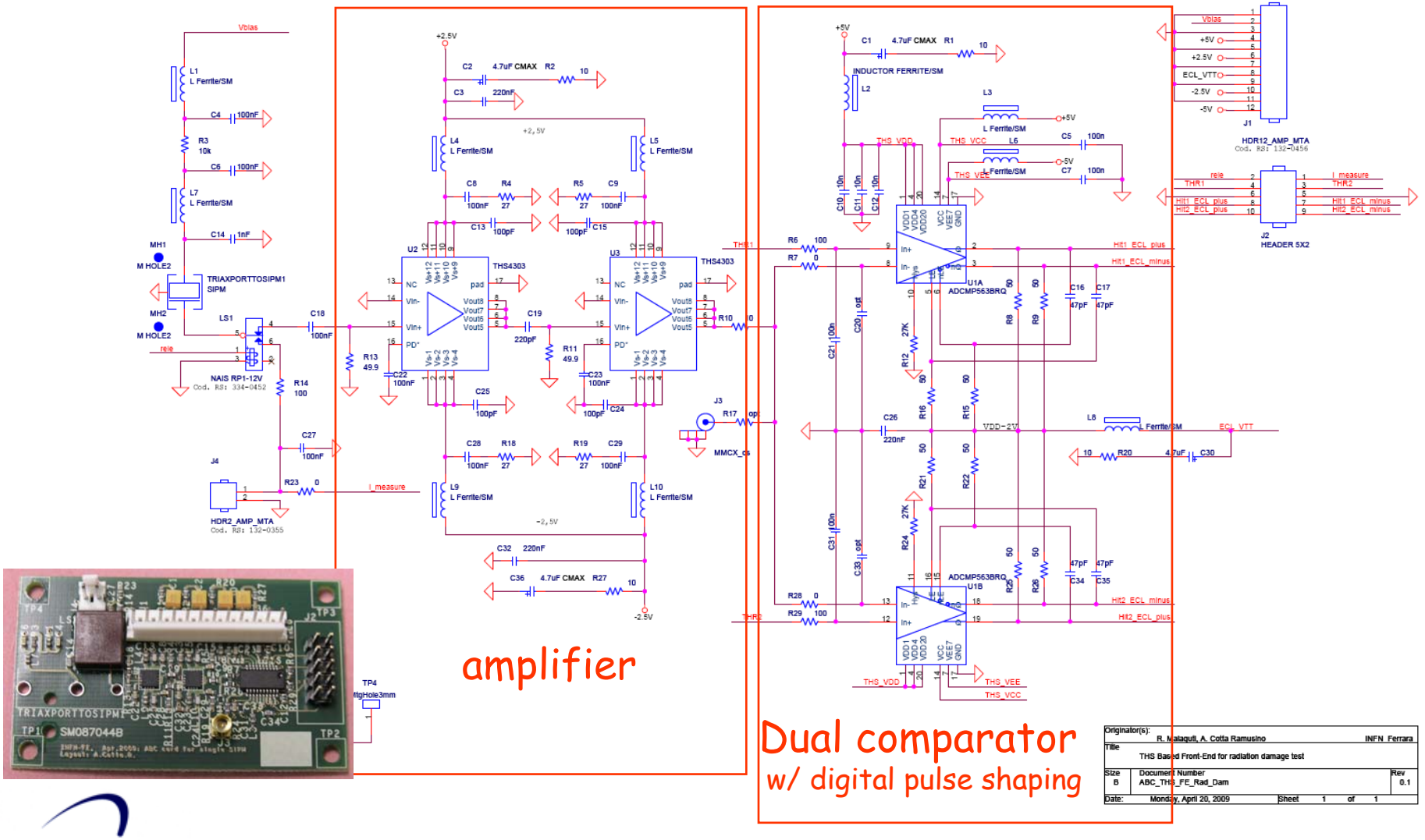
"IFR_ABC" card "core" built for radiation damage tests at FNG facility:
"MMIC-Type": based on the MMIC amplifiers BGA2748/BGA2716



amplifier

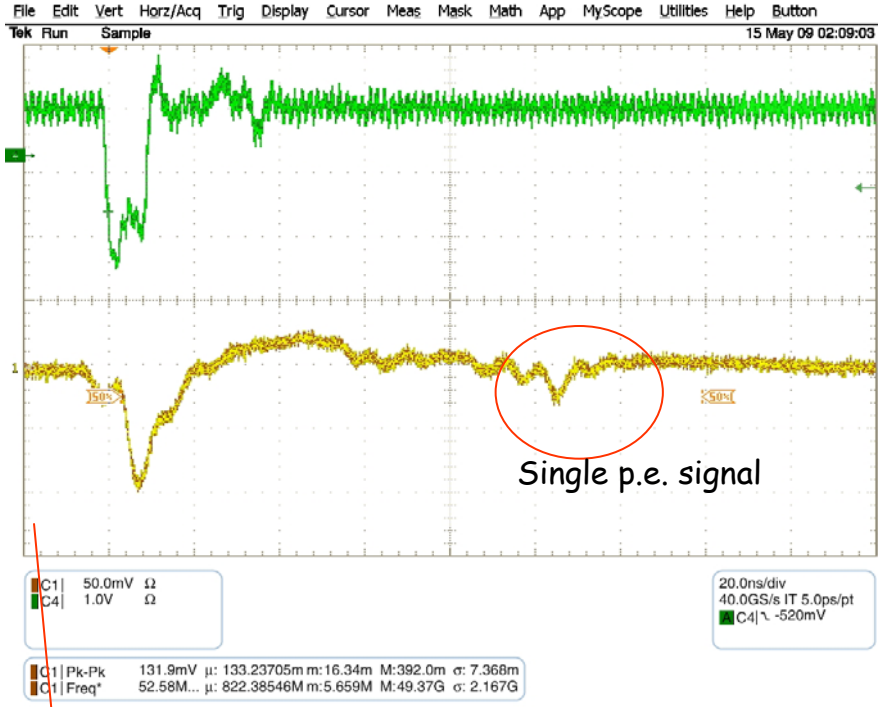
Dual comparator
w/ digital pulse shaping

"IFR_ABC" card "core" built for radiation damage tests at FNG facility.
"THS-type": based on the 10x gain op-amp THS4303

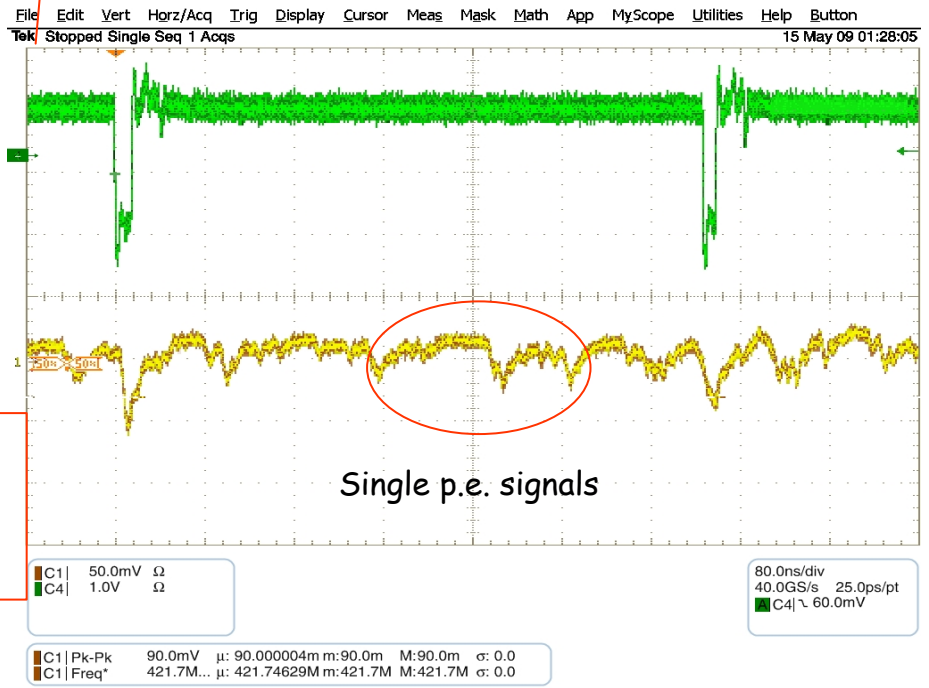


Outline of readout electronics for the SuperB IFR prototype

"IFR_ABC" card "core" waveforms:

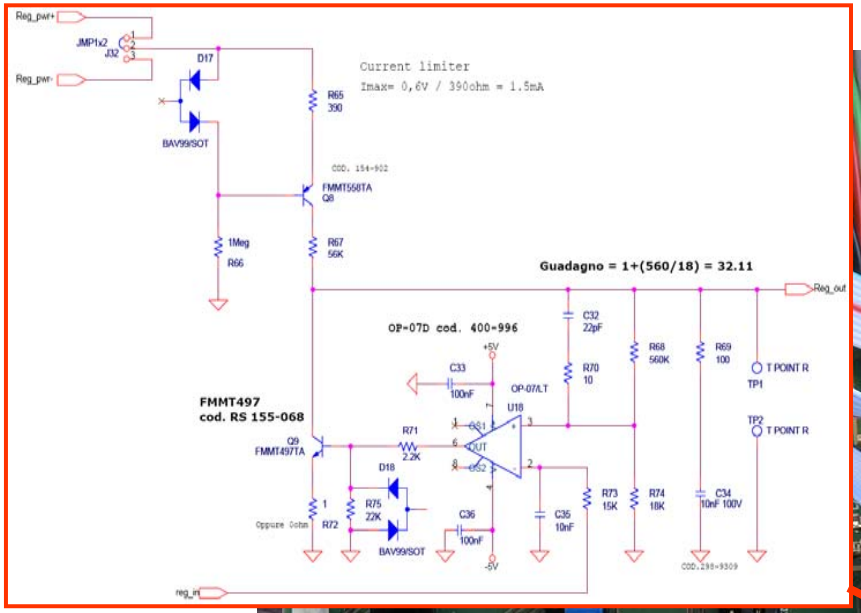


"THS-type" waveform
C1: output of ampli stage (attenuated by a factor 2)
C4: differential output of one discriminator/shaper with a threshold of -40mV

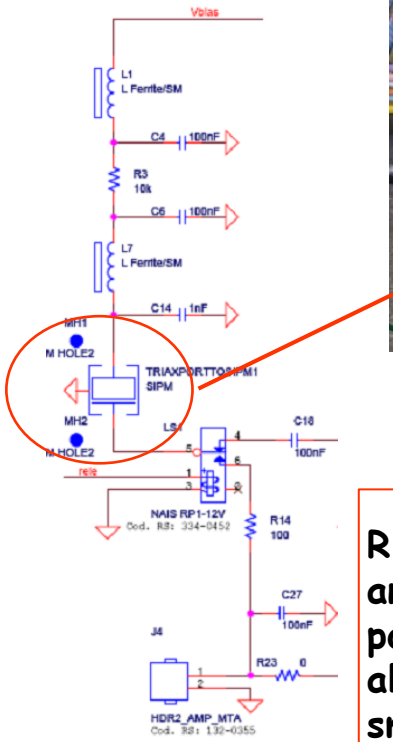


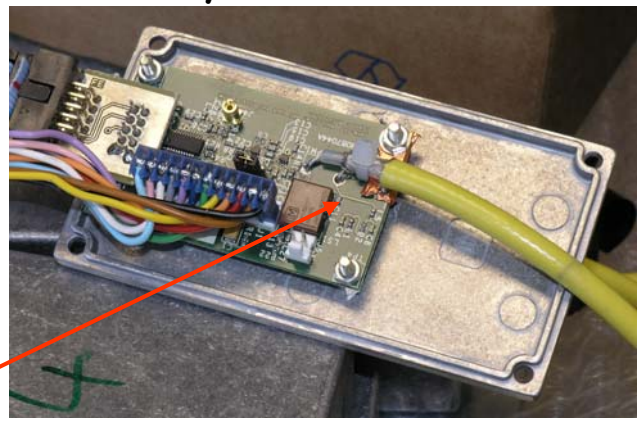
"MMIC-type" waveform
C1: output of ampli stage with (attenuated by a factor 2)
C4: differential output of one discriminator/shaper with a threshold of -150mV

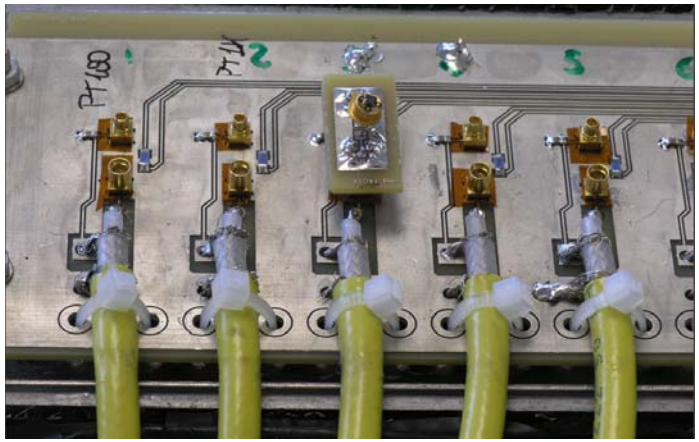
"IFR_ABC controller card" (R.Malaguti): it features, among other things, the circuitry to individually tune the bias voltage to the sensors



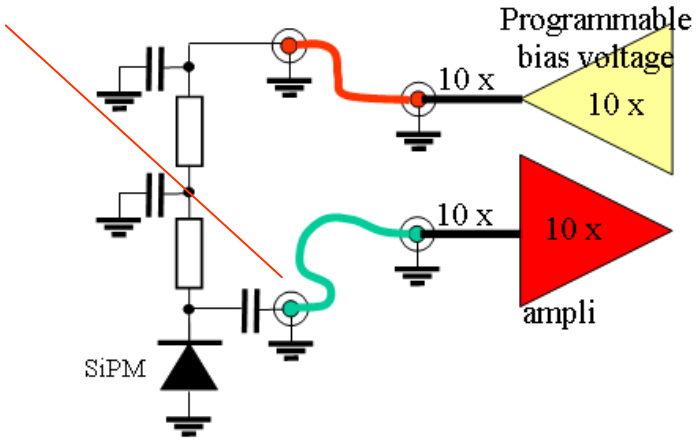
"IFR_ABC connection to sensors" (R.Malaguti): for the sensor irradiation test at the FNG facility triax cables was used:







R.Malaguti has found in literature and suggested a different sensor polarization scheme which would allow us to use a cheaper and smaller coax cable to collect the signal from the sensor (plus a coax cable to carry the bias voltage to it):



the performance of such a scheme is under evaluation

Current baseline development status:

• Core elements of the "IFR_ABC" cards have been built and have been used in the studies of aging under irradiation of the SiPM and the MMPC sensors → no radiation damage observed on the "IFR_ABC" card returned from the test at the FNG

• A preliminary design of the FPGA in the IFR_BiRO is being developed, starting from a standard NIOS-II ALTERA design and adding to it the IFR_BiRO specific modules coded in VHDL.
The NIOS-II soft processor of the standard desing runs a simple Telnet server application under a micro OS with a total footprint of 360kB. The NIOS-II code runs in an external RAM for which a DDR2 interface is also provided.

• A fully equipped LST_FE crate provided by INFN_Genova is now in Ferrara and development of the BiRO modules can start.