



APSEL6D Architecture, simulations and results

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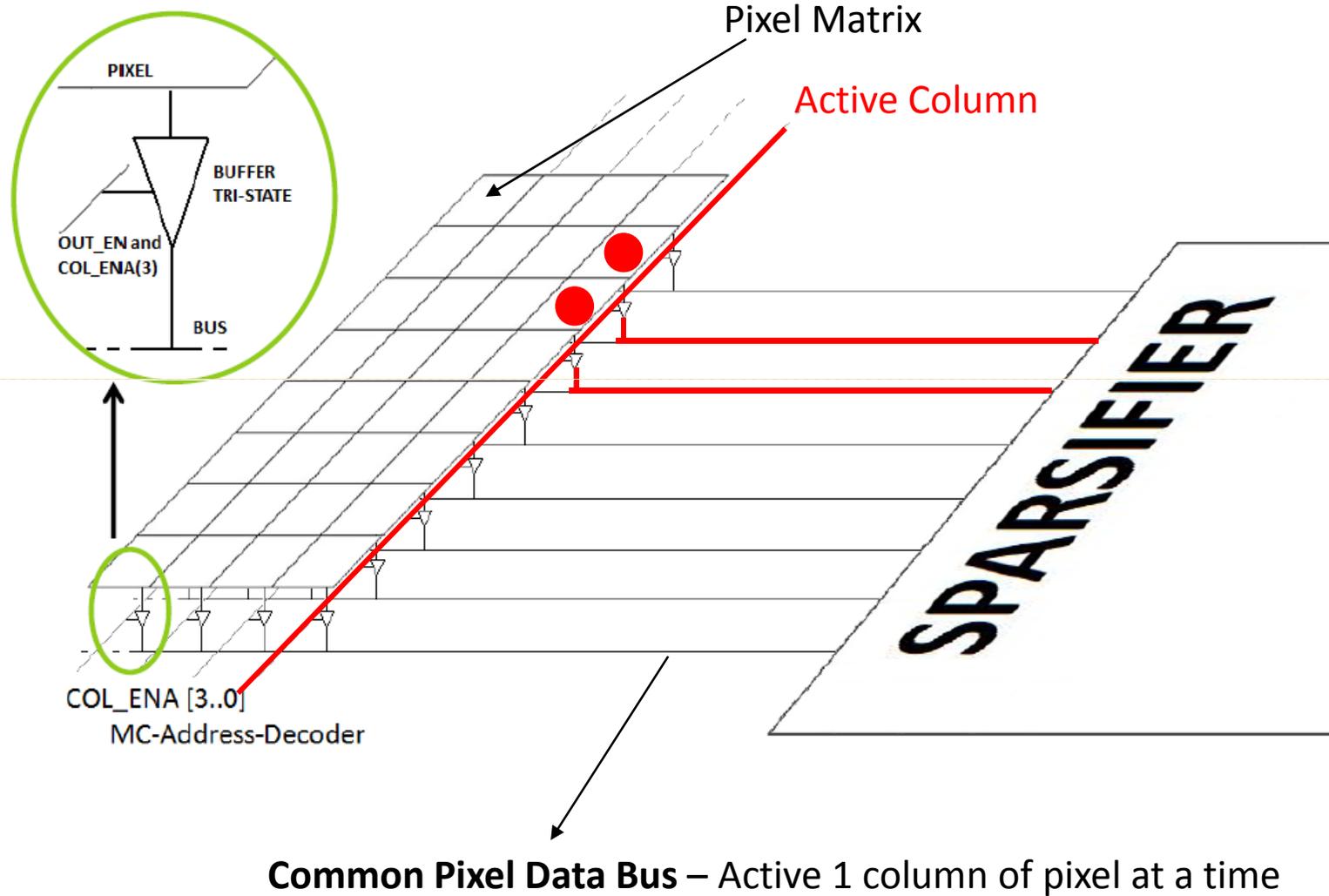
Outline

- Expected Target Conditions
- Matrix Architecture
- Readout architecture
- Simulations
- Efficiencies
- Summary

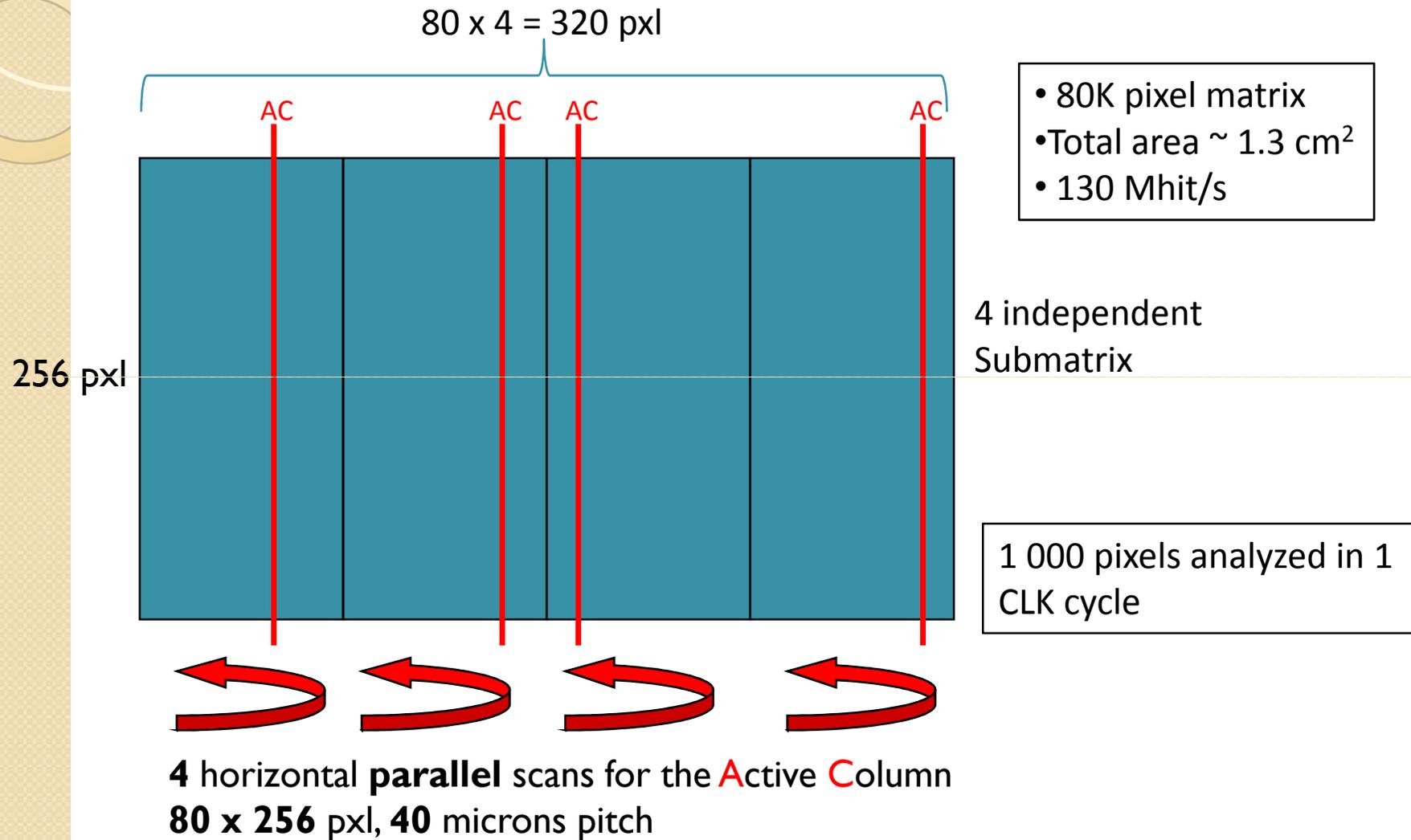
Target Conditions

- 100 MHz/cm² hit rate:
 - 25 MHz/cm² track rate (includes x5 security factor)
 - 4 MHz/cm² cluster factor
- 160 Mhit/s chip bandwidth
- 0.25 – 2.0 μs BCO clock:
 - Time Counter clock, represents the time granularity of the events.
- 60-100 MHz Matrix Read Clock

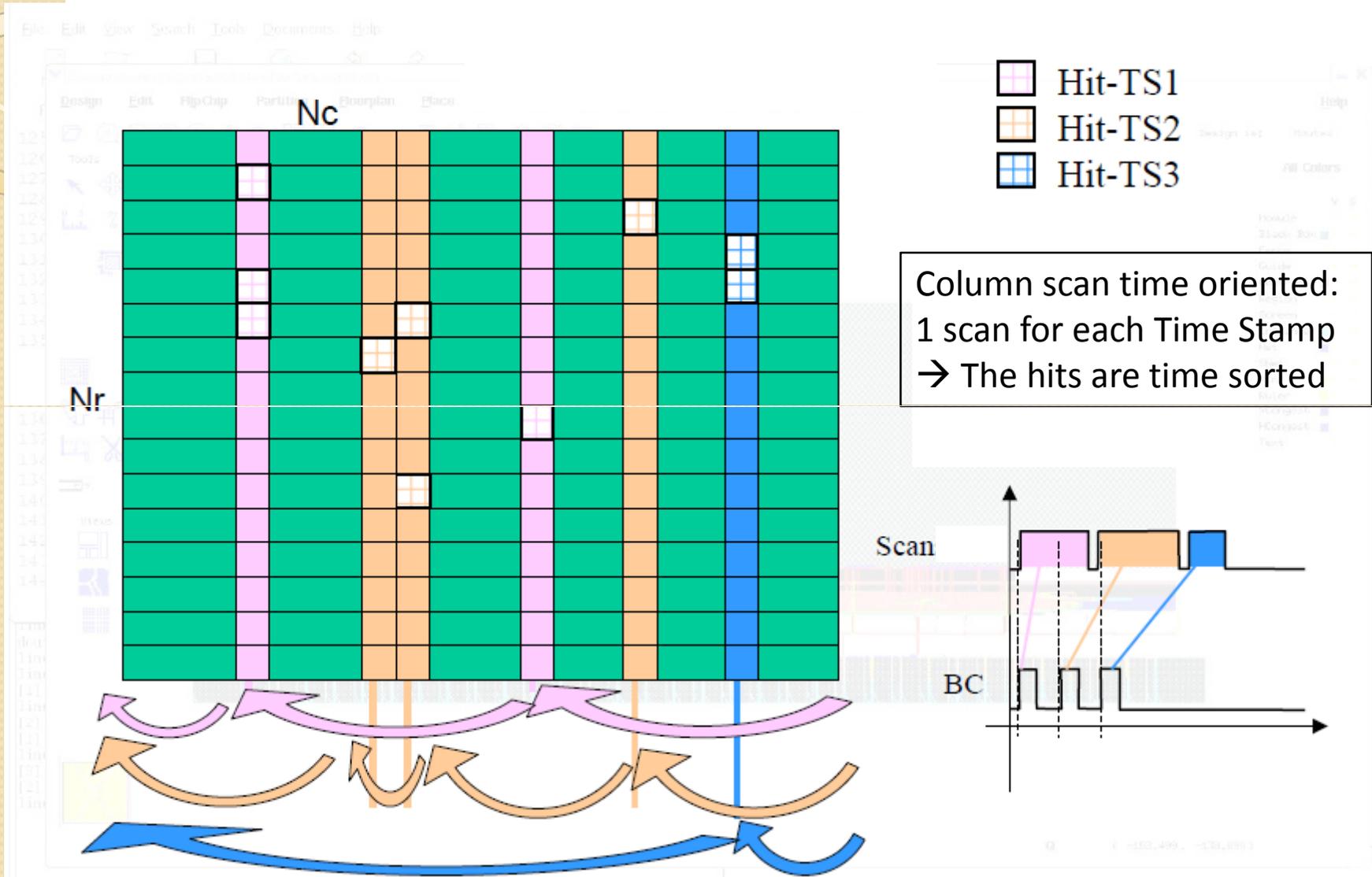
The Matrix Architecture



The Matrix 320x256 (40μm pitch)

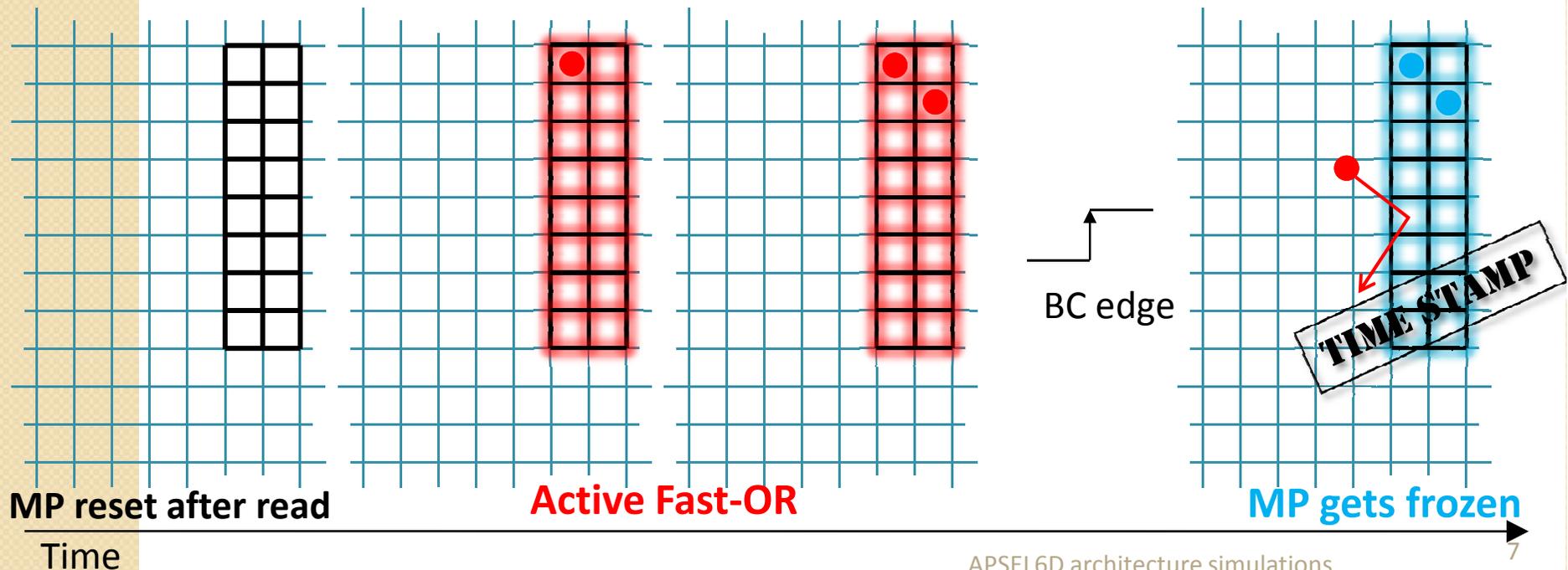


Submatrix Scan Policy



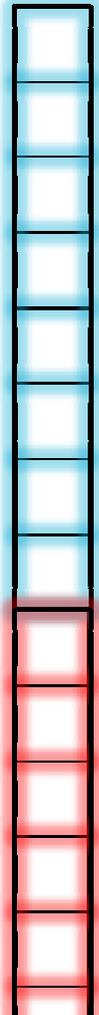
The Macro Pixels

- Matrix divided into MPs: group of pixels (2x8)
 - MP global lines:
 - **Fast-OR line:** (output) inclusive OR of all pixels.
 - **Freeze line:** (input) disable the reception of new hits.
 - On BCO clock edge all MPs with active fast-OR :
 - Gets frozen
 - Are associated to the current value of BCO counter (Time Stamp)
 - Waits to be scanned and reset



Zone sparsification of the Active Column

Active Column



Zone 0

Zone 1

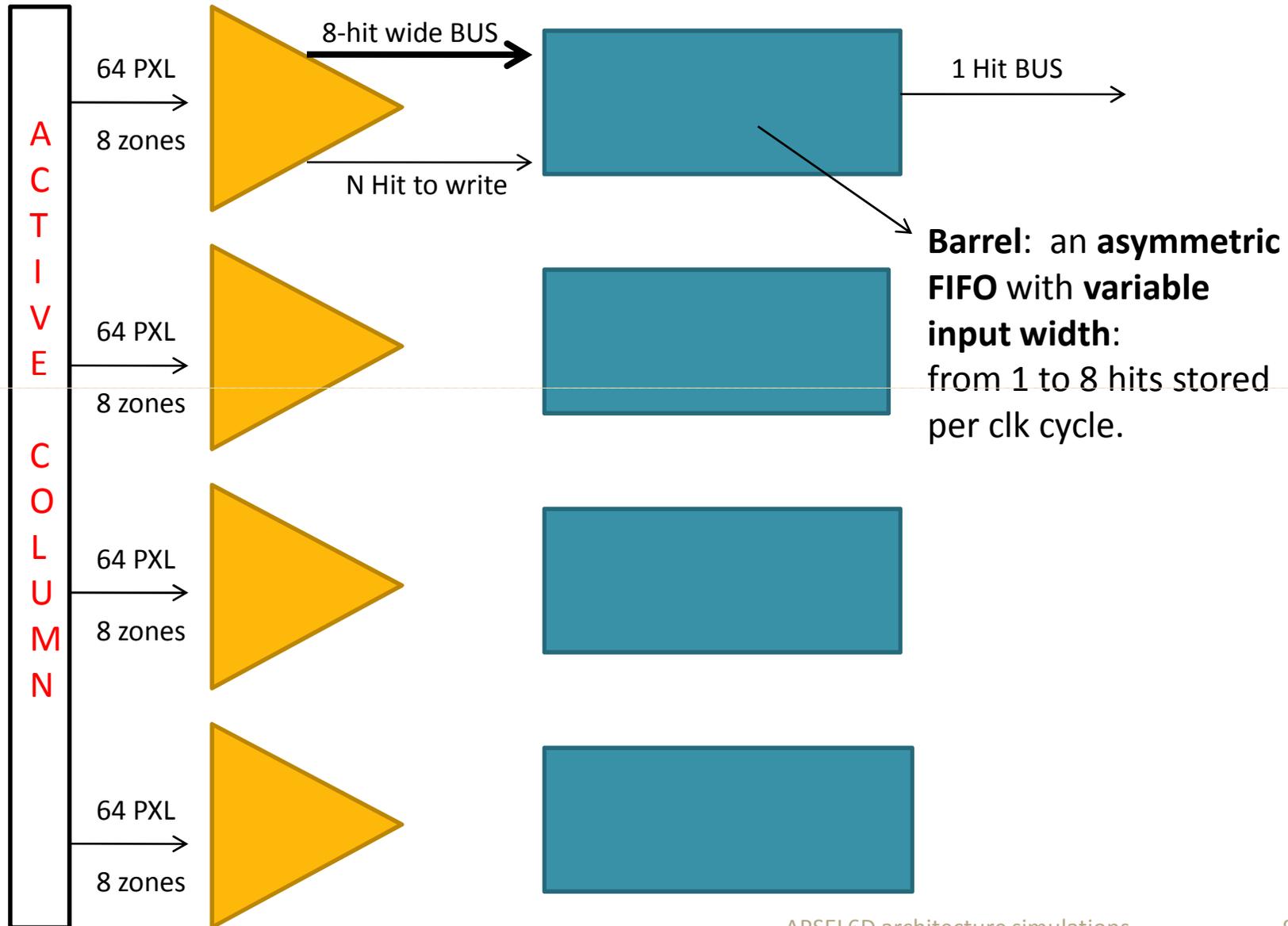


Active Column

- The **256 pixels** of the Active Column are **divided into 32 vertical zones (1x8 pixels each)**
- Every **HIT** stored contains the information of a zone, not of a single pixel:
 - **HIT= (Zone address+ Zone pattern)**
 - X zone address = Column address : 80 columns → 7 bit
 - Y zone address : 32 vertical zones → 5 bit
 - Zone pattern: 8-pixel zone → 8 bit
- **Time Stamp**: since the hits are time sorted, the relative TS word is stored at the beginning of each hit sequence

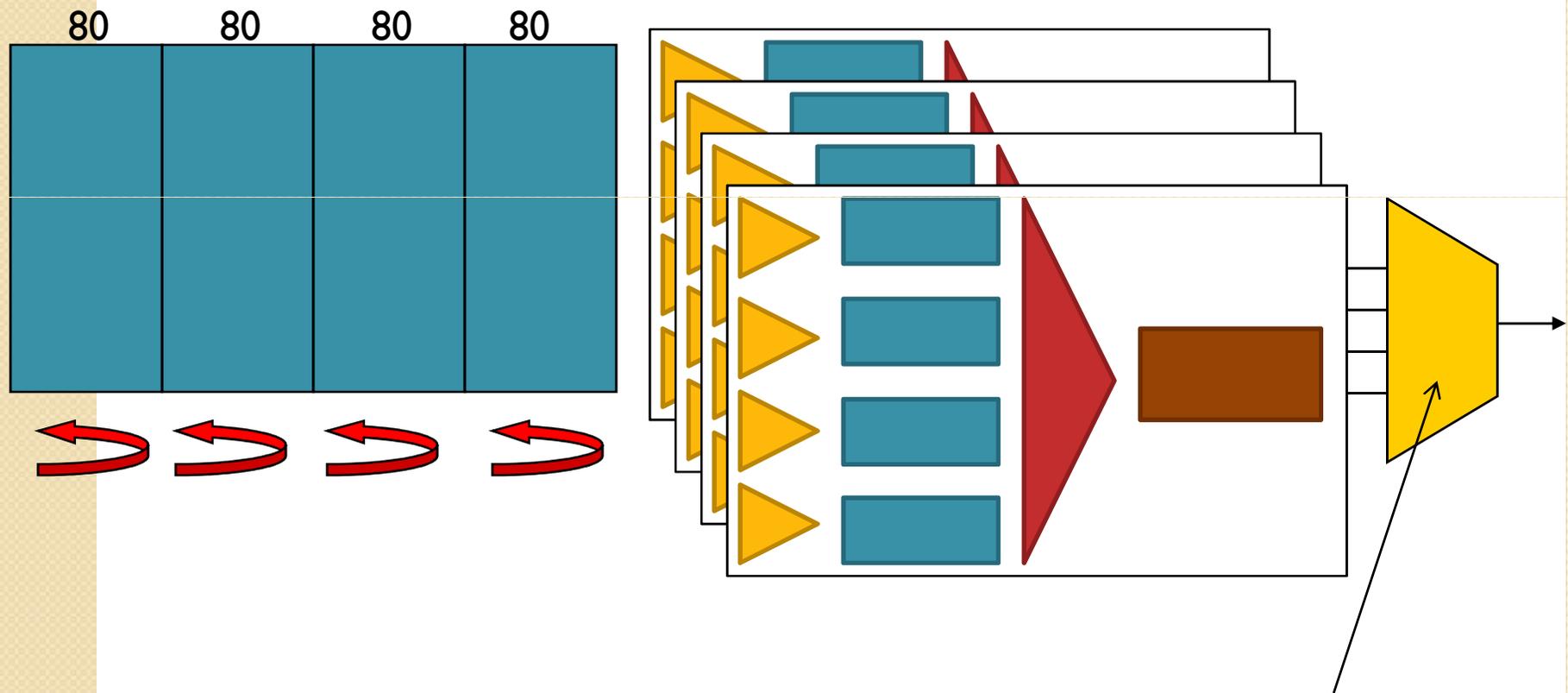


The sparsifiers and barrels



Sparsification and barrel trees

Each submatrix scan has its own readout – all working in parallel

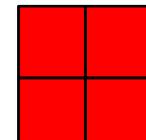


Common output stage

Output stage

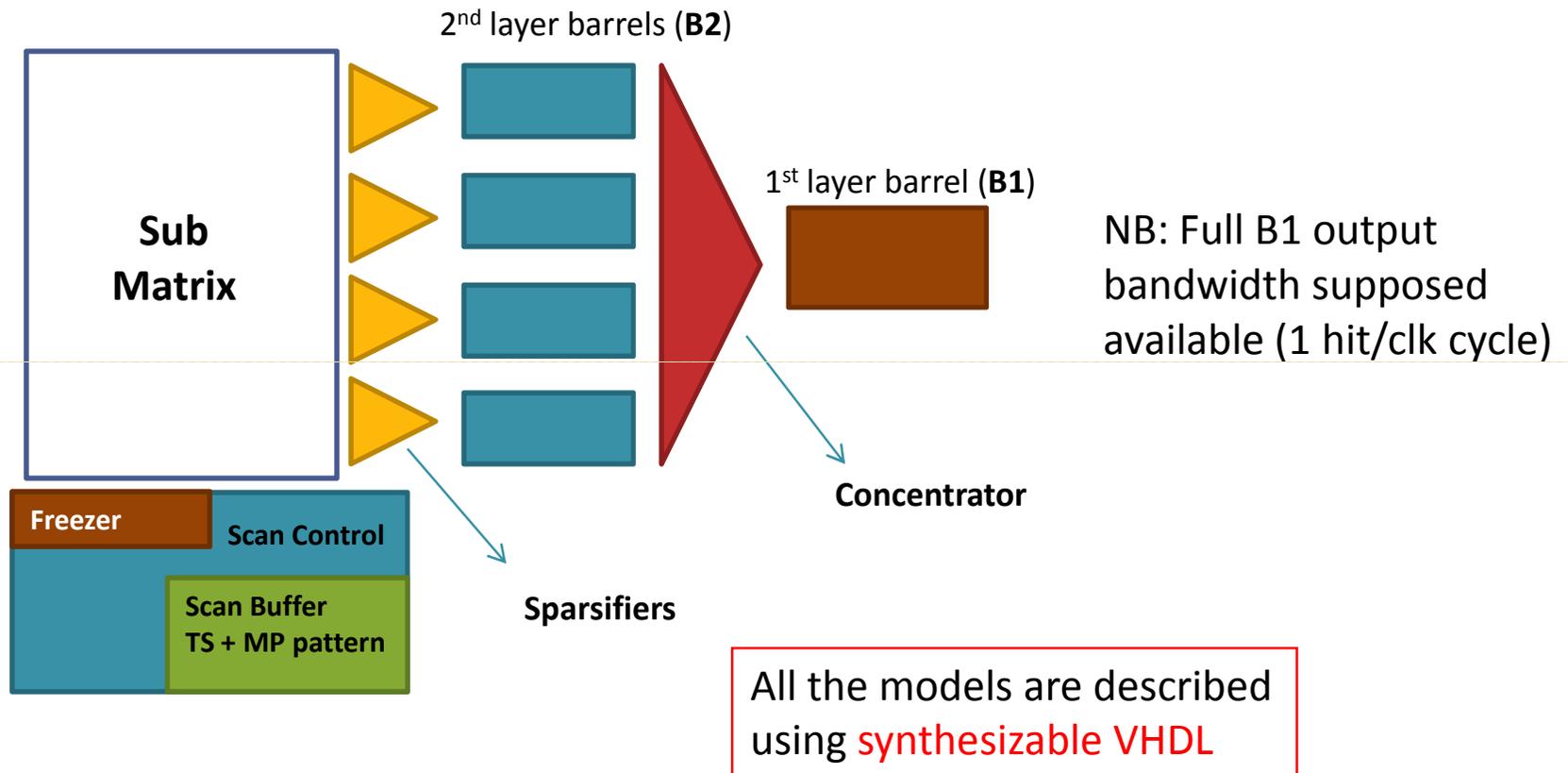
- FULL resolution Hit + time stamp
 - 8 bit TS (modulo 256 BCO counter)
 - 9 bit X address (320 pixels)
 - 8 bit Y address (256 pixels)
 - TOT **25 bit**
 - → expected rate **130 MHit/s per chip = 130MHz x 25bit = 3.2 Gbps**
- Zone sparsification & time sorting of the hits (TS heading the relative hits) lead to:
 - 2 bit Barrel L2 address (→ 1/4 of submatrix: 80x64 pxl)
 - 2 bit Barrel L1 address (1 submatrix: 80x256 pxl)
 - 7 bit X address (80 pixels)
 - 3 bit zone Y address (8 vertical zones for each L2 barrel)
 - 8 bit zone pattern
 - TOT **22 bit**
 - → expected rate: **130 (+1 TS) * 22 = 2.8 Gbps**

BUT: Considering the cluster factor **x4** of the expected rate in the form **2x2**:
in 87.5% of cases **2** hits only & in **12.5%** are required **4** hits

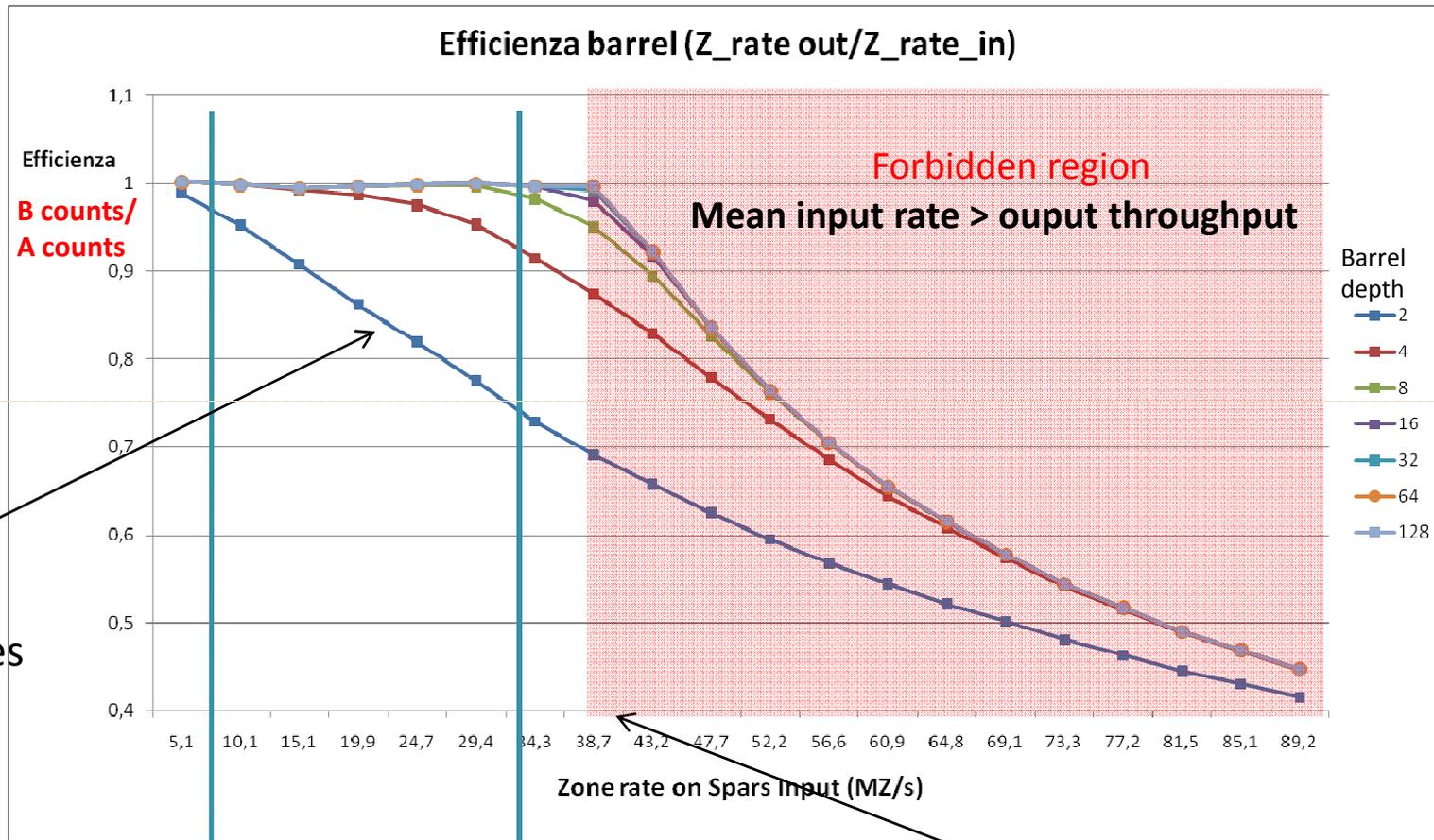
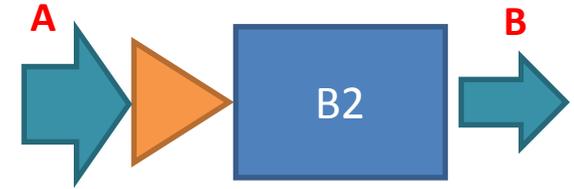


- → **[(22*2)* 0.875 + (22*4)*0.125] * 25 Mtrack s⁻¹ cm⁻² * 1.3 cm²**
 - **Weighted average ~ 1.6 Gbps**

The components simulated:



Study on Barrel optimal Depth:



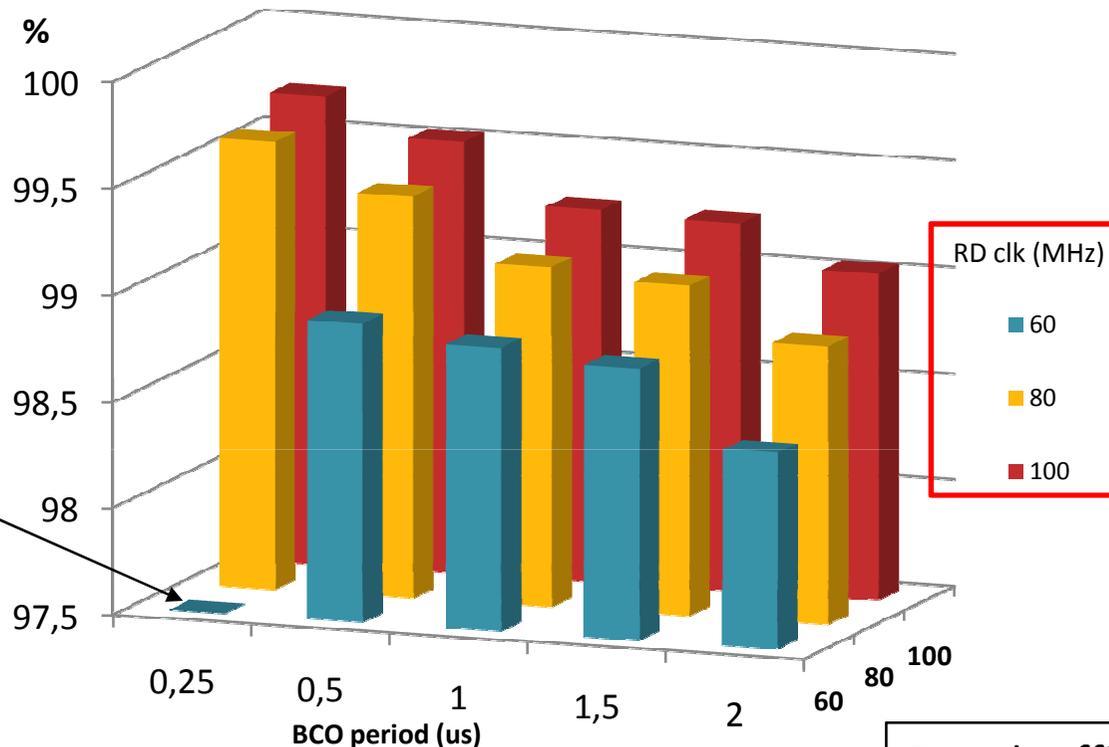
Barrel inefficiencies due to fluctuation over the mean rate

Expected rate @B2:
8,2 MPxl/s

Expected rate @B1:
32,8 MPxl/s

Barrel clock 40 MHz

Frozen Efficiency @ 100 MHz/cm²



Readout efficiency not 100% :
Scan buffer overflow

Barrels efficiency **100%**
No barrel overflow
(B2 and B1)

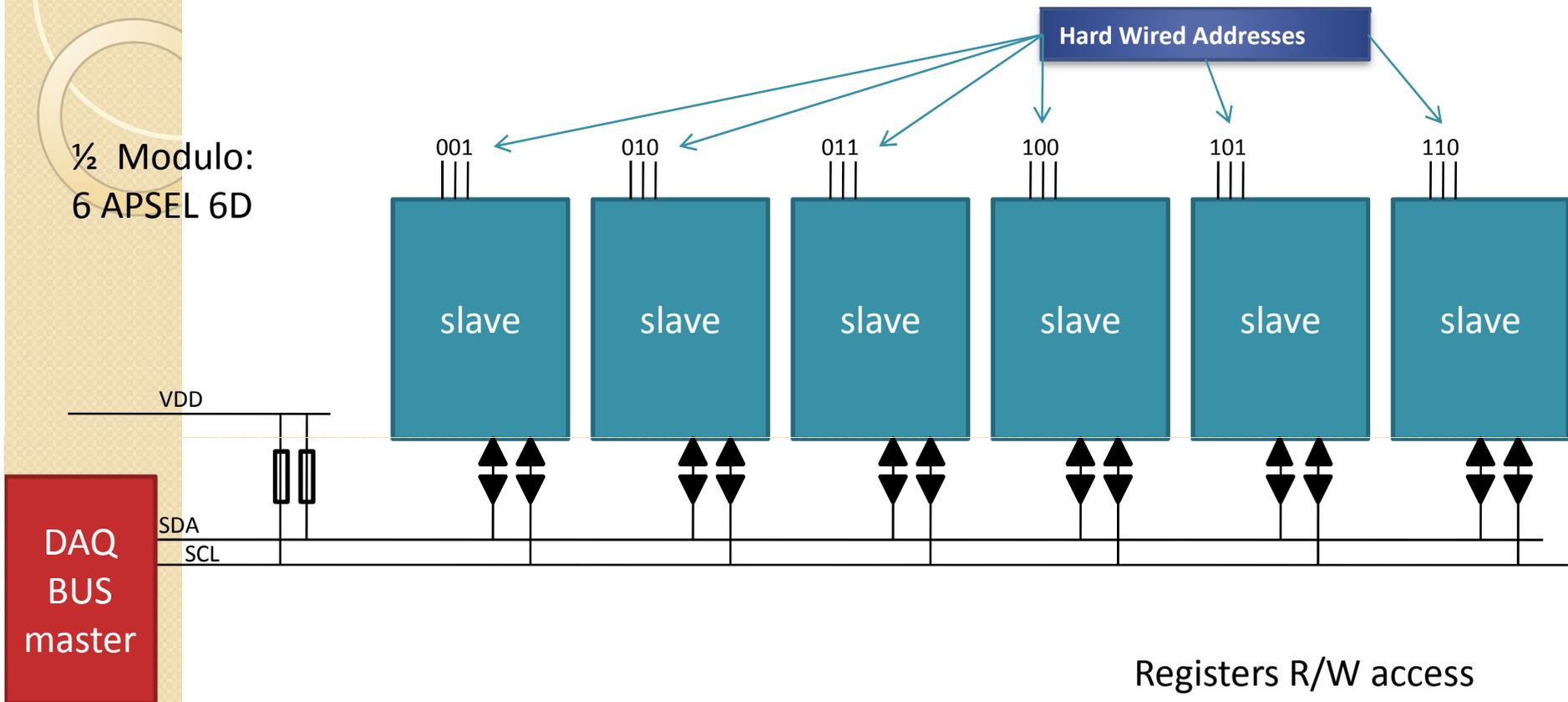
frozen effi.						
				BCO (us)		
			0,25	0,5	1	1,5
	100	99,7	99,5	99,3	99,2	99,0
Rd_clk (MHz)	80	99,6	99,4	99,1	99,1	98,8
	60	97,5	98,9	98,8	98,8	98,4

Fast read clock and narrow BC edges

NB: for 200 MHz/cm² minimum Rdclk 80MHz and efficiency with BC=1 us is 97.6%

Slow Control : I2C-like system

½ Modulo:
6 APSEL 6D



Registers R/W access
communication type

I²C : two bidirectional open-drain lines.
•Serial Data (SDA)
•Serial Clock (SCL), pulled up with resistors.

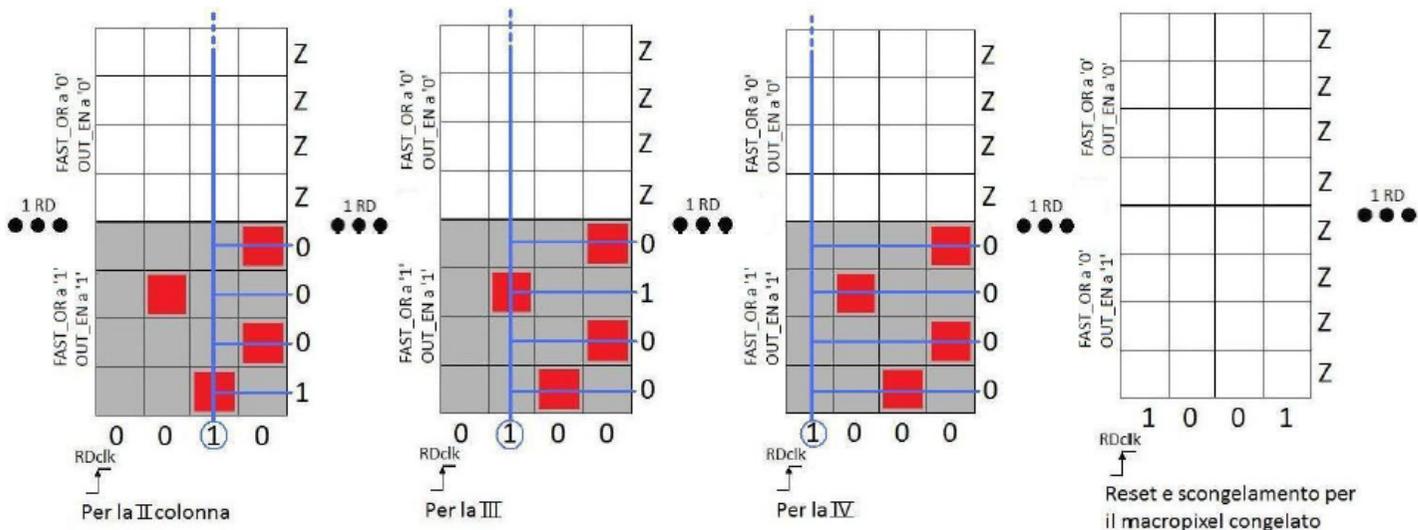
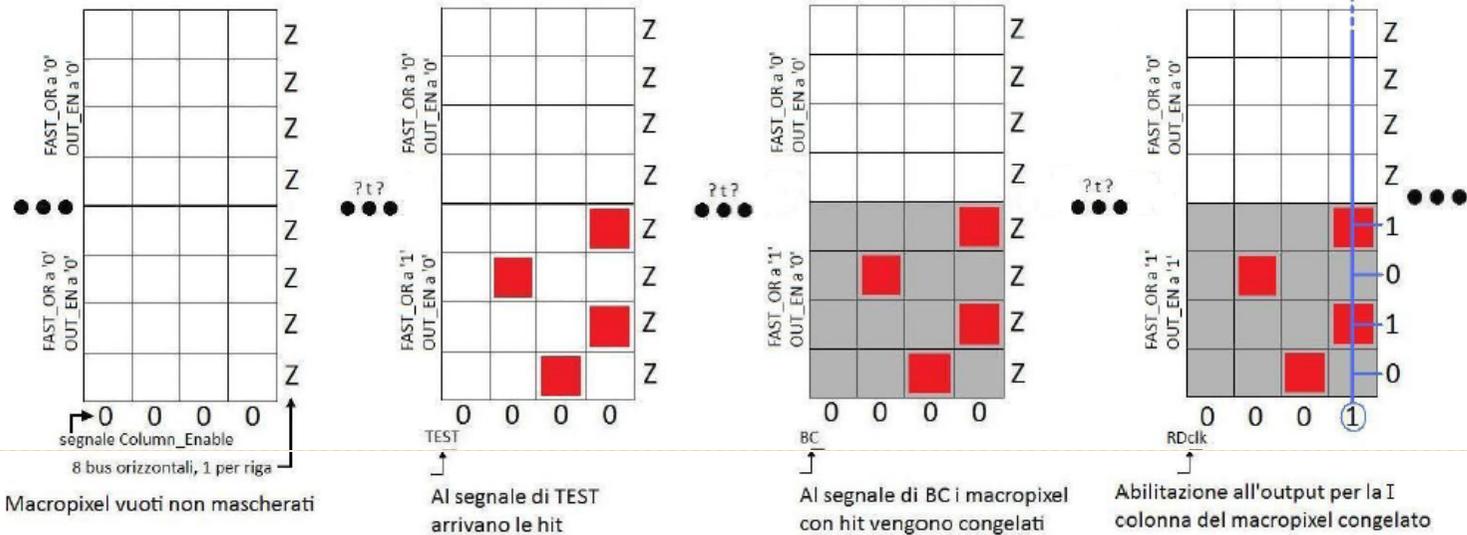
Conclusions

- Study conducted to point out the optimal readout policy and architecture.
- A parametrized model has been coded with synthesizable VHDL.
- Simulations performed allowed a fine adjustment of the free parameters, and showed for a “typical” configuration a global readout efficiency: above 98,4%
- Works in progress:
 - Realization of the final output stage
 - I2C like interface for slow control
- To Do
 - Service infrastructure (killmask, MP mask, calib facilities...)
 - Selection of the elements to be implemented in the sett 09 chip



BACKUP SLIDES

Macro Pixel Cycle



2D scan BCO vs RDclk @ 1MHz/mm2

RN	sim DURATION (us)	RDclk (MHz)	BCO (us)	Mean Sweeping time (us)	global hit rate (MHz)	rate on area (MHz/mm2)	B2 depth	B1 depth	B1 max fill	B1 mean fill	BC lost	Already hit effi (%)	frozen effi (%)	ro effi B2 (%)	ro effi B1 (%)
107	1	60	0,5	0,45	33,8	1.03	8	32	5	1	0	99,96	98,90	100	100
108	1	80	0,5	0,34	33,8	1.03	8	32	5	1	0	99,95	99,39	100	100
109	1	100	0,5	0,27	33,8	1.03	8	32	5	0	0	99,96	99,53	100	100
110	1	60	1	0,75	33,8	1.03	8	32	8	1	0	99,91	98,83	100	100
111	1	80	1	0,56	33,8	1.03	8	32	9	1	0	99,91	99,10	100	100
112	1	100	1	0,45	33,8	1.03	8	32	9	1	0	99,91	99,25	100	100
113	1	60	1,5	0,95	33,8	1.03	8	32	19	1	0	99,86	98,78	100	100
114	1	80	1,5	0,71	33,8	1.03	8	32	18	1	0	99,86	99,05	100	100
115	1	100	1,5	0,57	33,8	1.03	8	32	18	1	0	99,86	99,23	100	100
116	1	60	2	1,08	33,8	1.03	8	32	24	3	0	99,84	98,42	100	100
117	1	80	2	0,81	33,8	1.03	8	32	23	2	0	99,83	98,81	100	100
118	1	100	2	0,65	33,8	1.03	8	32	23	2	0	99,83	99,04	100	100