Front-End Analog Cell Optimization for Hybrid Pixel Sensors

G. Traversi[a], L. Gaioni[b], A. Manazza[b], M. Manghisoni[a], L. Ratti[b],
V. Re[a], V. Speziali[b]

[a]Università degli Studi di Bergamo and INFN Pavia
[b]Università degli Studi di Pavia and INFN Pavia

INFN Istituto Nazionale di Fisica Nucleare

SuperB

Introduction: Layer0 activities

- Need a new SVT (very similar to that of the 5 layer BaBar SVT) supplemented by a new layer 0 to measure the first hit as close as possible to the production vertex. Goal is coverage to 300mrad both forward and backward.

- Striplets: thin double sided silicon sensor with short strips. Mature technology, not so robust against background.

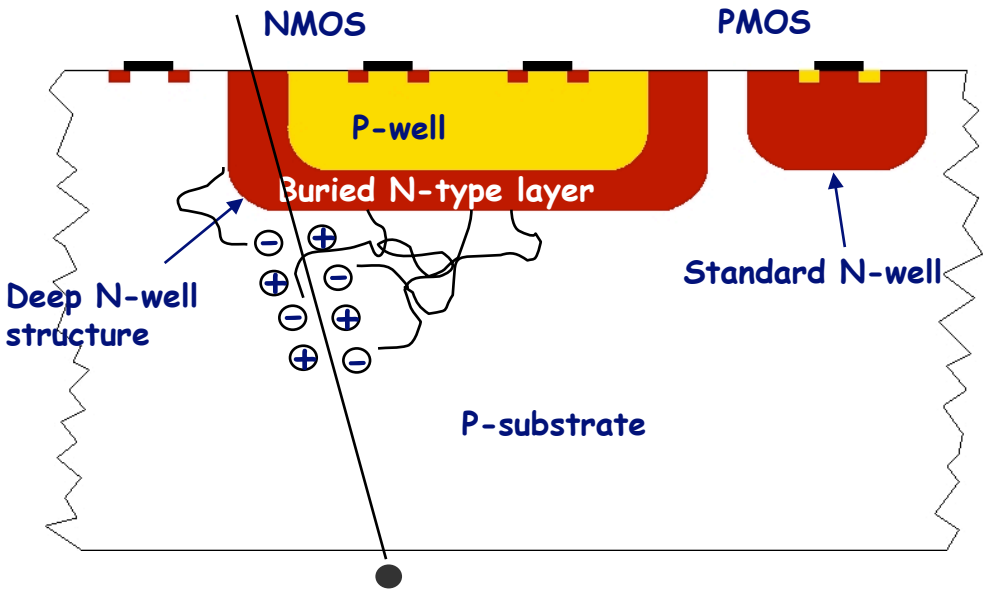
- CMOS MAPS: very promising technology, sensor & readout in 50um thick chip. Extensive R&D (SLIM5-Collaboration) on Deep N-Well devices 50x50um^2 with fast readout architecture.

  - DNW MAPS in a planar (2D) 130nm CMOS technology provided by STMicroelectronics. Apsel4D: successfully tested on a test beam Sept. 2008 @CERN. New version with improved sensor and FE performance (Apsel5T) fabricated and now under test.

  - DNW MAPS in a vertically integrated (3D) 130nm CMOS technology provided by Chartered/ Tezzaron semiconductor. First prototype with APSEL structures submitted in May (V. Re's talk).

- Hybrid Pixel: it could become the baseline Layer0 option for the TDR in case MAPS are not considered mature enough by that time. Need to demonstrate by 2010 that reduction in the front-end pitch to 50x50um^2 and in the total material budget is possible to meet Layer0 requirements. Front-end pitch reduced to 50x50um^2 in a first prototype chip submitted in Sept. 2009 and test beam in Sept. 2010. We plan to use pixel detectors (high resistivity) fabricated by FBK-IRST and interconnected with FE chip by IZM.

Deep N-Well CMOS MAPS



- In triple-well CMOS processes a deep N-well is used to shield N-channel devices from substrate noise in mixed-signal circuits
- DNW MAPS is based on the same working principle as standard MAPS

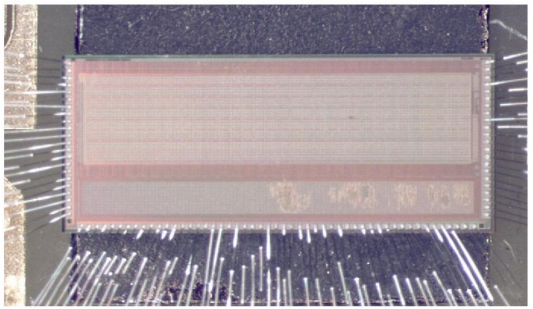
- Classical optimum signal processing chain for capacitive detector can be implemented at pixel level
- The collecting electrode (DNW) can be exploited to obtain higher single pixel collected charge
- A charge preamplifier is used for Q-V conversion → gain decoupled from electrode capacitance
- DNW may house NMOS transistors and using a large detector area, PMOS devices may be included in the front-end design → charge collection efficiency depends on the ratio between the DNW area and the area of all the N-wells (deep and standard)

Status of Deep N-Well MAPS

Sensors with different sparsified readout architectures and pixel pitches were developed for SuperB (large background, equivalent to a continuous beam operation) and for ILC (intertrain readout) in INFN programs.

The first generation of Deep N-Well CMOS MAPS with in-pixel sparsification and time stamping was successfully tested.

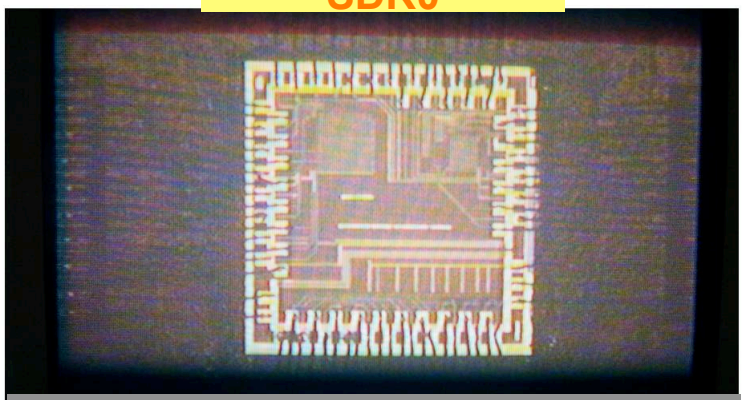
APSEL4D



32x128 matrix.
Data Driven, continuously operating sparsified readout
Beam test Sep. 2008

50x50 um pitch

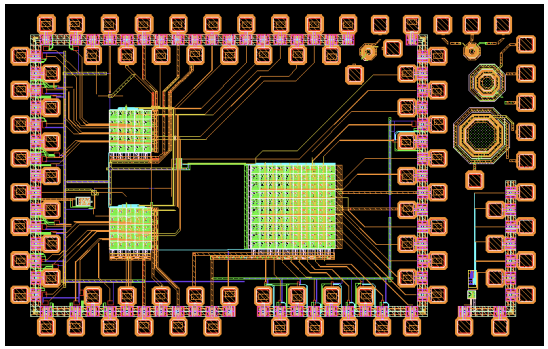
SDR0



16x16 matrix, Intertrain sparsified readout

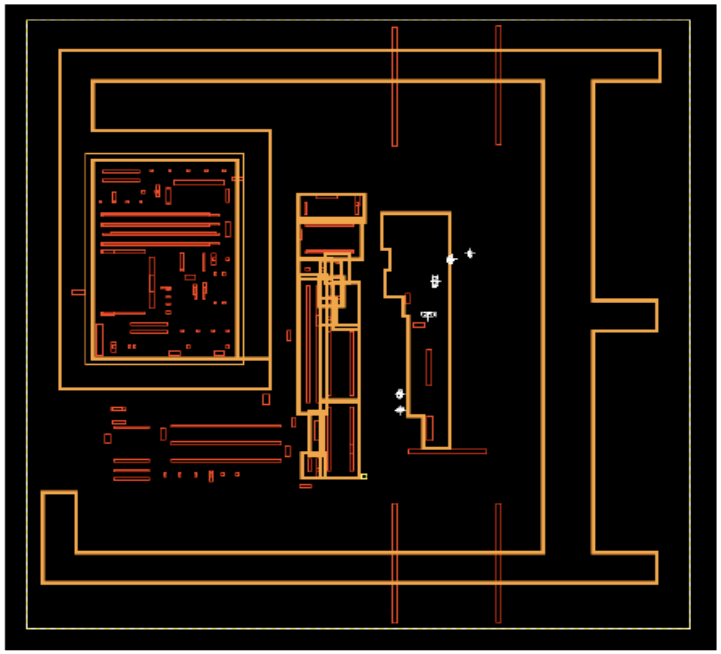
25x25 um pitch

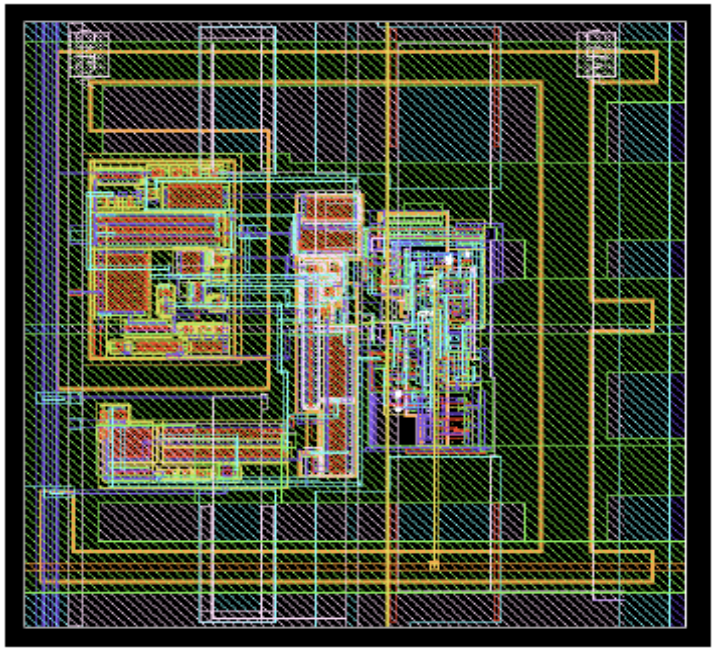
Layout of Apsel5T



Apsel5T: sensor layout

- Scaling to larger matrix size (128x128 or 320x80) dictates to remove the shaper stage to make room for additional macropixel private lines
- Shaper less front-end makes it possible to reduce the pixel pitch (from 50x50um^2 to 40x40um^2)
- Optimized cell with satellite N-wells surrounding PMOS competitive N-wells in APSEL5T ⇒ Efficiency ~ 99% (from TCAD simulations)
- Beam test results of APSEL4D show a ~90% efficiency, which agrees very well with TCAD simulations
- Metal shielding between analog and digital voltages was improved and made compatible with a large matrix

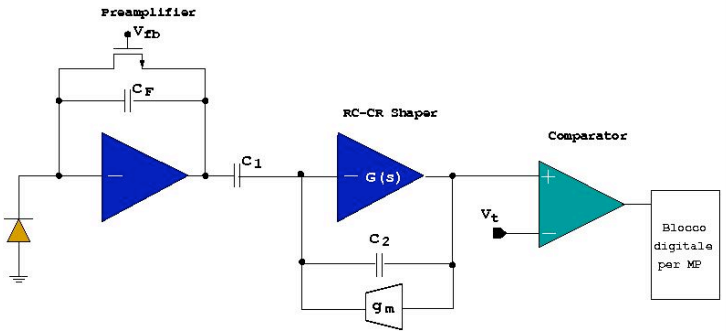




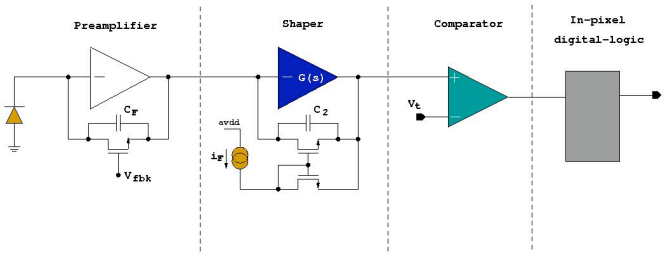
Front-end analog cell for hybrid pixel sensors

- Three different readout channel architectures have been studied

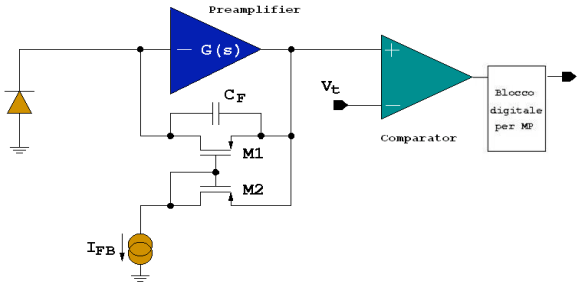
RC-CR shaper with 100ns peaking time



Shaper with current mirror feedback

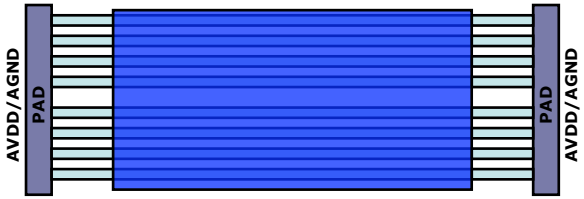


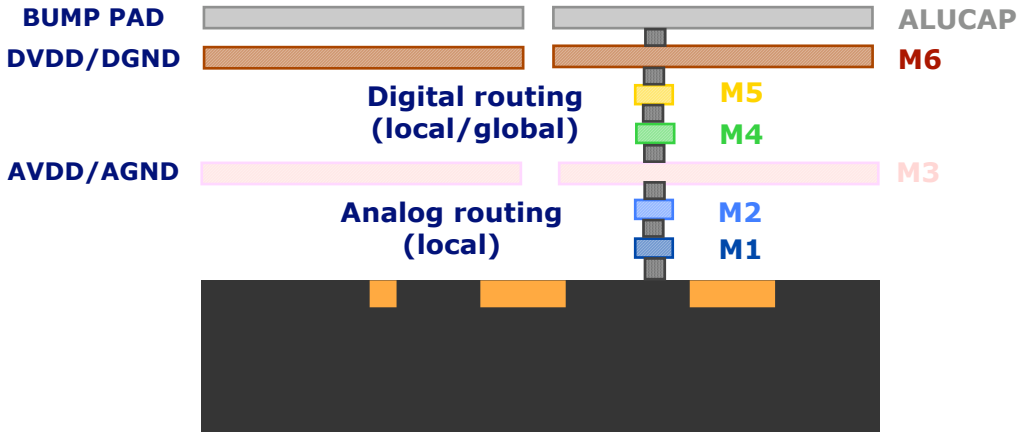
Shaper-less front-end



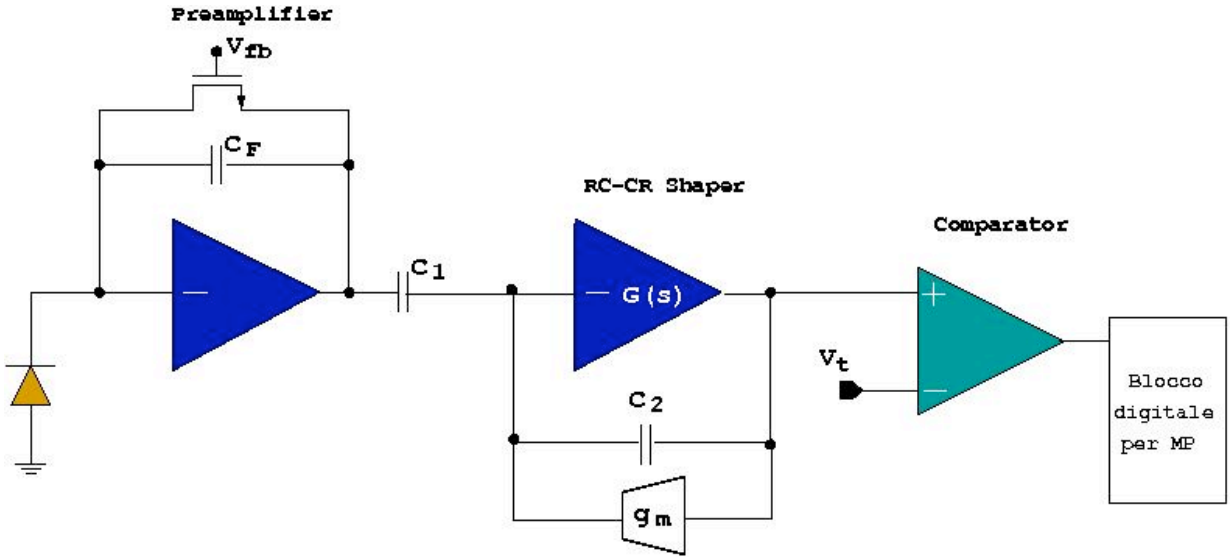
Analog cell for hybrid pixel sensors: specifications & constraints

- Analog current ≈ 1uA/pixel => minimize AVDD drop (P_{TOT} dominated by digital power ≈ 1W/cm² @160MHz clock)
- Pixel capacitance ≈ 100fF
- I_{leak} ≈ 200fA
- Shaping time ≈ 100ns (return to baseline < 3us => minimize dead time during which the cell is blind)
- Charge/pixel (MPV) ≈ 16000-4000 e-/pixel
- S/N ≈ 25 for minimal charge (S=4000e- => ENC≈160e-)
- Analog channel + in-pixel digital-logic + structures for testing FE chip w/o sensors in 50x50um²
- STM 130nm CMOS technology
- 6+1 metal layers
- No MIM CAPs allowed

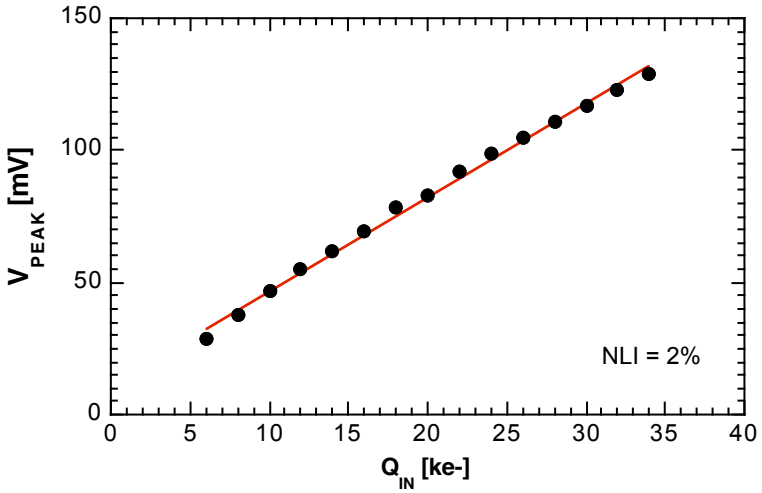




RC-CR shaper with 100ns peaking time

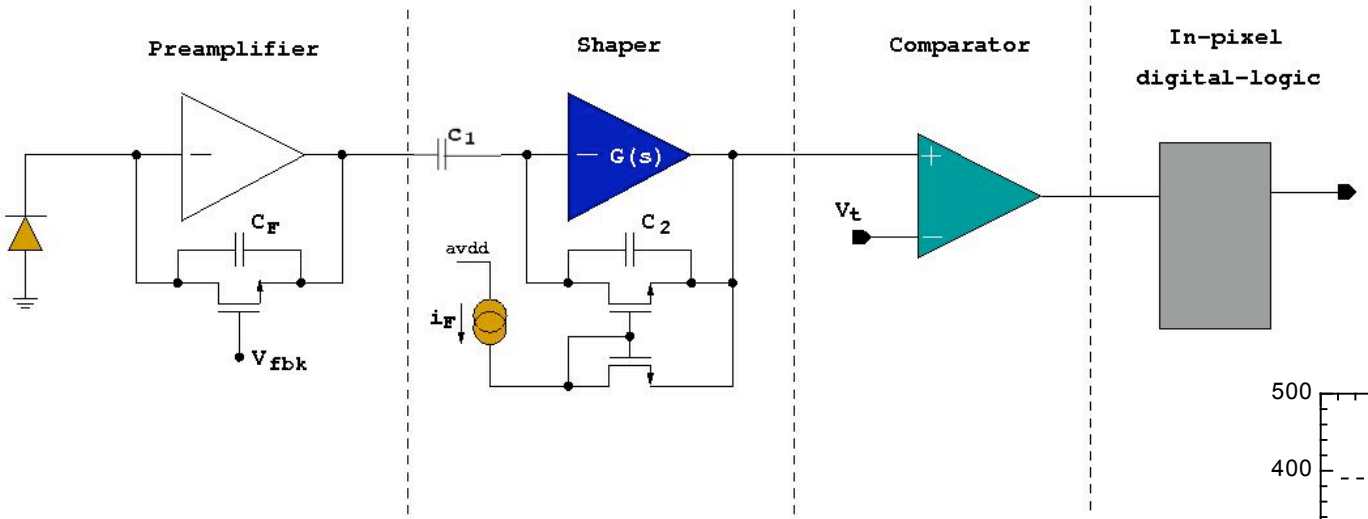


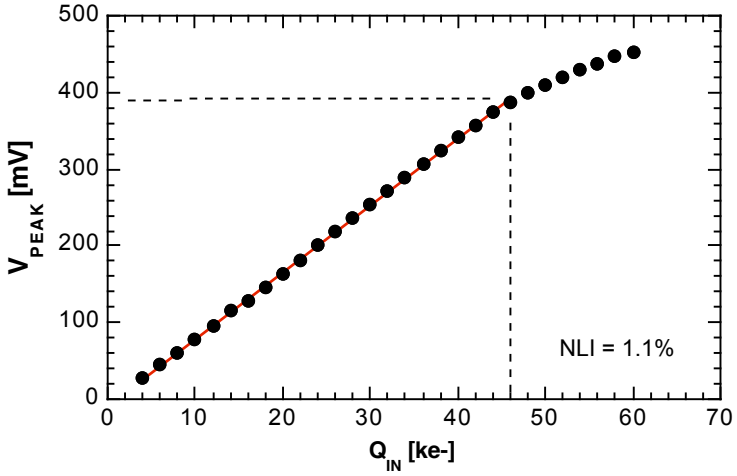
- I_{AVDD} ≈ 1.2 uA, power dissipated ≈ 1.4uW
- Charge sensitivity ≈ 40mV/fC
- ENC = 200e- @ C_D=100fF
- Threshold dispersion ≈ 320e-



- ✓ Constant recovery time
- ✗ Area for NMOS in DNW for C1, C2 and C_F
- 50x50um² not enough for low threshold dispersion analog front-end
- No room for threshold fine tuning circuits (DAC)

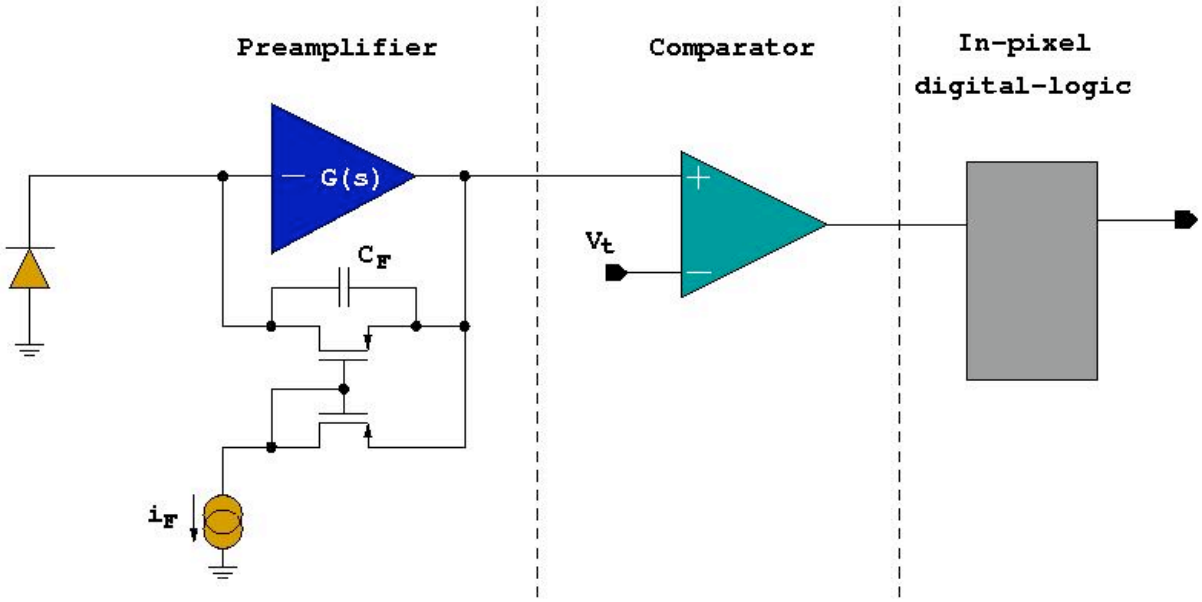
Shaper with current mirror feedback

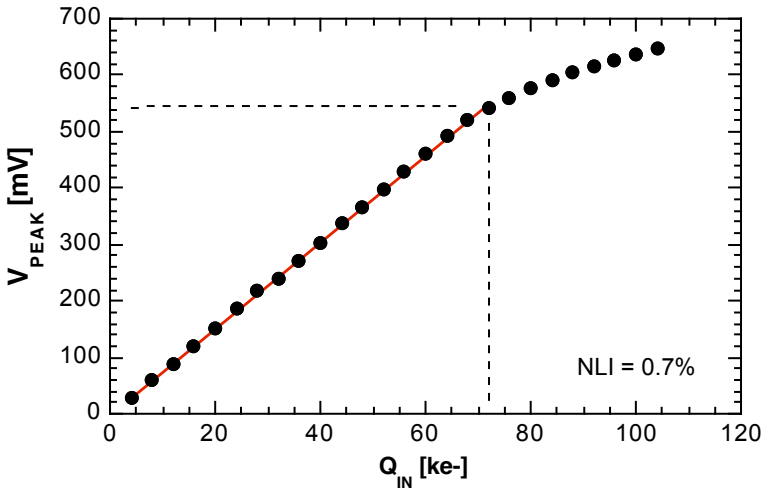




- I_{AVDD} ≈ 1.5 uA, power dissipated ≈ 1.8uW
- Charge sensitivity ≈ 40mV/fC
- ENC = 190e- @ C_D=100fF
- Threshold dispersion ≈ 175e-
- NMOS with DNW for C1 and C2
- NMOS current mirror structure continuously resetting the shaper feedback capacitor C_2.
- The recovery time increases linearly with the signal amplitude (this filtering technique lends itself to amplitude-to-time conversion).

Shaper-less front-end





- I_{AVDD} ≈ 1 uA, power dissipated ≈ 1.2uW
- Charge sensitivity ≈ 45mV/fC
- ENC = 150e- @ C_D=100fF (high frequency noise contribution has been reduced limiting the PA bandwidth)
- Threshold dispersion ≈ 190e-
- The recovery time increases linearly with the signal amplitude
- ✓ More room is available for test structures (Cinj, kill mask, internal pulser, …)

Preliminary

Conclusions and future plans

In R&D activity for the Layer0 of SuperB three different approaches are being followed

- Latest version of Apsel family chip (Apsel5T) has been fabricated in a planar 130nm DNW CMOS technology (STMicroelectronics) and test are in progress

- First prototype of an Apsel-like chip has been submitted for fabrication in a 130nm vertically integrated (3D) CMOS technology

- We are investigating the possibility to design a fine pixel pitch (50x50um2) analog front-end for hybrid pixel detector

  Three different readout channel architectures have been studied